T-Stamp/Sync (TS/S) Module Specs -- Functional Overview
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1. Input/Output Connections

The Time-Stamp/Sync (T-stamp/Sync, or TS/S) module is a single-wide VME module that can serve either as a Time Stamp Master or Time Stamp Receiver, selectable with a hardwire jumper.

The module has the following input and output connections:

1. Clk In	TTL, 50 ohm
2. Sync1/T-stamp In	TTL, 50 ohm
3. Sync2	TTL, 50 ohm
4. Timer Reset	TTL, 50 ohm
5. T-stamp Out 1	TTL, 50 ohm
6. T-stamp Out 2	TTL, 50 ohm
7. Sync Out 1	TTL, 50 ohm
8. Sync Out 2	TTL, 50 ohm
9. CyCLk OUT	TTL, 50 ohm
10. 16-bit digital output	TTL, 50 ohm on P2
11. 8-bit digital input	TTL
12. RS232 port	RS232, RJ11

All of these input and output connections are available on via front panel AND via the rear P2 connector. Front panel connectors for signals 1-9 are LEMO; the front panel connector for the 16-bit digital output port is a header connector (as used for Echotek ECDR 814). The front panel connector for the 8-bit digital input is a standard 10 pin header. A header will control whether the signals come from the front panel or the rear P2. P2 connections will be compatible with SCSI standard as much as possible. The 16-bit digital output on the P2 will have 50 ohm drive.

2. Indicators

The module has the following front panel LED indicators:

Time Stamp Master mode (GRN)
Time Stamp Receiver mode (GRN)
Sync1/T-stamp In NOT present (RED)
SYNC1 In selected (YEL)
SYNC2 NOT present (RED)
Sync2 In selected (YEL)
Internal Clk selected (YEL)
External Clk selected (YEL)
External Clk not present (RED)
TimeStamp not SYNC'd (RED)

3. Time Stamp Master Function

A 64-bit counter holds the T-stamp word. The counter is pre-set and read from the VME backplane. The counter is incremented with the cycle clock (CyClk).

Note:
2^32 = 4.3E9 which, at 4.001Khz = 1.1E6Seconds or 12.5 days
2^64 = 18.45E18 which, at 4001Khz = 4.61E15 Seconds or 53.4E Days or 146E6 Years

CyClk is derived by dividing down the system clock (Clk) by a 16-bit integer factor N (CyClk = Clk/N). N is set and read from the VME backplane. Under normal operation, the system clock frequency is equal the ring revolution frequency (1.28038 MHz), N = 320, and the CyClk frequency = 4.001 kHz.
Clk is selectable from an external source (Clk In) or an internal source by VME command. Under normal operation, the external input is used.

Sync1/T-stamp In and Sync2 In disabled **(??? or should they be used to resync CyClk divider???).**

An 8-bit serial data packet is transmitted synchronously with CyClk from each of the T-stamp Out 1 and T-stamp Out 2 output ports. The data packet bit rate is determined by the transmit/receive UART clock (Tx/Rx Clk).

Time-stamp data packet protocol: see Appendix 1.

Tx/Rx Clk operates at the standard UART rate of 115.2 kbps. This clock rate is derived internally. The leading edge of the time-stamp data packet start bit must have low jitter with respect to CyClk: circuitry is provided to assure that the leading edge of the start bit is synchronous with CyClk.

A sync pulse is transmitted from the Sync Out 1 output port synchronously with CyClk and delayed from the CyClk leading edge by D1 Clk periods, where D1 is a 16-bit integer that is set and read from the VME backplane. Under normal operation, the Clk frequency is equal the ring revolution frequency (1.28038 MHz), N = 320, and D1 < 320. Sync Out 1 can be enabled and disabled under software control via the VME backplane.

A sync pulse is transmitted from the Sync Out 2 output port synchronously with CyClk and delayed from the CyClk leading edge by D2 Clk periods, where D2 is a 16-bit integer that is set and read from the VME backplane. Under normal operation, the Clk frequency is equal the ring revolution frequency (1.28038 MHz), N = 320, and D2 < 320. Sync Out 2 can be enabled and disabled under software control via the VME backplane.

Another counter (SysTimer) incremented with Clk **(or a much higher frequency???)** is used for program execution timing measurements and can be read over VME. The counter is reset to 0 with the leading edge of the time-stamp start bit.

The 16-bit digital output port is programmed via VME and updated synchronously with CyClk.

4. Time Stamp Receiver Function

A 64-bit counter holds the T-stamp word. The counter is loaded with information from a series of Time-Stamp serial data packets received from the Sync1/T-Stamp In input port. The contents of the counter can be read from the VME backplane. The counter is incremented with the leading edge of each received data packet, which is used as an externally generated cycle clock (CyClk).

The internally generated CyClk is disabled.

Time-stamp data packet protocol: see Appendix 1.

The received 8-bit Time-Stamp serial data packet is clocked into a parallel register by the transmit/receive clock (Tx/Rx Clk).

Tx/Rx Clk operates at the standard UART rate of 115.2 kbps. This clock rate is derived internally. The leading edge of the time-stamp data packet start bit must have low jitter with respect to CyClk: circuitry is provided to assure that the leading edge of the start bit is synchronous with CyClk.

Clk is selectable from an external source (Clk In) or an internal source by VME command. Under normal operation, the external input is used and the system clock frequency is equal the ring revolution frequency (1.28038 MHz).

A sync pulse is transmitted from the Sync Out1 and Sync Out2 output ports synchronously with and delayed from either

1. the external CyClk derived from Sync1/T-Stamp In, or
2. from an external sync pulse received from the Sync2 In input port, or
3. from a software-generated sync

The Sync1, Sync2 or software synchronization input source is selected from the VME backplane. Sync Out 1 or Sync Out 2 can be enabled and disabled under software control via the VME backplane.

Sync pulses are one Clk period wide, and are delayed from the leading edge of the selected Sync input source by D1 Clk periods for Sync Out 1, and by D2 Clk periods for Sync Out2, where D1 and D2 are 32-bit integers that are set and read from the VME backplane. Under normal operation, the Clk frequency is equal the ring revolution frequency (1.28038 MHz) and D1 and D2 are < 320.

Under normal operation, the Sync1/T-stamp input would be used to generate synchronizing output pulses at the CyClk rate (4.001 kHz) for stored beam orbit processors and other orbit control components. The Sync2 input would receive a 10 Hz beam injection trigger and would be used to generate synchronizing output pulses at the beam injection rate for 1st-turn(s) orbit processors and other orbit control components.

Another counter (SysTimer) incremented with Clk **(or a much higher frequency???)** is used for program execution timing measurements and can be read over VME. The counter is reset to 0 with the leading edge of the time-stamp start bit.

The 16-bit digital output port is programmed via VME and updated synchronously with CyClk.

VME SysReset – Does not effect the MASTER. Only the SLAVE is reset on SysReset.

VME Interface
The TSSM is an A24 D32 slave with RORA (Release on Register Access) interrupt capabilities.

VME Interrupts:
VME Interrupts can be generated by any of 9 sources. These sources can be enabled or disabled in the INTEN register. The leading edge of these signals is detected and produces an interrupt. The INTPEND register will indicate which input is causing the interrupt. The interrupt can only be cleared by writing the appropriate bit in the INTPEND register.

Master:
In the Master mode, interrupts are generated by either the SYNC pulse or one or more of the Digital Input lines. The Source of the SYNC pulse is selected by setting the appropriate bits in the SYNC_SOURCE field in the CSR register.

Slave:
In the Slave mode, interrupts are generated by either the SYNC pulse or one or more of the Control bits received with the TimeStamp.