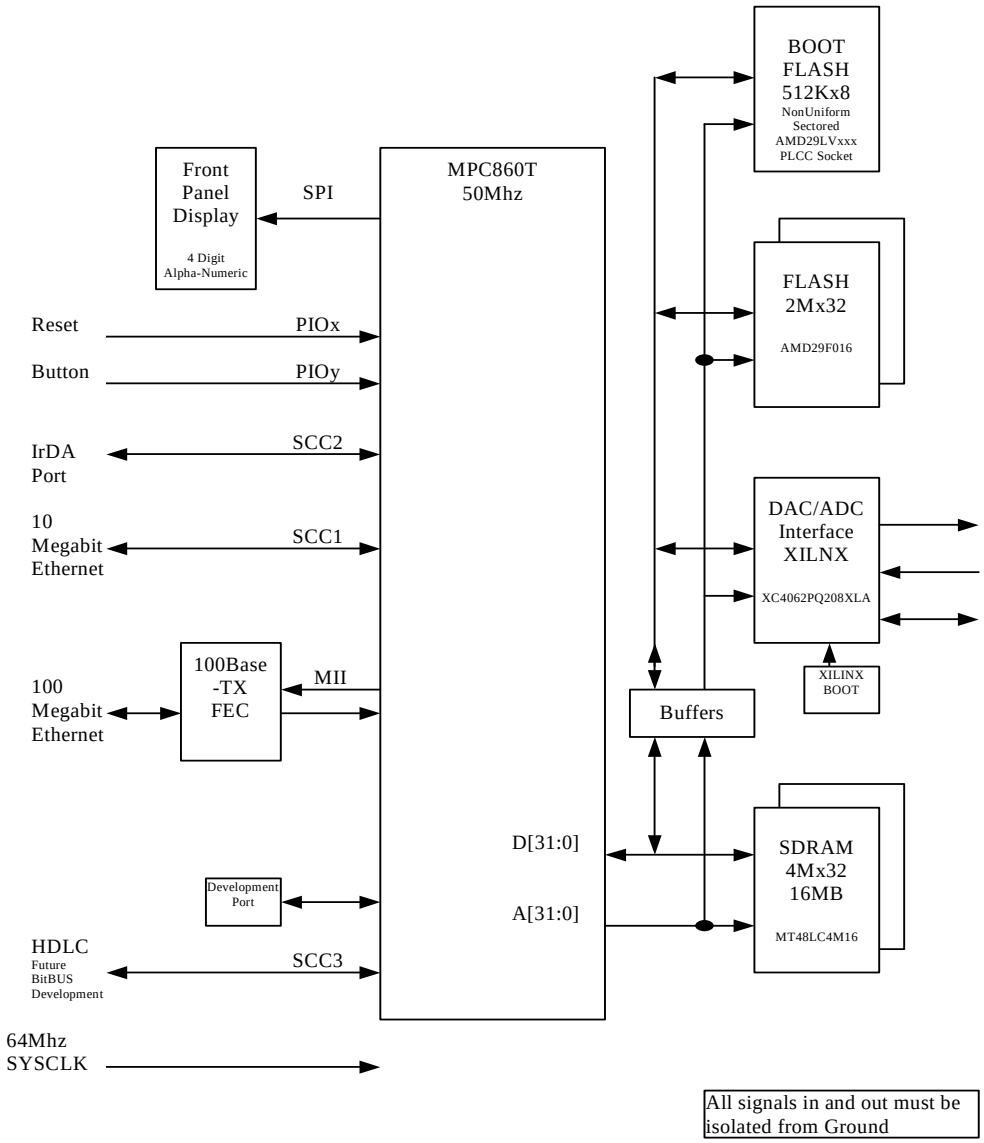
The SPEAR 3 MCOR Controller is an 8 channel, 30A Magnet Corrector Controller. It is designed to fit into the existing MCOR Analog backplane.

SPEAR 3 - 8 Channel MCOR Controller
Block Diagram of Digital Section



1 BOOT Flash

1. 512Kx8 socketed plcc.
2. Contains the code to configure the memory and I/0 devices.
3. Could contain the default code for the controller.
4. Can only be programmed externally.
5. Controlled by General-Purpose Chip-select Machine (GPCM) and CS0

2 System Flash Memory

1. 2Mx32
2. Downloadable from Ethernet
3. Controlled by General-Purpose Chip-select Machine (GPCM) and CS1

3 SDRAM

1. 4Mx32 Synchronous DRAM
2. Controlled by User Programable Machine B (UPMB) and CS4

4 XILINX

1. 256x32 Registers available.
2. XC4000XLA series FPGA. Actual part size to be determined.
3. Controls Serial to Parallel conversion to DAC's.
4. Controls Serial to Parallel conversion from ADC's.
5. Controls Multiplexors and other control functions in the Analog section.
6. Possibly perform PID filter algorithm.
7. Provide board status register readable by MPC860.
8. Controlled by GPCM and CS2 .
9. Boot from JTAG's XILINX Serial PROM. Re-programmable from MPC860.

5 **Front Panel Display**

1. Infineon 4 Character Alpha-Numeric display
2. Programmable from MPC860 via the Serial Peripheral Interface (SPI).

6 IR Port

1. IR Port for diagnostics
2. Controlled by Serial Management Channel 1 (SCC2).

7 10Base-Tx Port

1. 10 Mbit Ethernet Port for auxillary data and control transfers
2. Controlled by Serial Communication Controller 1 (SCC1).

8 100Base-Tx Port

1. 100 Mbit Ethernet Port for Set Point transfer and control
2. Controlled by MII Fast Ethernet Interface

9 Parts count and cost (not a complete list of all parts)

Part Number	Manufacturer	Description	Quantity	Unit Price	Total
MPC855T	Motorola	Motorola PowerPC	1	70	70
MPC860T	Motorola	Motorola PowerPC	1	170	170
AM29F016D	AMD	16Mbit (2Mx8) Flash	4	30	120
AM29F040	AMD	4Mbit (512x8) Flash	1	6	6
MT48LC4M16	Micron	4Mx16 SDRAM	2	20	40
LXT970A	LevelOne	100M Ethernet MII	1	10	10
XC4062XLA	XILINX	4000 Series FPGA	1	200	200
SCDV5540	Infineon	4 Character display	1	10	10
TFDS6000	Vishay	IrDA Transiever	1	6	6

Port A

Port A				
Signal	Function	Use	PAPAR	PADIR
PA15	RXD1	Receive DATA IN for 10Base-T (SCC1)	1	0
PA14	TXD1	Transmit DATA OUT for 10Base-T (SCC1)	1	0
PA13	RXD2	Receive DATA IN for IrDA (SCC2)	1	0
PA12	TXD2	Transmit DATA OUT for IrDA (SCC2)	1	0
PA11				
PA10				
PA9	SD/MD	Shutdown/Mode for IrDA	0	
PA8				
PA7	CLK1	Transmit CLOCK in from 10Base-T (SCC1)	1	0
PA6	CLK2	Receive CLOCK in from 10Base-T (SCC1)	1	0
PA5				
PA4				
PA3				
PA2				
PA1				
PA0				

Port B

Port B					
Signal	Function	Use	PBPAR	PBDIR	PBODR
PB31					
PB30	SPICLK	Serial CLOCK OUT to SPI Display (SPI)	1	1	0
PB29	SPIMOSI	Serial DATA OUT to SPI Display (SPI)	1	1	0
PB28	/SPILD	Load Strobe for the SPI Display	0		0
PB27					
PB26					
PB25					
PB24	X_CCLK	CCLK to XILINX	0		0
PB23	X_DIN	DIN to XILINX	0		0
PB22	/X_INIT	INIT to XILINX	0		1
PB21	X_DONE	DONE from XILINX	0		1
PB20	/X_PGM	PGM to XILINX	0		1
PB19	/RTS1	TX_EN for 10Base-T (SCC1)	1	1	0
PB18					
PB17					
PB16					
PB15					
PB14					

Port C

Port C					
Signal	Function	Use	PCPAR	PCDIR	PCS0
PC15					
PC14					
PC13					
PC12					
PC11	/CTS1	Collision for 10Base-T (SCC1)	0	0	1
PC10	/CD1	RX_EN for 10Base-T (SCC1)	0	0	1
PC9					
PC8					
PC7					
PC6					
PC5					
PC4					