

APPENDIX IV

ON-LINE COMPUTER SYSTEM FOR THE SPECTROMETER FACILITY

A. Boyarski, SLAC Group C

A powerful computer and interface system will be used with the spectrometers for doing on-line experiments. The computer will read the data from various detectors into core memory, storing this data on magnetic tape in compressed form, and doing preliminary calculations on the data. Various checks for proper operation of equipment can readily be performed by the computer. Accurate alignment checks of the spectrometer, and magnet current control will be done by the computer. An oscilloscope display system will allow rapid presentation of accumulating data so that, to some extent, on-line decisions can be made on the operation of the experiment.

The computer, an SDS 9300, has the following properties:

1. 24 bit word length.
2. 1.75 μ sec cycle time.
3. 16 K memory, to be expanded to 32 K within the next few months.
4. Hardware floating point with 39 bit mantissa and 9 bit exponent, allowing for up to twelve significant decimal digits.
5. A repertoire of over 100 instructions with a complete set of shifting and bit manipulation instructions.
6. 32 levels of priority interrupt.
7. 32 sense lines.
8. 24 parallel input lines (PIN) for transferring data into the computer.
9. 24 parallel output lines (POT) for transferring data out of the computer.
10. 15 lines are provided to the user for selecting up to 2^{15} different devices. These lines are activated by an "energize output from memory" (EOM) instruction.
11. 2 data channels which can transfer blocks of data from core memory to peripheral devices, simultaneous with computation.

The 9300 computer is slightly faster than an IBM 7090, but has a smaller word size (24 bits instead of 36) and a smaller instruction repertoire. Floating point precision is better than the 7090 single precision arithmetic. An extensive line of software is available in the form of FORTRAN IV, META SYMBOL -

a machine language symbolic code assembler, and a monitor which enables loading and executing a job with any mixture of FORTRAN, META SYMBOL or BINARY programs. A real time FORTRAN IV, necessary when interrupts are used, will soon be available from SDS. The 9300 operation can be considered almost as powerful as the 7090 class of computers, but the flexible priority interrupt hardware makes it better suited to on-line computation.

Peripheral devices connected to the computer include:

1. A 10 character/sec typewriter.
2. A 600 line/min lineprinter.
3. A 400 card/min card reader.
4. A 100 card/min card punch.
5. Two magnetic tape recorders (IBM 729 compatible at 200 or 556 characters/inch).
6. An XY plotter 10"× 10", 0.01" increments at 100/sec.
7. A 17" oscilloscope display system with vector and character generator and lightpen.
8. A rapid access disk file.

Interface to the 9300

The interface between the 9300 computer and the various pieces of experimental equipment can be divided into four major functions, namely the decoder for the device selection corresponding to an address word, input devices connected to the PIN lines, output devices at the POT lines, and the interrupt lines to the computer. These functions are blocked off in Fig. 1. In addition, there is a data link to the Beam Switchyard SDS 925 computer.

Decoding Logic

The decoding logic translates or decodes the information appearing on 15 EOM BUFFER flip-flops set by the computer into a signal onto one out of many select lines connected to the various pieces of equipment. Three of the EOM lines are used for specifying the type of input/output transfer that is to occur, namely the transfer can occur: a) with or without a binary to decimal conversion for output data; b) with or without a decimal to binary conversion for input data; c) with or without a reset to the device after the data is transferred; and d) special tests such as setting a flag flip-flop if the selected device is not ready. Another set of three EOM lines are used to channel or multiplex (MPX) the remaining nine lines to eight possible sub-decoding logic blocks, each capable of providing unique select lines to $\leq 2^9$ devices.

One of these sub-decoding blocks further subdivides the 9 lines into 4 + 5 lines, where 4 lines are used to provide 16 channels or GROUP DECODE lines with each channel having $\leq 2^5$ or 32 devices. Selection of the latter 32 devices within a given group is done by the DEVICE DECODE logic block, as shown in several places in Fig. 1.

In practice, several device decoders will be spaced throughout the counting house together with the input (or output) multiplexers which multiplex the 24 data lines from the devices to a common bus line. This will adequately accept most data logging inputs such as scalers, pulse height analyzers, etc., where no more than 32 devices normally occur within a local area of the counting house. Other devices such as digital voltmeters (DVM) may have hundreds of inputs, and here the 9 bit decoder can be used to select any input (out of $\leq 2^9$) to the DVM, while the normal group decoder can later select the DVM to the computer.

Input Devices

At the present time, the possible input devices to the computer from all three spectrometers consist of:

- 264 discriminator-coincidence-buffer (DCB) units
- 8 pulse height analyzers (128 channel)
- 1 4096 two-dimensional pulse height analyzer
- 20 fast (100 Mc/sec) scalers
- 48 flag flip-flops
- 24 manual status switches
- 10 thumbwheel switches
- 12 shaft encoders
- 4 digital voltmeters
- 1 time of day clock

The interface is being designed to accept all of these inputs, with considerable expansion capability.

Normally, several of these devices will be grouped into a local multiplexer (MPX) with 24 parallel line drivers to a common 24 line bus. This bus line extends throughout the counting house and feeds into the PIN BUFFER. Hence any device selected by the decoding logic will present its data to the pin buffer, which can then be read by the computer either directly or through the BCD \rightarrow BIN converter. In addition to the 24 data lines, a DEVICE READY line and a RESET line to the device are similarly multiplexed to all devices to allow flexibility for devices which require ready tests or resets.

Output Devices

At the present time, devices which accept data from the computer are the controls to the magnet power supplies, interval timers and nixie tube displays. Eventually it is likely that the computer may control more of the experiment, in which case more output devices will appear. For example, light pulsers for selected phototubes may be energized to provide on-line checking of the phototubes and electronics.

A 24 line output from the computer is transferred to the POT BUFFER either directly or through the BIN \rightarrow BCD converter. The contents of this buffer is channelled to the device as specified by the decoding logic.

Interrupt Input

Each of the 32 priority levels of interrupt can be energized either by a pulse from some device or manually by an operator. A patch panel will be provided to readily select the desired priority level for any device. The status of each interrupt will be revealed by two indicator lights, one which displays whether the interrupt line is armed (or ready to accept pulses) and another which displays the waiting state (i. e. , a pulse has energized an interrupt but a higher level interrupt is still in process).

The sequence of operation for reading in data from a device is as follows: When the device is ready to transfer data, an interrupt is sent to the computer. When the computer is able to acknowledge the interrupt, a program is entered which executes the instructions:

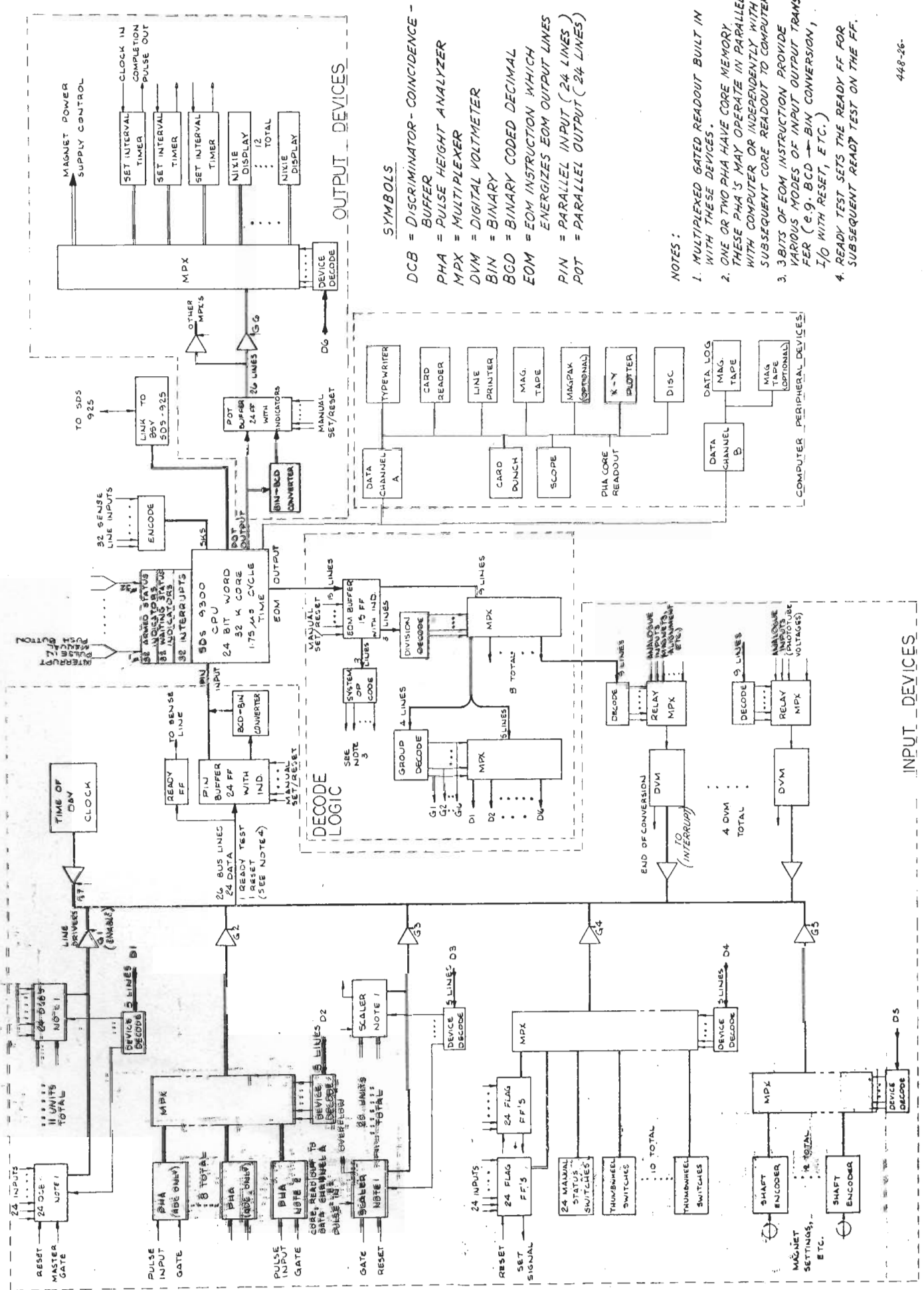
EOM A

PIN B

The EOM A instruction places the address A on the EOM lines. The decoding logic energizes one and only one select line corresponding to the address A. This line must be connected to the device that originally provided the interrupt. Thus, the contents of the selected device are gated onto the 24 bus lines and into the PIN BUFFER register. The next instruction, PIN B, reads the contents of the pin buffer into core memory location B. Having completed the data transfer to memory, the computer would then proceed to do any lower level priority interrupts which may be waiting to be acknowledged.

Control Panel

A control panel will display the PIN BUFFER, the POT BUFFER and the EOM BUFFER. A manual mode will enable an operator to manually insert any input into these buffers for purposes of checking out programs when devices are not connected to the interface, or for checking proper connections between the device and the computer. The control panel will also contain all the interrupt push buttons and indicators.



SYMBOLS

- DCB = DISCRIMINATOR - COINCIDENCE -
- PHA = PULSE HEIGHT ANALYZER
- MPX = MULTIPLEXER
- DVM = DIGITAL VOLTMETER
- BIN = BINARY
- BCD = BINARY CODED DECIMAL
- EOM = EOM INSTRUCTION WHICH ENERGIZES EOM OUTPUT LINES
- PIN = PARALLEL INPUT (24 LINES)
- POT = POTENTIAL INPUT (24 LINES)

NOTES :

1. MULTIPLEXED GATED READOUT BUILT IN WITH THESE DEVICES.
2. ONE OR TWO PHA HAVE CORE MEMORY. THESE PHA'S MAY OPERATE IN PARALLEL WITH COMPUTER OR INDEPENDENTLY WITH SUBSEQUENT CORE READOUT TO COMPUTER.
3. 3 BITS OF EOM INSTRUCTION PROVIDE VARIOUS MODES OF INPUT OUTPUT TRANSFER (E.G. BCD → BIN CONVERSION, I/O WITH RESET, ETC.)
4. READY TEST SETS THE READY FF FOR SUBSEQUENT READY TEST ON THE FF.

FIG. 1 -- COMPUTER SYSTEM AND INTERFACE FOR SPECTROMETER FACILITY