Development of Monolithic Active Pixel Sensors
in a 0.13 μm Triple Well
CMOS Technology with
In-Pixel Full Analog Signal Processor

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On behalf of the SLIM5 Collaboration

Outline

- Introduction: standard MAPS for vertex detectors in HEP
- The new features of our MAPS:
  - deep n-well collecting electrode
  - signal processing at pixel level
- The characterization of the 1st prototype "Apsel0":
  - Front-End Electronics
  - Sensor response to:
    - soft X-rays from ^{55}Fe
    - β-rays from ^{90}Sr/^{90}Y
- 2nd prototype "Apsel1":
  - FEE improvements
  - Single channel response to ionizing radiation
  - Test on the matrix
- Next submission: "Apsel2"
- Conclusions

Conventional CMOS MAPS

- Several reasons make them very appealing as tracking devices :

  - detector & readout on the same substrate

  - wafer can be thinned down to few tens of μm

  - radiation hardness (oxide ~nm thick)

  - high functional density and versatility

  - low power consumption and fabrication costs

Principle of standard operation:

- The undepleted epitaxial layer acts as a potential well for electrons moving by diffusion
- Signal (~1000 e-) collected by the n-well/p-epi diode
- Charge-to-voltage conversion provided by the sensor capacitance
  → small collecting electrode
- Extremely simple in-pixel readout (3T NMOS, PMOS not allowed)
  → sequential readout

V_{DD}

RESET M1

M2

M3

SELECT

electronics and interconnects

n+   p+

p−   epitaxial layer (about 10 μm thick)

p++

substrate (about 300 μm thick)

M.I.P.:80 e-h pairs /μm
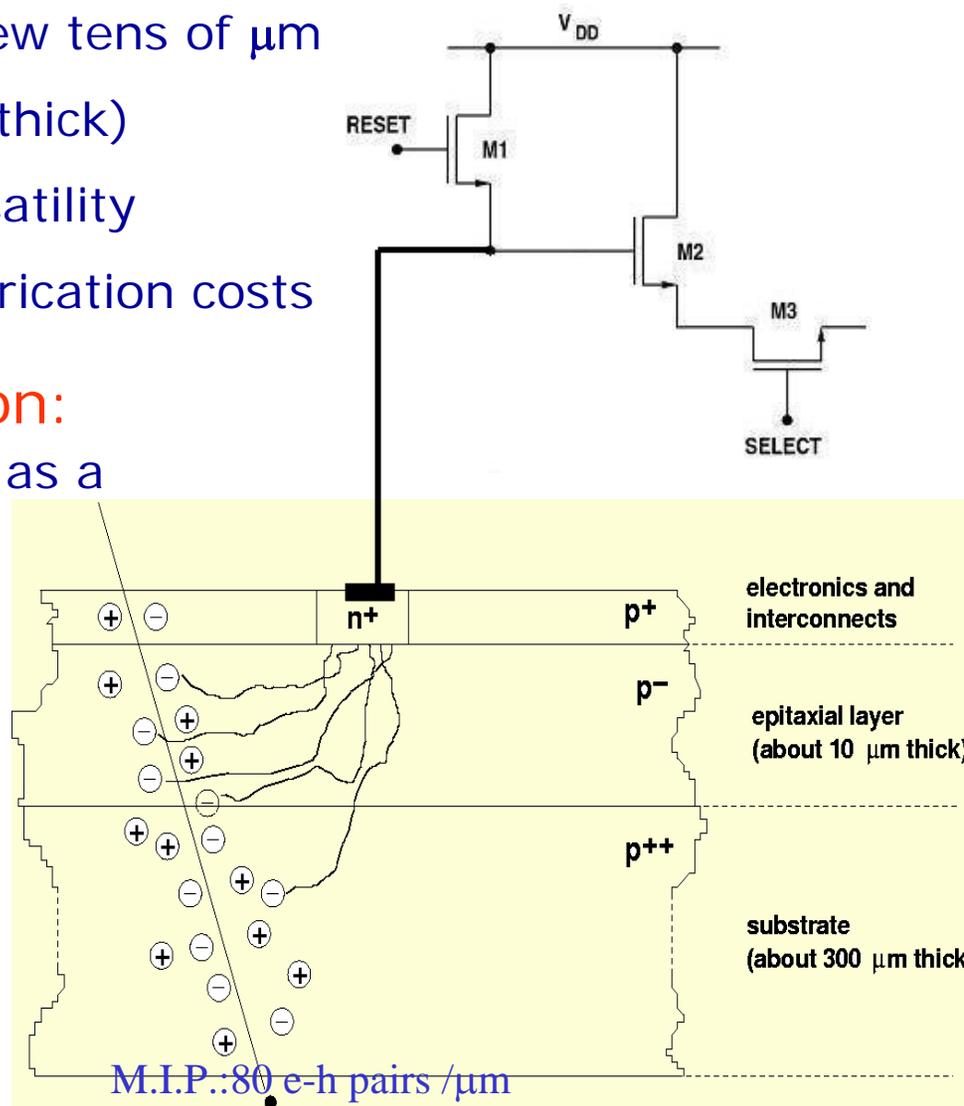
Triple well CMOS process

• In triple-well CMOS processes a deep n-well is used as a shielding frame against disturbancies from the substrate to provide N-channel MOSFETs with better insulation from digital noise
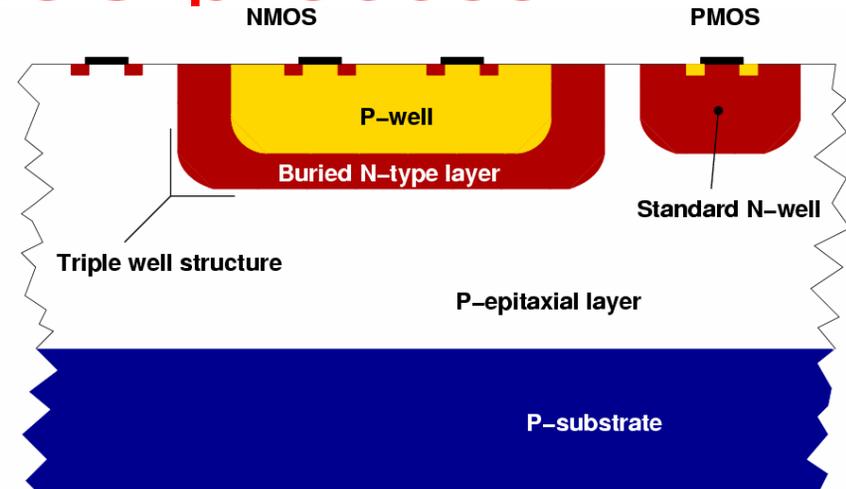
The new design features of our CMOS pixels:

- The deep n-well can be used as the collecting electrode*

- NMOSFETs can be integrated both in the epitaxial layer or in the nested p-well. p-channel MOSFETs are integrated in standard n-wells

- A full signal processing circuit can be implemented at the pixel level overlaying the NMOS transistors on the collecting electrode

* Use of the deep n-well was proposed by Turchetta et al. (*2004 IEEE NSS Conference Record*, N28-1) to address radiation hardness issues

Deep n-well sensor concept (I)

Standard signal processing chain for capacitive detector (i.e. hybrid-pixel-like) implemented at pixel level:
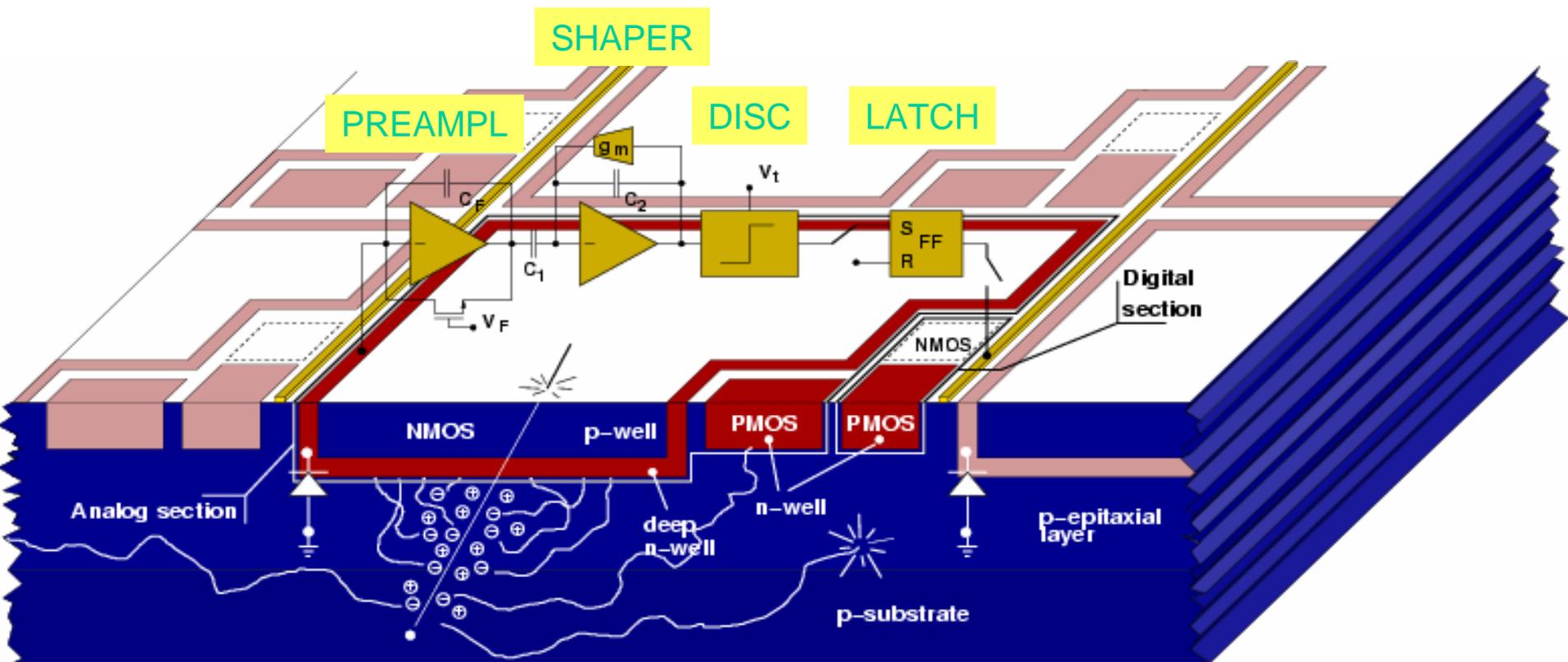
- Charge-to-Voltage conversion done by the charge preamplifier

- The collecting electrode can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance)

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Deep n-well sensor concept (II)

- NMOS devices of the analog section built over the deep n-well

- Included complementary devices needed for CMOS design

- Fill factor ≡ Area(deep n-well)/Area (total n-wells) (≥ 0.85 in the prototype test structures)

- The readout scheme well fits into already existent architectures for data sparsification at the pixel level to improve readout speed

DEEP N-WELL

N-WELL

N-WELL

PMOS analog section

PMOS digital section

NMOS analog section (including input device) + collecting electrode

NMOS digital section

Shaper feedback MiM cap.

Shaper input MiM cap.

~43 µm

~43 µm

Pixel cell layout
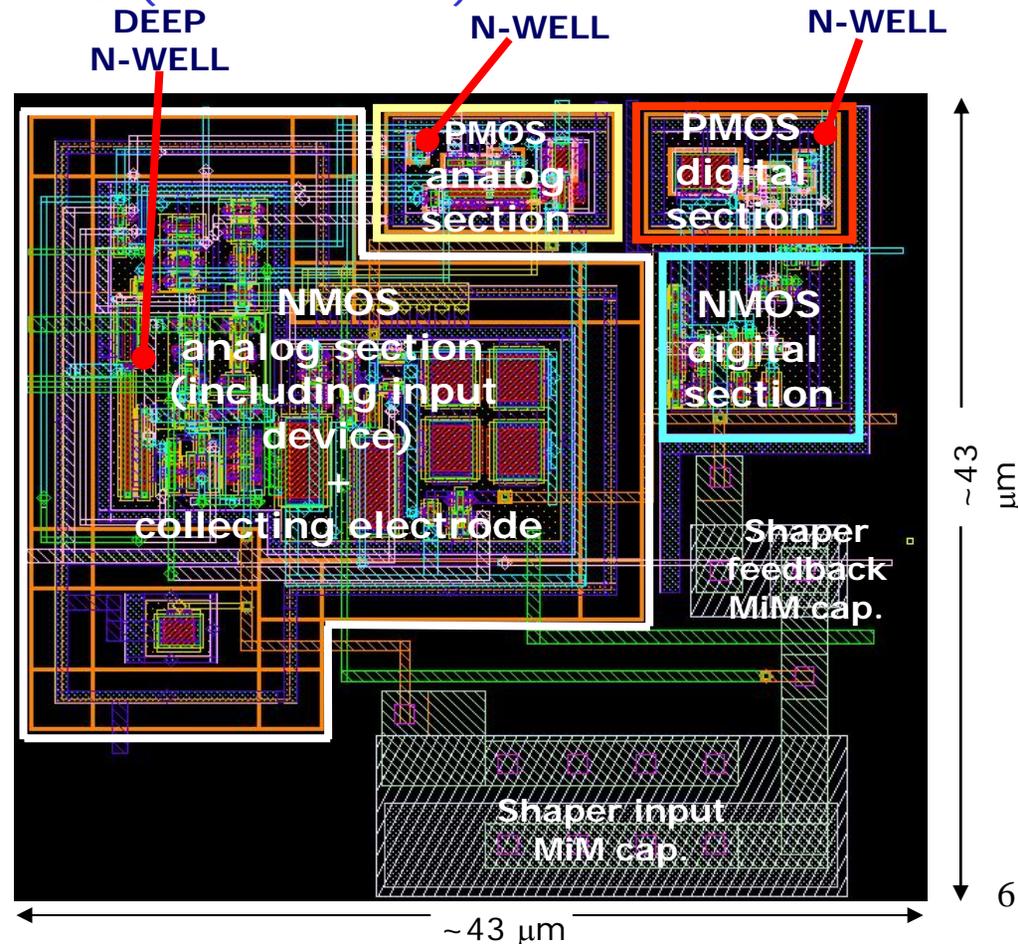
1st Test Chip Layout: apsel0

0.13 μm CMOS HCMOS9GP by STMicroelectronics: epitaxial, triple well process (available through CMP, Circuits Multi-Projets)

channel 5 - pixel with input pad for charge injection ($830\ \mu m^2$ collecting electrode area)

channel 6 - pixel with **small** ($830\ \mu m^2$) collecting electrode area

channel 3- pixel with **medium** ($1730\ \mu m^2$) collecting electrode area

channel 4 - pixel with **large** ($2670\ \mu m^2$) collecting electrode area

channel 1 - pixel with input pad for charge injection

channel 2 - pixel with input pad for charge injection (100 fF detector simulating capacitance)

Ch. 1-2-5 have integrated injection capacitance for readout electronics characterization

Pixel level charge processor
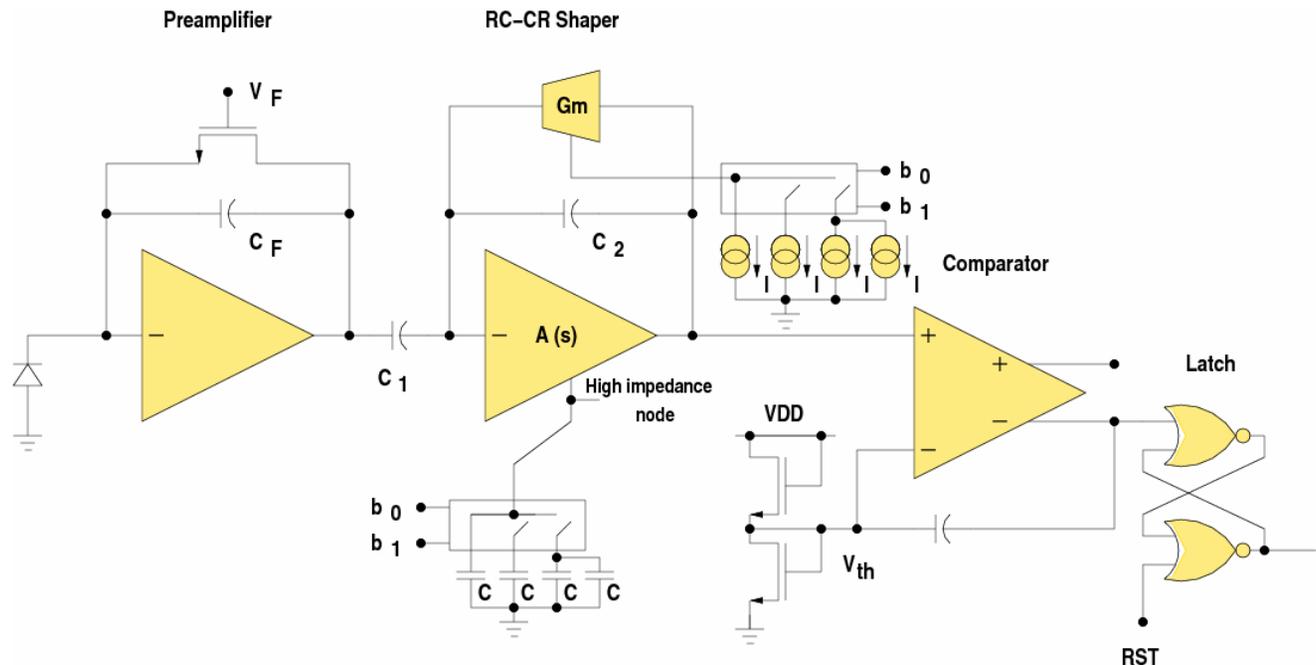
- High sensitivity charge preamplifier with continuous charge reset (n-well/p-epi diode leakage current)

- The preamplifier input provides the bias to the deep n-well (0.3 V)

- Input device (W/L=3/0.35) optimized for a 100 fF detector capacitance and operated at a drain current of about 1 μA

- RC-CR shaper with programmable peaking time: 0.5, 1 and 2 μs. Conservatively chosen to avoid ballistic deficit

- A threshold discriminator is used to drive a NOR latch featuring an external reset

- Power consumption: 10 μW

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Front-End Electronics Characterization

Channel 1
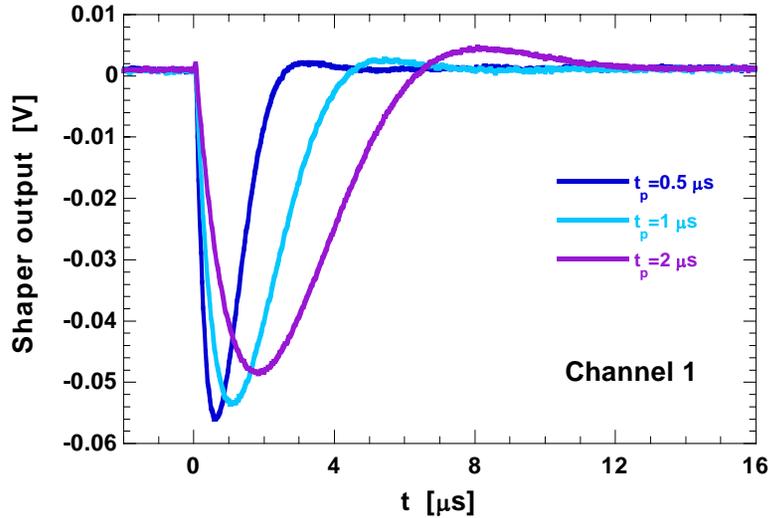
- Shaper response to a 560 e⁻ input charge at the three different peaking times

- About 15% variation in peak amplitude moving from the shortest to the longest peaking time

Channel 2

- Slight overshoot probably due to residual parasitic coupling between preamplifier input and shaper output

- The latch preserves the signal until it has been retrieved

- External reset signal sent to the latch returns it to the initial condition
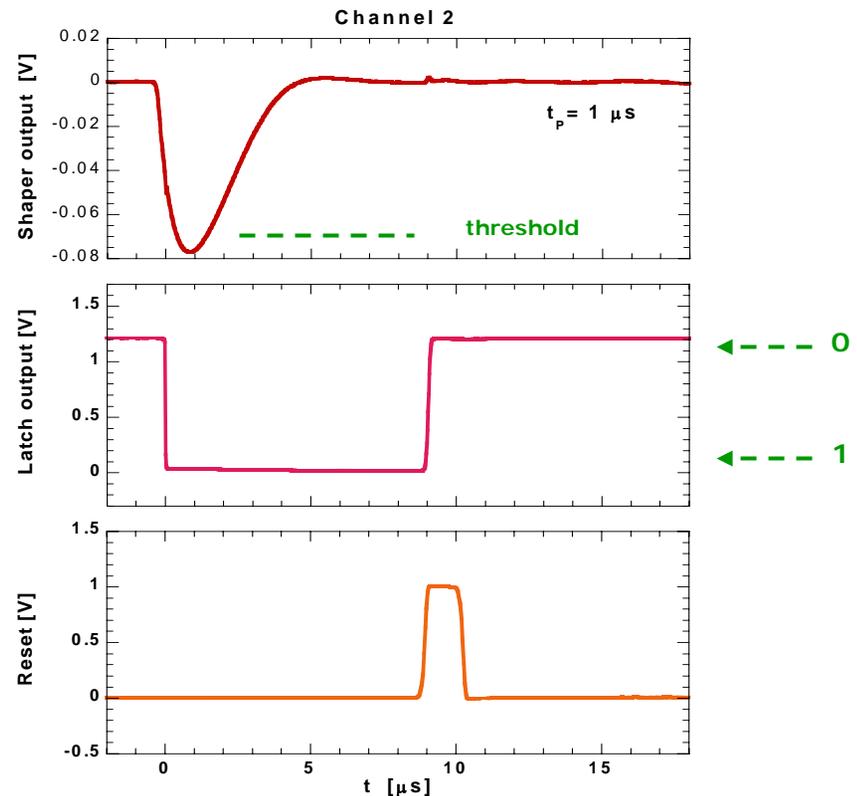
Gain & Noise Measurements

- Charge sensitivity and Equivalent Noise Charge measured in the three channels with integrated injection capacitance C_{inj}

- Good agreement (~10%) with the post layout simulation results (PLS)
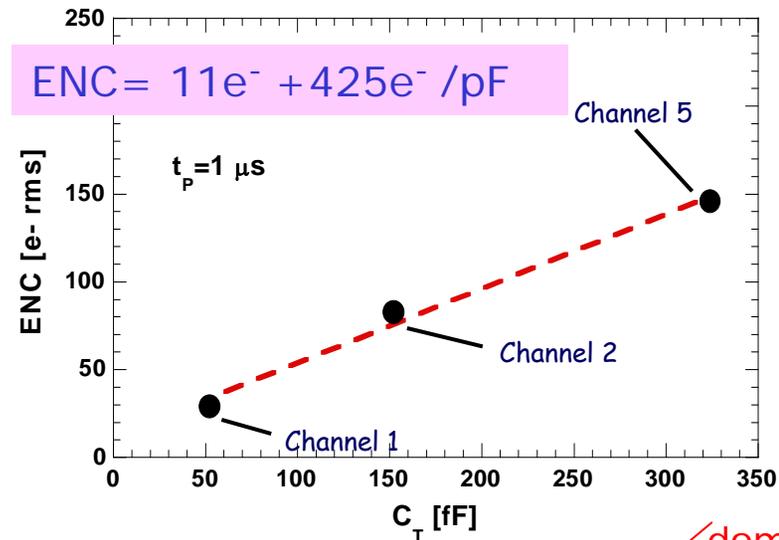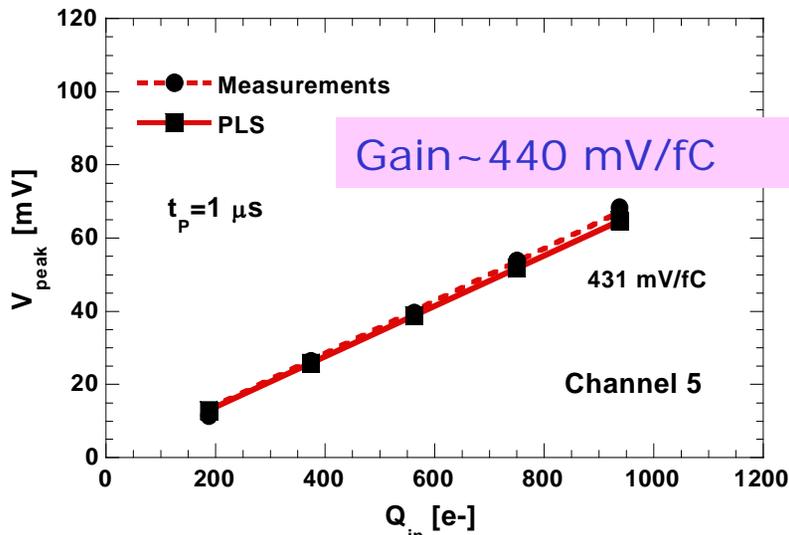
- Equivalent Noise Charge is linear with C_{Tot}

$C_{Tot} = C_D + C_F + C_{inj} + C_{in}$

C_D = detector capacitance(~270fF ch.5, C_D^{MIM}=100fF)

C_F = preamplifier feedback capacitance (8 fF)

C_{inj}= test inj. Capacitance (30 fF)

C_{in} = preamplifier input capacitance (14 fF)

dominant contribution

$$ENC = C_T \sqrt{S_W \frac{A_1}{t_p} + A_2 A_f}$$

S_W=series white noise spectral density

A_f=1/f noise power coeff., A_1, A_2=shaping coeff.

•Sensor capacitance higher than initially expected: noise performance greatly affected. Room for improvement in next chip submission

Calibration with soft X-rays from ^{55}Fe

X-ray from a ^{55}Fe source used to calibrate pixel noise and gain in channels with no inj. capacitance

Peak value of the shaper output:
- blue - ^{55}Fe source (5.9 keV)
- green - no source
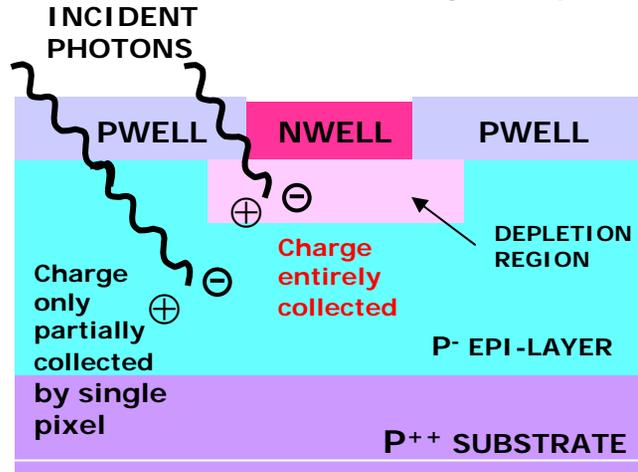
5.9 keV line ≈ 1640 e/h pairs:

• charge entirely collected

→ clear peak @ 105 mV → gain=400 mV/fC

• charge only partially collected → below 100 mV excess of events w.r.t. noise only spectrum

• Calibration with ^{55}Fe source in fair agreement with results obtained both with external pulser tests and with PLS (ENC=140 e-, gain=430 mV/fC expected, 125 e- and 400 mV/fC measured)
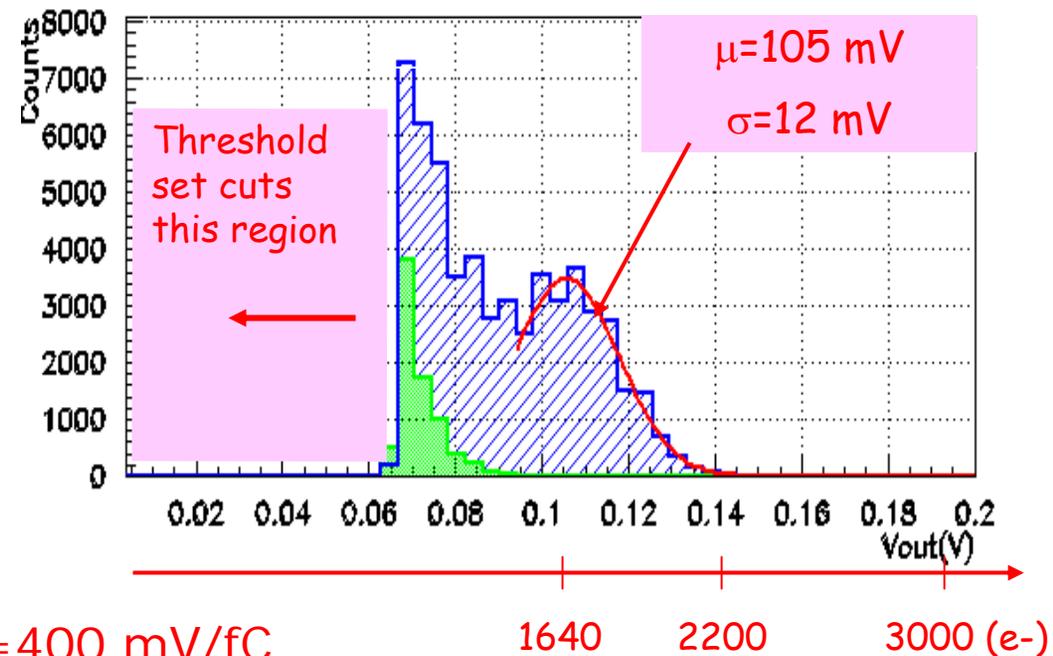
Response to β-ray from a ⁹⁰Sr/⁹⁰Y source

Response to M.I.P from the beta source used to measure S/N ratio

Electrons from ⁹⁰Sr and ⁹⁰Y

15% die in Si

Sr-90 beta spectrum

45% are ~ M.I.P: Landau peak

40% release more than a M.I.P, they deform Landau shape or saturate the shaper
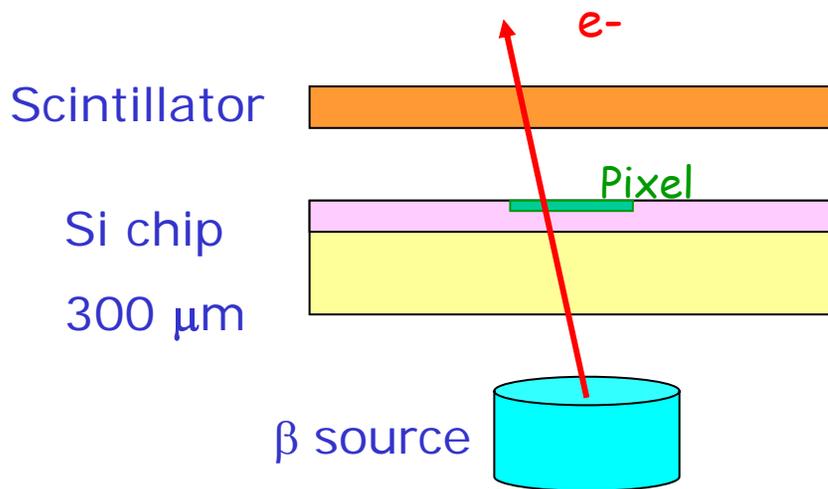
Acquisition triggered by the coincidence (scintillator AND pixel) signal above threshold, set @ ~0.5 MIP
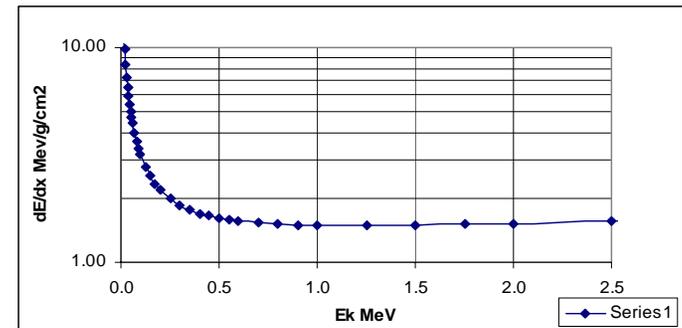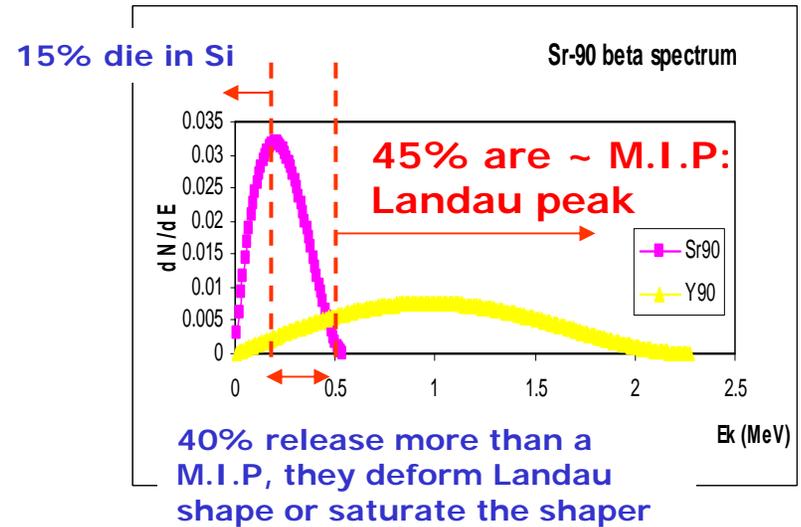
Results from β-ray

- The spectrum clearly shows a Landau peak @80 mV

- Using M.I.P signal and average pixel noise:

  S/N=10

- Using gain measured with ^{55}Fe, M.I.P most probable energy loss corresponds to about 1250 e-

- Fair agreement with sensor simulation: ~1500 e- expected for p-epi layer thickness >15 μm

- Some hint on the process secrets: p-epi layer is thick!

Peak value of the shaper output:
- blue   - with β source
- green - no source

Landau peak 80 mV

saturation due to low energy particle.

Threshold set cuts this region

1250   2200   3000 (e-)

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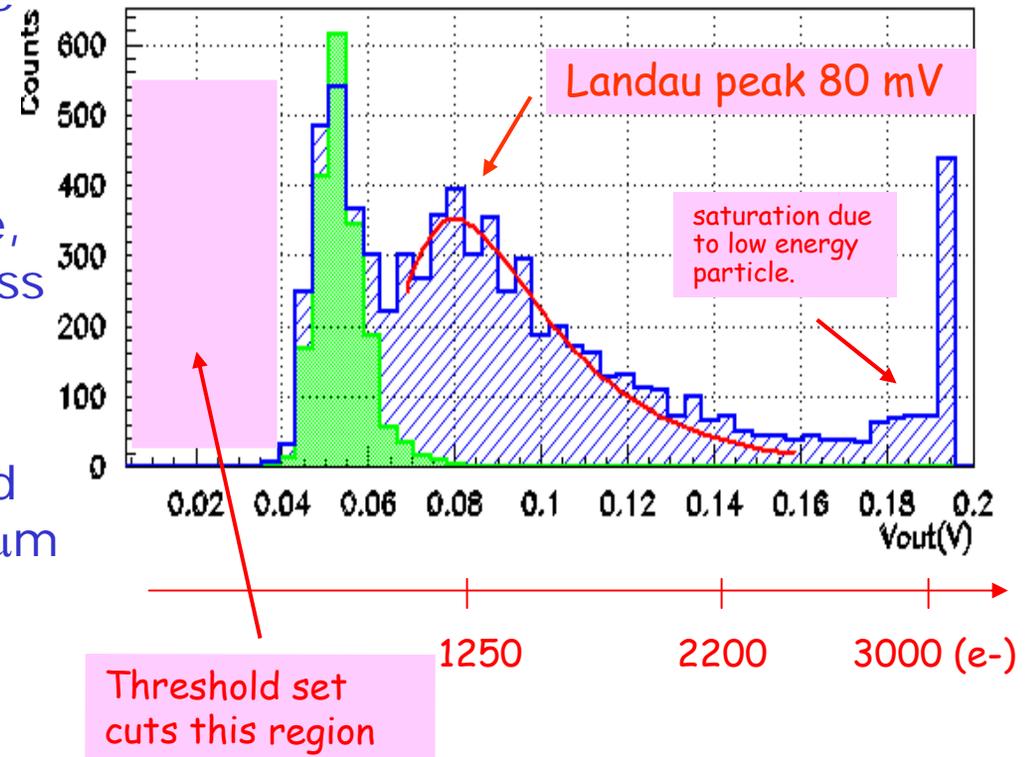
The apsel1 chip

- Submitted August 2005 (delivered Jan.2006)

- Front end modified to address the gain and noise issues (apsel0)

- The chip includes:

-5 single pixel cells(with C_{inj})

    1 standalone readout channel (ROC)

    4 Deep N-Well MAPS with different sensor area

-an 8x8 MAPS matrix (50 μm pitch) with a trigger signal (wired OR of the latch outputs)

8 x 8 matrix + dummies

5 Single pixel test structures

1.2 mm

1.3 mm
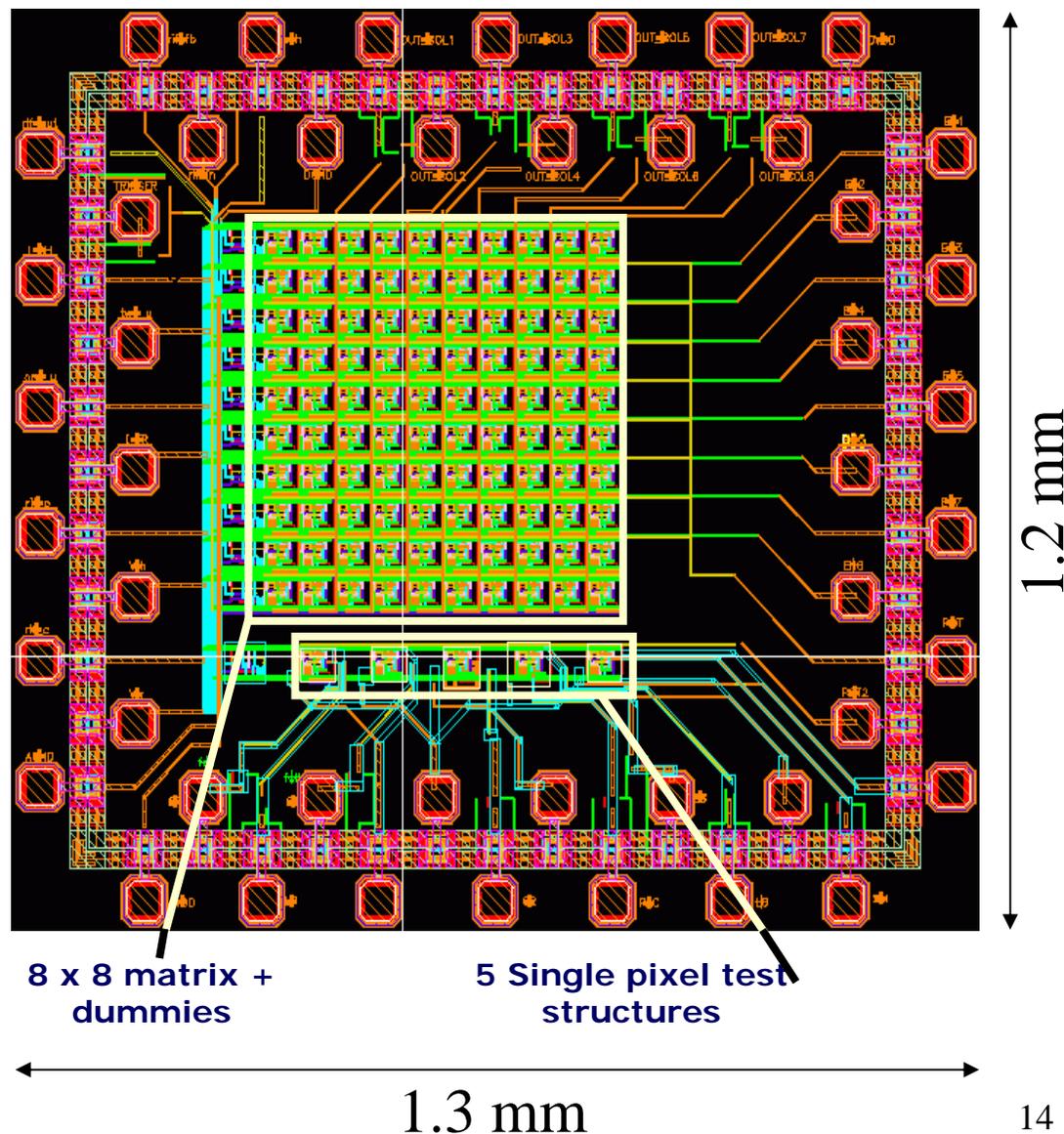
FEE Test Results

The new front-end circuit design solved the gain and noise issues raised by the 1st prototype:

– folded cascode and active load stage implemented in the charge preamplifier

– input element: W/L=16/0.25 (optimized for C_D=320 fF)

– drain current in the input stage: 30 μA (dissipation: P=60 μW/channel)
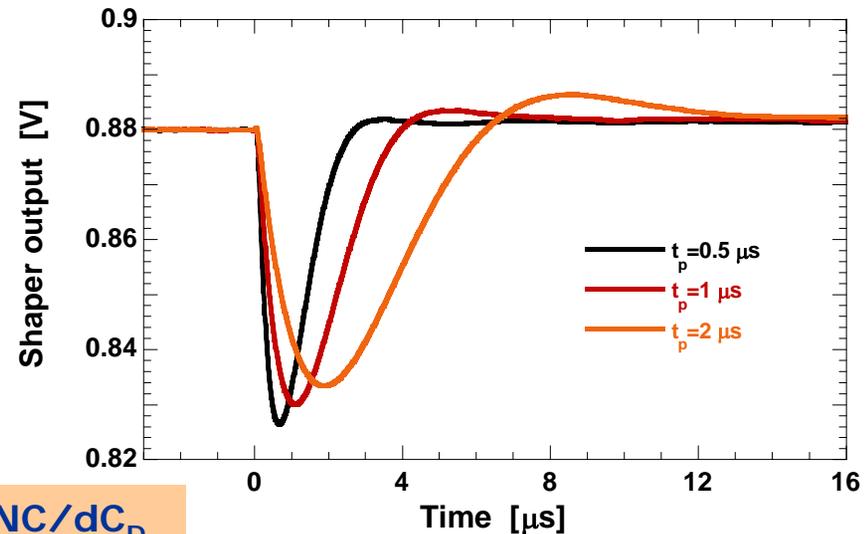
Response to a 750 e⁻ pulse

Peaking time [μs]	ENC [e⁻ rms]	Charge sensitivity [mV/fC]	dENC/dC_D [e⁻/pf]
0.5	41	466	70
1	39	432	68
2	39	406	68

Contributions to ENC
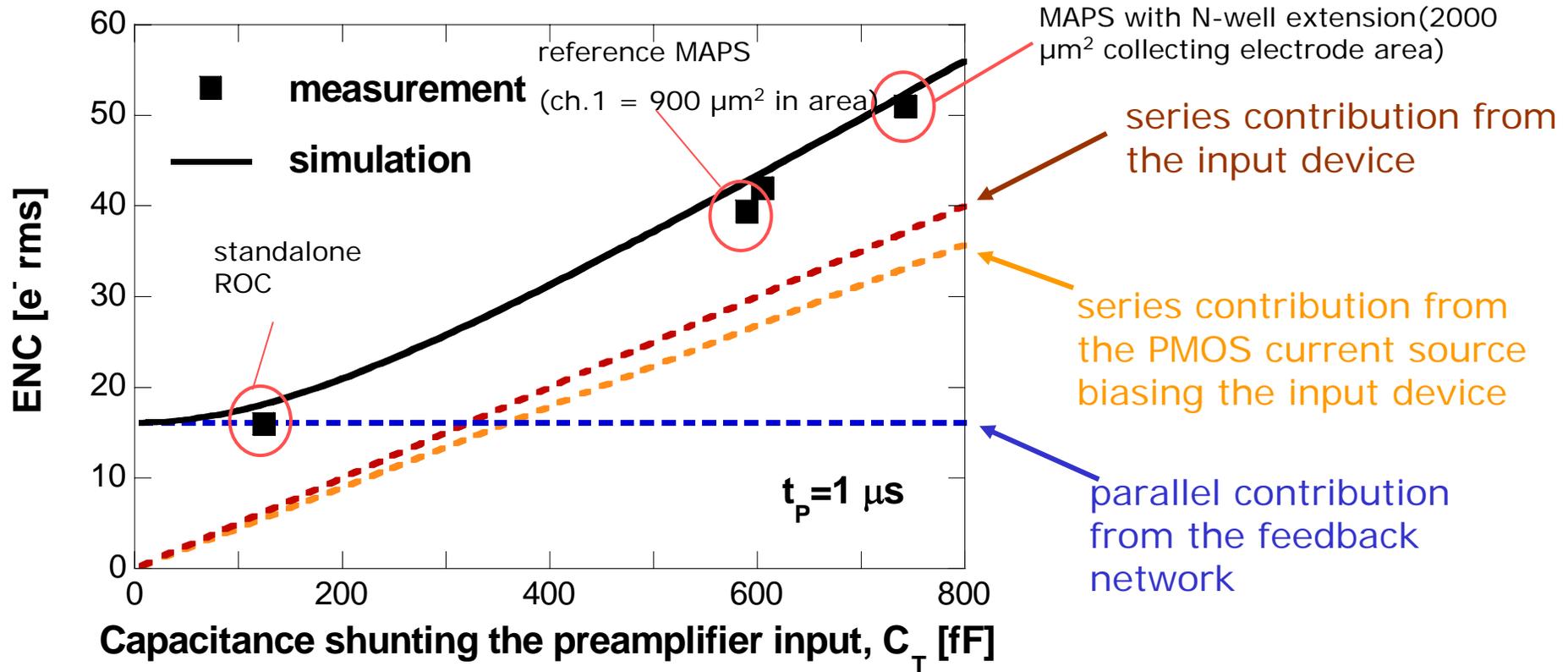
$C_T = C_D + C_{inj} + C_{in} + C_F$
$C_D = 460$ fF for ch.1
$C_{inj} = 60$ fF, $C_{in} = 40$ fF, $C_F = 8$fF

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Single channel response to soft X-rays from Fe^{55}

$$Gain_{Fe^{55}} = \frac{V_{peak}(mV)}{1640 \cdot 1.6 \cdot 10^{-4}\, fC} = 457\,(mV/fC)$$

μ=120 mV
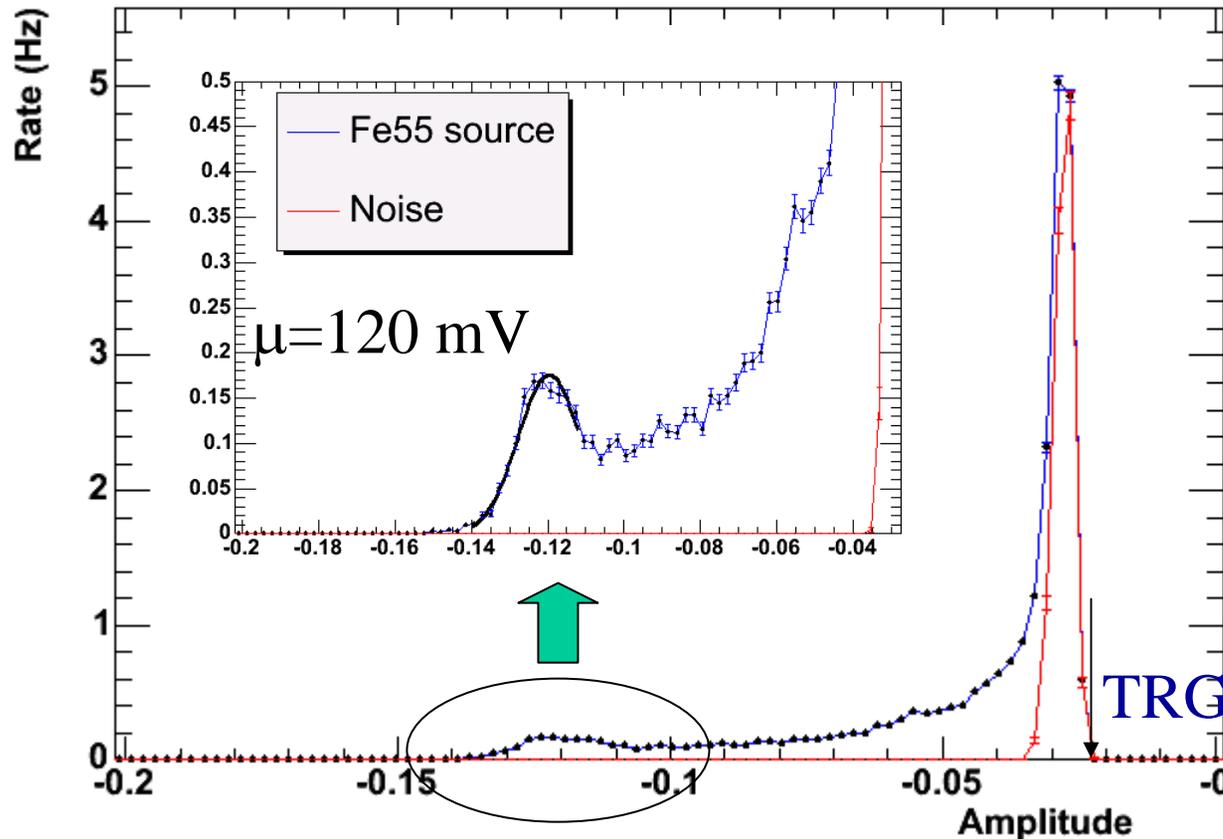
The events on the right of the peak are due to charge partially collected.

$$\frac{S}{N} = 30$$

Fe^{55} : 5.9 keV

TRG cut=20 mV

(Volt)

Single channel response to β

- Observed a clear signal

- Continuous spectrum of collected Energy!

- WHY "**Landau**" NOT VISIBLE?

- Two effects conspires:
  - **Released Energy**: (from Geant4 simulations) the released energy strongly depends (through multiple scattering) on the amount of material supporting the die. Mechanical differences (apsel1,apsel0) in the assemblies may obscure the peak.
  - **Collected Energy**: efficiency not uniform, contribution from a broad region outside the collecting electrode.

Spectrum (pixel in coinc.with scint.)

collecting electrode

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Geant simulation (β-rays): basic geometry

Pixel:
30x30x15(μm)

Si bulk
1x2x0.3(mm)

2 cm

Source

path
length (μm)

Q released (e-)

Q Released in the active region (e-)
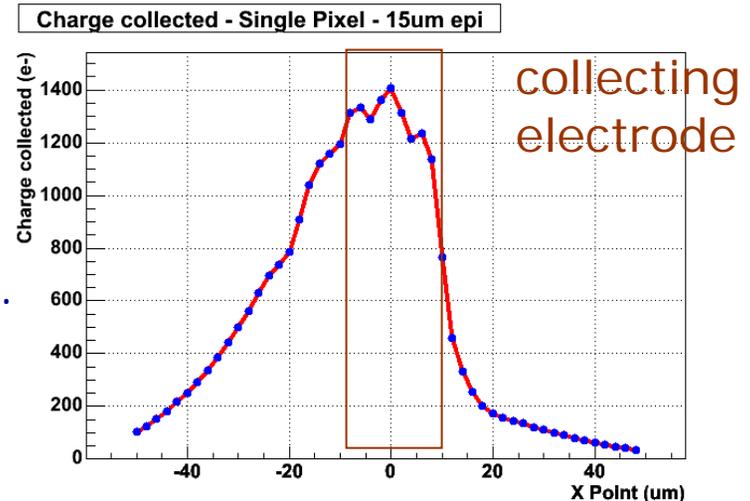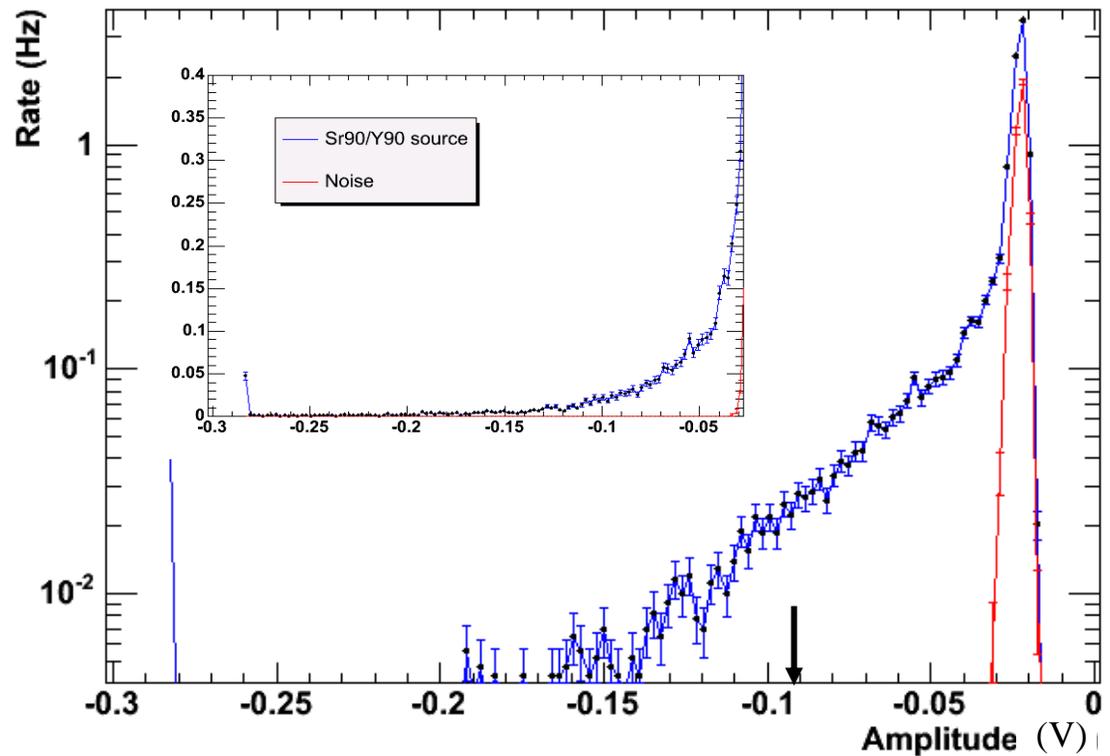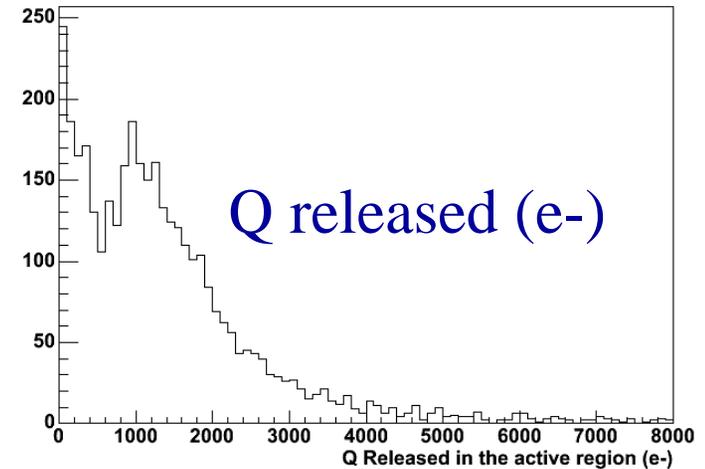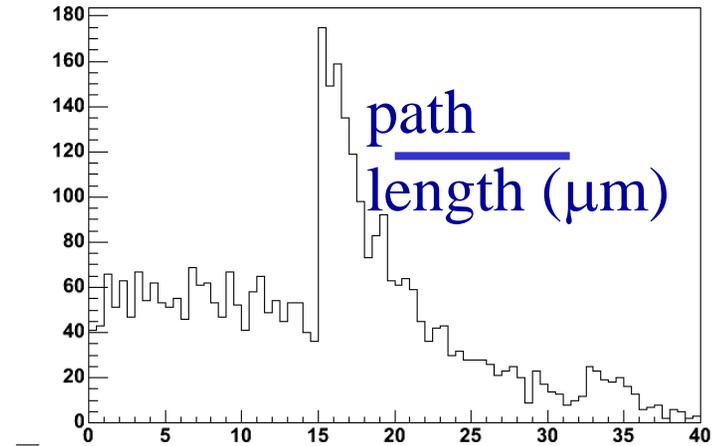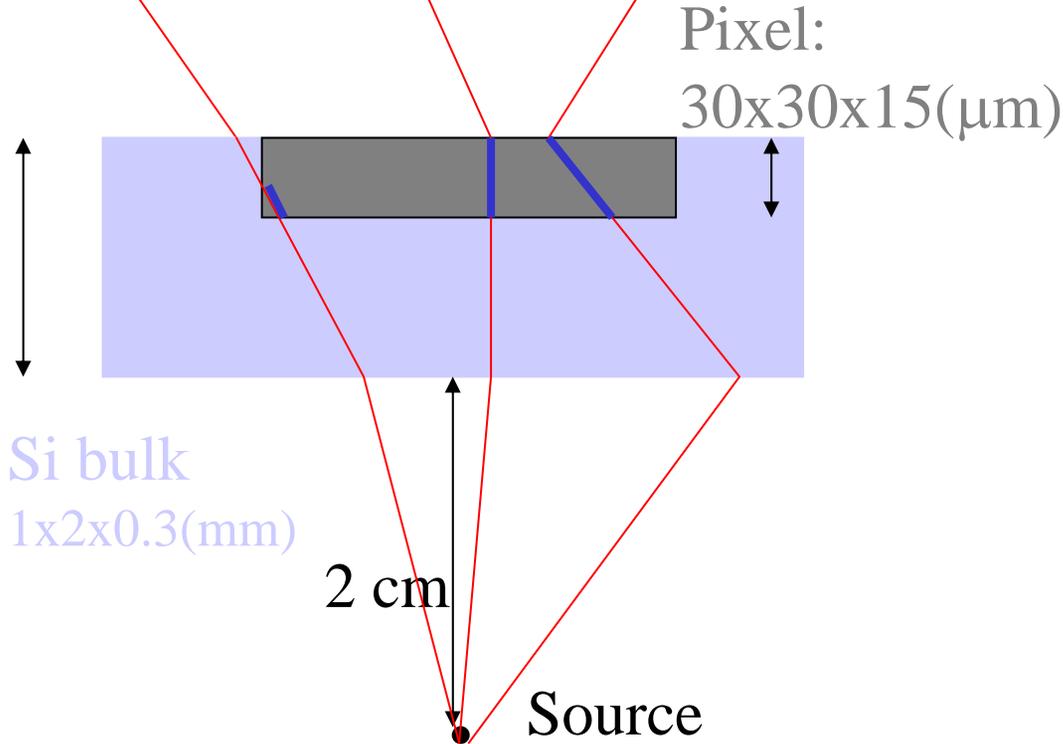
Geant4 simulations indicate that material used to support the sensor might produce large (multiple scattering) effects due to the very low momentum of the impinging electrons.

– The chip holders (apsel0 vs apsel1) are slightly different: Inserted a 300 μm thick Al radiator (with a 1 mm hole) to dissipate power (on the back) and mount the (apsel1) die.

The effect of the not uniform efficiency region

Q released

Starting with a
"perfect" Landau:
Q released by
a MIP in15 μm...

(e-)
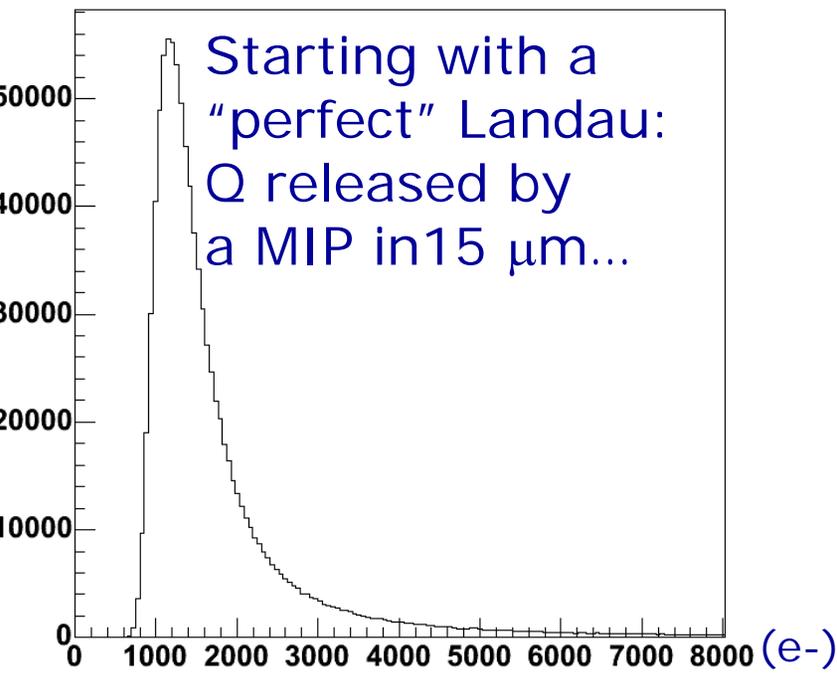
$$Q(collected,r)=Q(released,r)*\varepsilon(r)$$
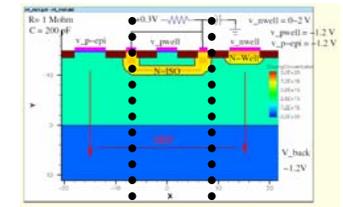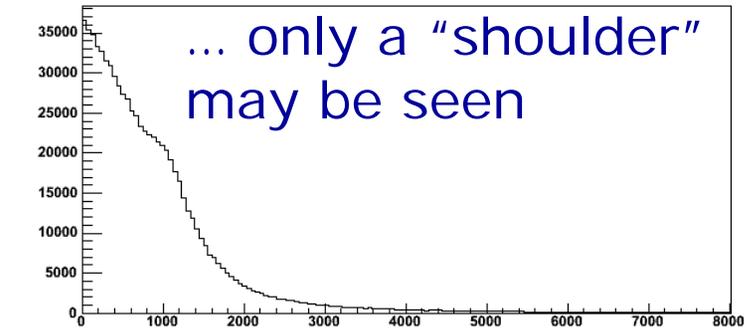
Charge collection efficiency
(from ISE simulation)

Q collected

... only a "shoulder"
may be seen
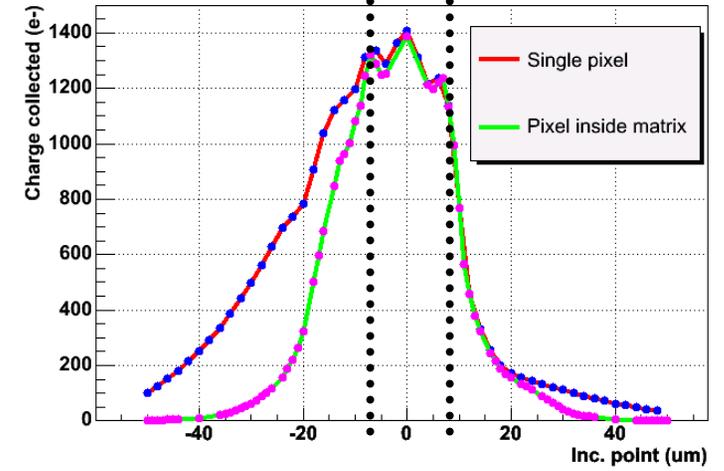
The larger the region,
the smaller the shoulder

(.. and less sensitive to a deconvolution ...)

This effect is expected to be
less significant in the matrix.

Further investigations

- Still investigating the best set-up to enhance the "Landau" (MIP crossing $\perp$ the sensitive region)

- The actual spectrum with β-rays (low energy e-) prevents us from measuring a Signal/Noise ratio for MIP for apsel1.

  Relying on the measurements on Fe^{55}, we can expect:

$$\frac{S}{N} \approx 22 \text{ for MIP}$$

CCE with laser spot on apsel1
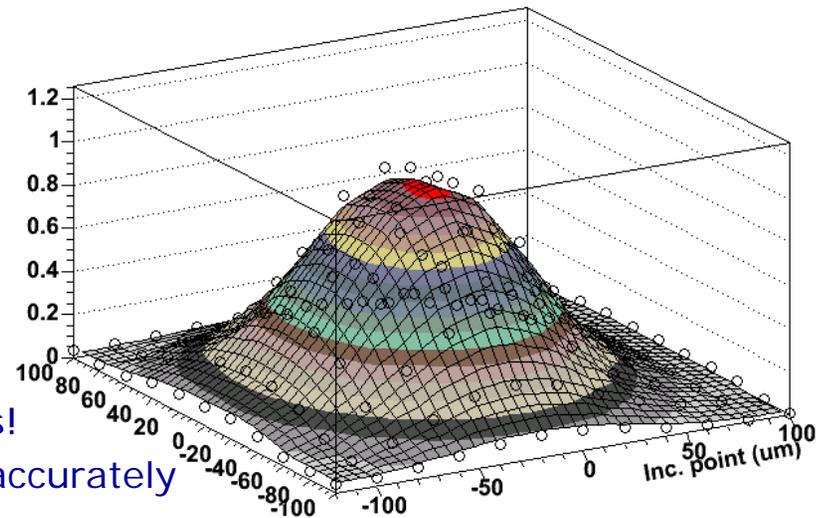
- A scan with an I.R. laser with a small spot size used to measure CCE efficiency across the pixel cell, for:
  - comparison with simulations
  - differences apsel0/apsel1
    - Dummy metals are causing reflections!
    - vertical position must be reproduced accurately

Work in progress

Test of the matrix

- Available (only) the digital info (latch output)
- Unique discriminator Threshold value for all the pixels

IN	OUT
100011	100011
010011	010011
100010	100010
000111	000111

10010100…

Vth

chip

TLA 715

Pattern
Generator

Logical
Analyzer

00010101…
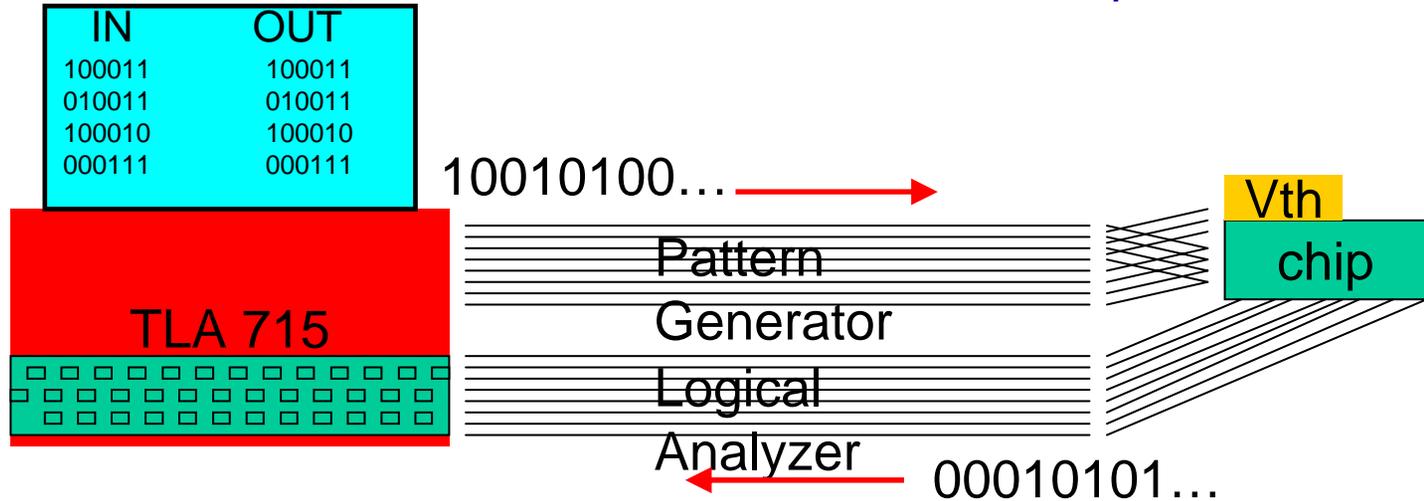
- Sequential readout of the matrix successfully tested up to 30 MHz
- Test Results:
  - Noise scan (latch firing efficiency vs discriminator thr.)
    - ➢ Significant Threshold dispersion
    - ➢ How to cure the effect
  - Threshold scan with trigger on external pulse
    - ➢ I.R. laser
    - ➢ Response to radioactive sources (β and X) w/o analog info:
      - ✓ Integral rate vs Thr. → differential rate = Energy spectrum

Noise scan

$T=30\mu m$

Sequence:

RST

GATE

$\tau=3\mu S$

ENABLE(0,7)

8 clock ticks (x30 ns) to readout the 8 columns
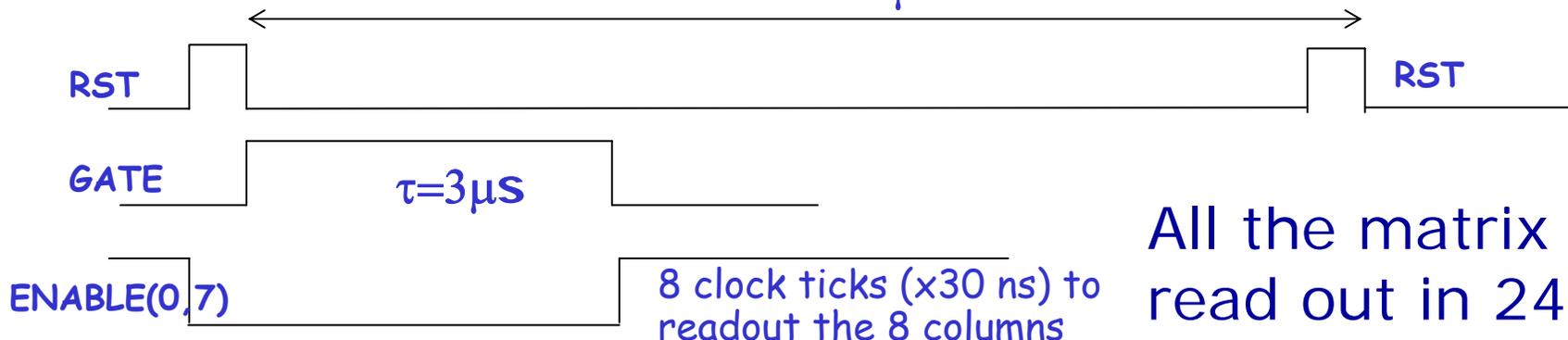
All the matrix read out in 240 ns

RST
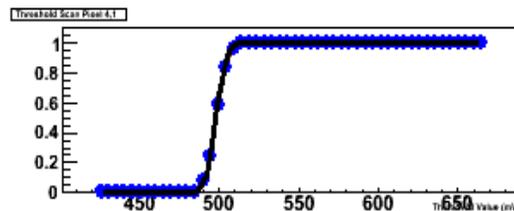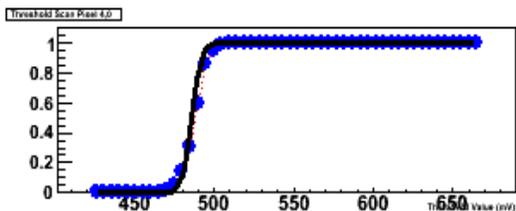
Typical "S" curves:
Occupancy vs. Threshold (mV)
with error function fit
for the pixel of one row
(5 mV step)

50 %
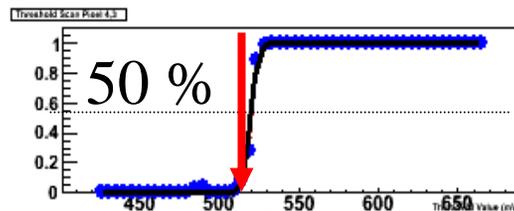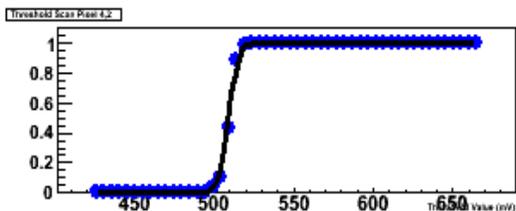
VTH(50 %)

noise

VTH(50 %) provides an estimate of the baseline **offset** of the shaper output

offset

THR

SHAPER OUT:

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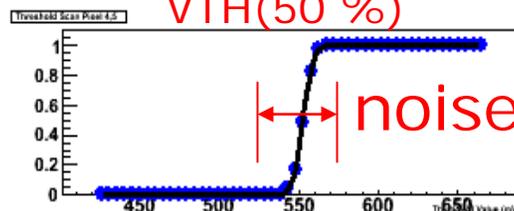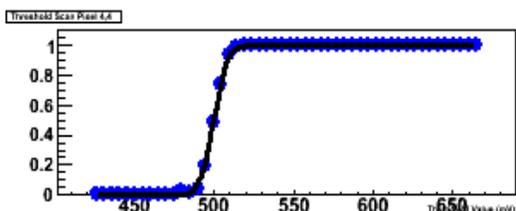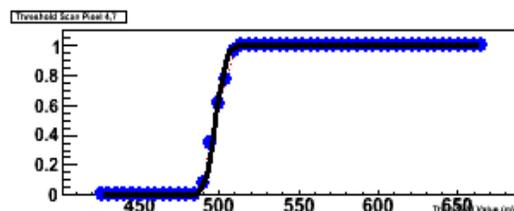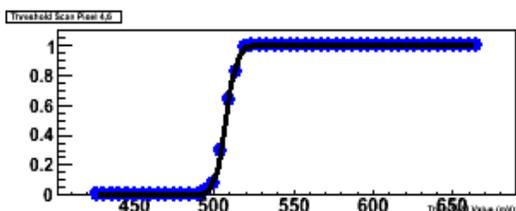
Vth(50%) dispersion and noise on the matrix

In a CMOS process threshold voltage (and channel transconductance g_m) typically affected by microscopic variations in physical quantities(e.g. oxide thickness, dopant concentration …)

Dispersion of the fitted thr0.5

1-D plot	
Entries	64
Mean (mV)	522.5
RMS	23.32
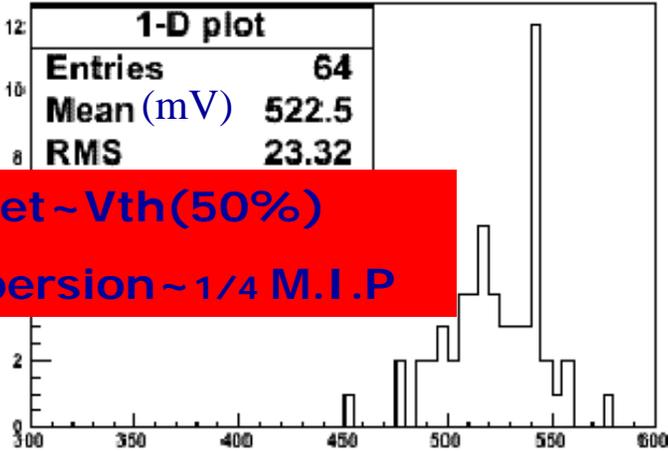
Offset~Vth(50%)

Dispersion~1/4 M.I.P

Dispersion of the fitted noise

1-Ds plot	
Entries	64
Mean (mV)	5.662
RMS	1.902
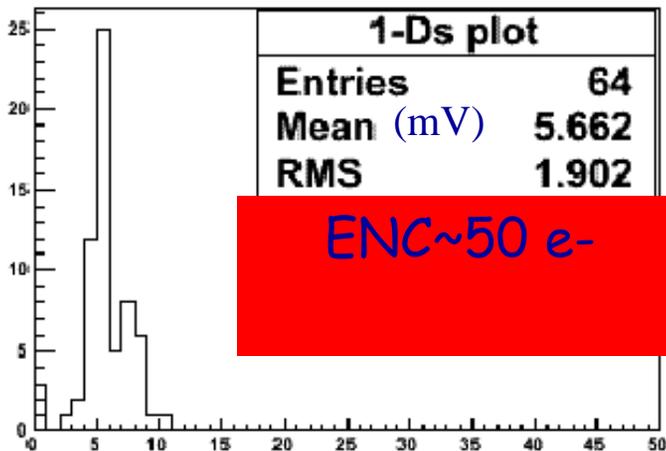
ENC~50 e-

- Possible to act on the device dimensions:

$$\sigma_{V_{th}^{MOS}} = \frac{A_{V_{th}^{MOS}}}{\sqrt{WL}}$$

$A_{V_{th}^{MOS}}$ constant provided by the foundry

- The dominant contribution to the threshold dispersion is expected to come from the dispersion on the shaper output baseline.

- In the Apsel1 chip, MC simulations in fair agreement with the results from the characterization of the matrix.

- Significant reduction (~factor 10) of the dispersion obtained by redesigning of the transconductor and part of the shaper (without increasing the ENC)
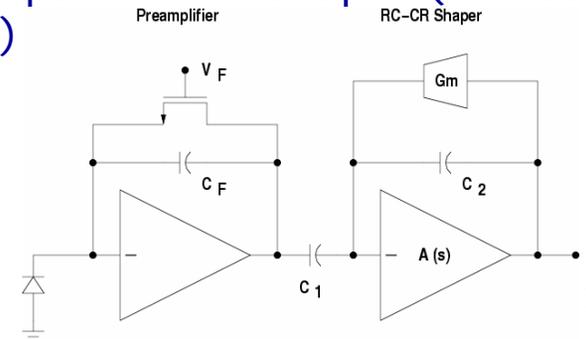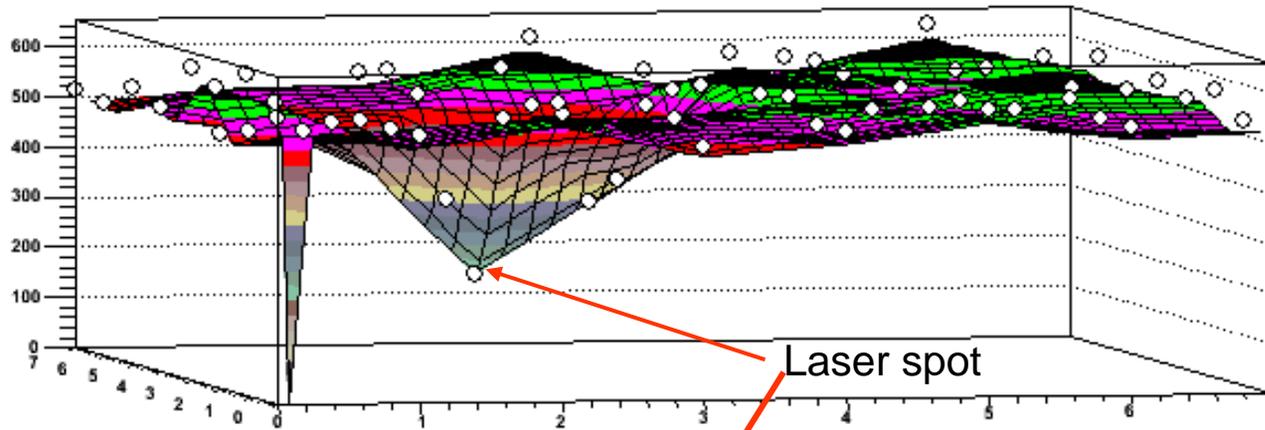
Preamplifier   RC–CR Shaper

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I.R. (1060 nm) laser

Graph2D

Laser spot

Fitted thr offset
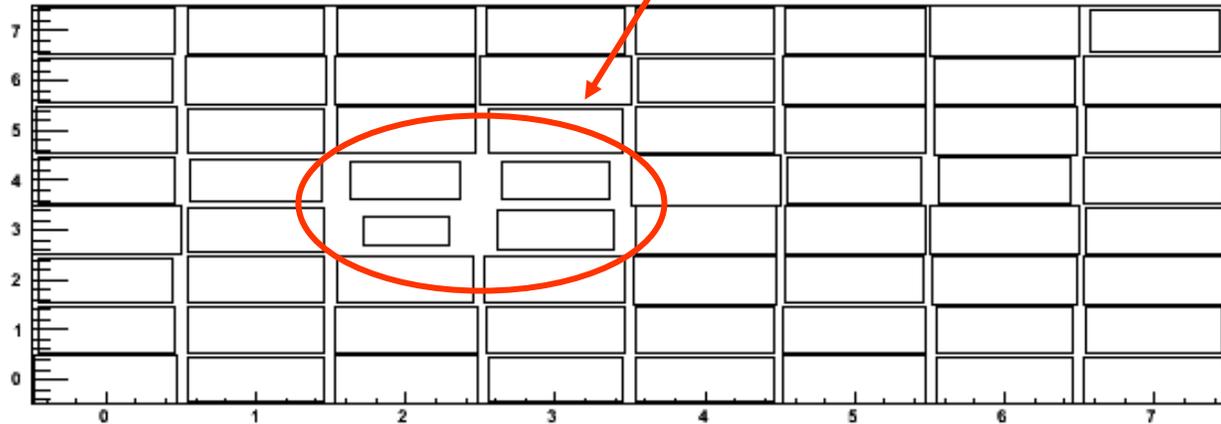
The laser beam ($\sigma_x = \sigma_y \sim 10\ \mu m$, Power$\sim$150 fJ/pulse) releases $\sim$3000 e- in 15 μm of active volume (metal dummies cause reflection).
First indication on the cluster size for charge uniformly distributed.

TH-scan with X-ray and β sources

During these measurements we have observed various effects that distort the resulting energy spectra not-trivially, hence we choose not to show the spectra at this time.

We are investigating the origin of these effects (cross-talk among the pixels in the matrix, ground bounce, ...?) both by checking at the layout level and with specific diagnostic tests.

Toward Apsel2

We are working on the design of the next chip:

- Matrix 8x8 (same read out):
  - FE modified to reduce the Thr. Dispersion
  - Insert analog info on a selection of pixels
  - Inj. Capacitance for ext. stimulus
  - Hopefully we can cure the "cross-talk"

  for diagnostic purpose

- Single pixel channels with different collecting electrode

Area → micromatrix 3x3 with analog/digital info available
for the central pixel
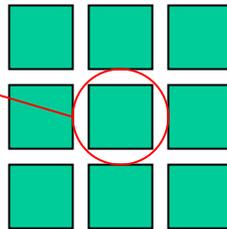
- A lot of work ongoing toward sparsification implemented at the pixel level (verilog simulation phase): test structures to test digital blocks of readout architecture will be implemented.

Conclusions (I)

- A novel kind of CMOS MAPS (deep N-well MAPS) has been designed and fabricated in a 130 nm CMOS technology:

  - A deep n-well used as the sensitive electrode

  - The standard readout channel for capacitive detectors used to amplify the charge signal and extract digital information

- The first prototype, apsel0, was tested and demonstrated that the sensor has the capability of detecting ionizing radiation.

- In the new chip, apsel1, noise and gain issues (present in apsel0) have been correctly addressed.

- Single pixel measurements confirm the observation of soft X and β rays

- The 8x8 (simple) matrix has been successfully readout

Conclusions (II)

- Still ongoing analysis of the response to radioactive sources from the pixel matrix

- Next submission (Aug. 06) focused on:
  - Cure the threshold dispersion
  - More diagnostic features on pixel matrix
  - Test digital blocks toward data sparsification

- Our final goal: to develop a matrix with sparsified readout suitable to be used in a trigger (L1) system based on associative memories.

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4 Workpackages:

.1 MAPS and Front End Electronics

.2 Detectors on high-resistivity Silicon

.3 Trigger / DAQ

.4 Mechanics/Integration/Test-Beam