

MCOR Tester Programmers Guide

Version 1.0

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MCOR Tester Programmers Guide

Revision History

Document

Version	Date	
1.0	12/18/13	New Design

FPGA

Version	Date	
1.0	12/18/13	New Design

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Set/Reset Registers

Many of the functions are controlled by three registers within the block of registers:

Status Register

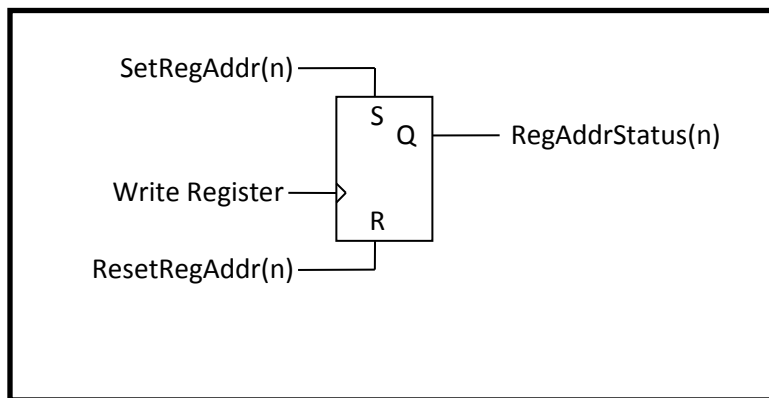
This Register will contain the current value of the settings for the particular bits.

Set Register

Writing a '1' to a bit in this register will SET the corresponding bit in the Configuration/Status register without affecting any other bits.

Reset Register

Writing a '1' to a bit in this register will CLEAR the corresponding bit in the Configuration/Status register without affecting any other bits.



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UDP Packets

The MAC and IP address are stored in the SD Memory Card. On power-up, the SD Memory Card is read. If the data on the card is a valid PIC/Lion Chassis Configuration, the MAC and IP address from the SD Card are used. If the data is not a valid PIC/Lion Chassis Configuration, the MAC and IP addresses are set to the default value:

MAC	08:00:56:00:03:00
IP	C0:A8:00:01 (192.168.0.1)

UDP Address

The Cells UPD Port address is 56789.

UDP Protocol

UDP Header

All messages have the same 12 Byte header consisting of:

Byte		
0	Protocol Version	1 Byte
1	Task ID	1 Byte
3-2	Padding	2 Bytes
7-4	Word Address	4 Bytes
9-8	Word Count	2 Bytes
11-10	Padding	2 Bytes

Protocol Version

Protocol Version used for this message. The MSB of the Protocol Version is used to indicate a Read or a Write.

Bit		
7	Write/Read	'1' → Write from IOC to Chassis
6	Endian	'1' → Little Endian
[5..0]	Protocol Version	0x01

Task ID

Unique identifier supplied by the driver. The Task ID is returned in the Response Message. This can be used to check the validity of the Response Message.

Address

The Word Address is the starting address of the Desired Block.

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Word Count (16 Bit words)

The Word Count is the number of words that follows, NOT including the 8 Byte Header. Maximum block size is 512 words (1K Bytes).

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UDP Write Commands

UDP Write Commands write to one or more sequential register. The Chassis will respond to all Write Commands with a Response Message. The Response Message word count will be zero.

Write Command from IOC

Byte		
0	0x01	Protocol Version
1	0x55	Task ID
2-5	0x00000002	Address
6-7	0x0004	Word(16 bit) Count
8-9	Data 0	
10-11	Data 1	

Response from Chassis

Byte		
0	0x01	Protocol Version
1	0x55	Task ID
2-5	0x0002	Address
6-7	0x0000	Word(16 bit) Count

UDP Read Commands

UDP Read Commands returns a block of data starting at the Address.

Read Command from IOC

Byte		
0	0x01	Protocol Version
1	0x55	Task ID
2-5	0x00000000	Address
6-7	0x0000	Word Count

Response from Chassis

Byte		
0	0x01	Protocol Version
3	0x55	Task ID
4-5	0x0000	Address
6-7	0x0004	Word Count
4-5	Data 0	Data
6-7	Data 1	

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Register Memory Map

	0x0000	Fault Control Status
	0x0001	Fault Control Set
	0x0002	Fault Control Reset
Magnet Fault Control	0x0003	Magnet Fault Control Status
	0x0004	Magnet Fault Control Set
	0x0005	Magnet Fault Control Reset
Status	0x0006	Monitor Readback
	0x0007	Unused
	0x000F	
System ID	0x0010	Firmware Version
	0x0011- 0x0018	System ID
	0x0019- 0x0020	Sub Type
	0x0021- 0x0028	Firmware Date
	0x0029- 0x002F	Unused
Xilinx System Monitor	0x0030	Current Temp
	0x0031	Current $V_{(Int)}$
	0x0032	Current $V_{(Aux)}$
	0x0033	Max Temp
	0x0034	Max $V_{(Int)}$
	0x0035	Max $V_{(Aux)}$
	0x0036	Min Temp
	0x0037	Min $V_{(Int)}$
	0x0038	Min $V_{(Aux)}$

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Fault Control

Address			
0x0000	Fault Control Status	uInt16	
0x0001	Fault Control Set	uInt16	
0x0002	Fault Control Reset	uInt16	

Fault Control Status

This register contains the status of the Fault Bits.

Bit	Function		
[15..0]	Fault[15..0]		

Fault Control Set

Writing a '1' to a bit in this register sets the corresponding Fault Output.

Fault Control Reset

Writing a '1' to a bit in this register resets the corresponding Fault Output.

Magnet Fault Control

Address			
0x0003	Magnet Fault Control Status	uInt16	
0x0004	Magnet Fault Control Set	uInt16	
0x0005	Magnet Fault Control Reset	uInt16	

Magnet Fault Control Status

This register contains the status of the Fault Bits.

Bit	Function		
[15..11]	Unused		
10	Water Sum Fault		
9	Gnd_Res		
8	HV Fault		
[7..0]	Magnet Fault[7..0]		

Magnet Fault Control Set

Writing a '1' to a bit in this register sets the corresponding Fault Output.

Magnet Fault Control Reset

Writing a '1' to a bit in this register resets the corresponding Fault Output.

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Status Register

Address			
0x0006	Status	uInt16	

Status Register

This register contains the status from the MCOR.

Bit	Function		
[15..6]	Unused		
5	Reset_Det		
4	Inhibit_Det		
[3..0]	Interlock Det[4..1]		

Read System Information Response

Address			
0x0010	Firmware Version	uInt16	0x0100 (Version 1.00)
0x0011- 0x0018	System ID	8 Bytes, ASCII	"MCOR "
0x0019- 0x0020	Sub Type	8 Bytes, ASCII	"TESTER "
0x0021- 0x0028	Firmware Date	8 Bytes, ASCII	"mm/dd/yy"

Xilinx System Monitor

The Xilinx contains an on-chip monitor that, among other things, allows access to the chip temperature and $V_{(Int)}$ and $V_{(Aux)}$. The current value as well as the Min and Max are stored in the Xilinx and can be readout via the System Monitor Interface.

Read Xilinx Monitor Response

Address		
0x0020	Current Temp	UInt16
0x0021	Current $V_{(Int)}$	UInt16
0x0022	Current $V_{(Aux)}$	UInt16
0x0023	Max Temp	UInt16
0x0024	Max $V_{(Int)}$	UInt16
0x0025	Max $V_{(Aux)}$	UInt16
0x0026	Min Temp	UInt16
0x0027	Min $V_{(Int)}$	UInt16
0x0028	Min $V_{(Aux)}$	UInt16

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$$Temperature (^{\circ}C) = \left(\frac{Counts}{64} * 503.975/1024\right) - 273.15$$

$$Volts = \frac{Counts}{64} / 1024 *$$

$$V_{(Aux)} = 2.5V$$

$$V_{(Int)} = 1.0V$$