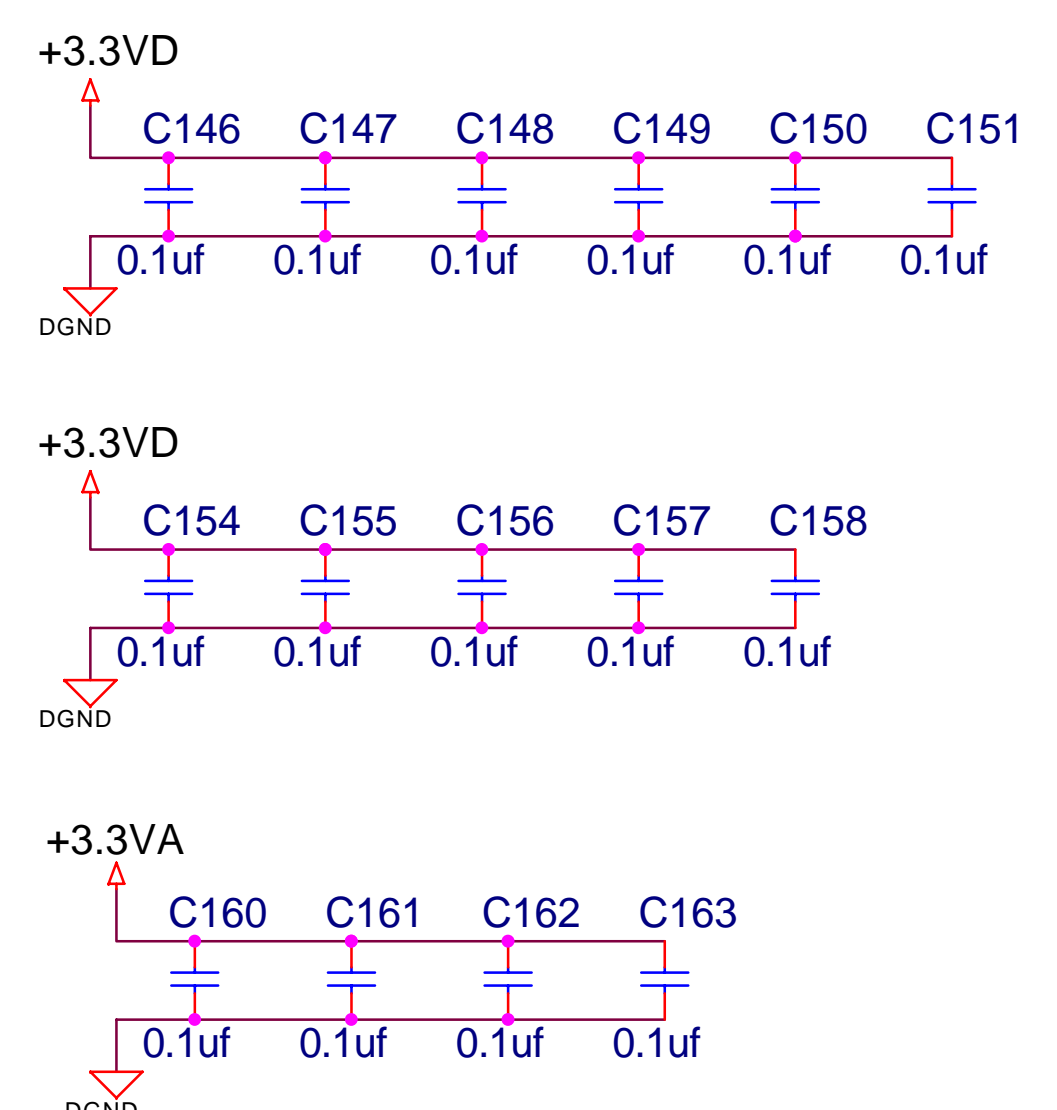


Digikey  
 490-1044-1-ND  
 BLM21BD121SN1D  
 FERRITE CHIP 120 OHM 200MA 0805

**Ethernet 10BaseT (Twisted Pair)**

Pin #	Signal Name	Function
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	NC	No Connection
5	NC	No Connection
6	RD-	Receive Data
7	NC	No Connection
8	NC	No Connection



Till's Note:  
 The coldfire's DMA timers can be used to initiate a DMA transfer ('timer' is a bit misleading, in principle it's just an external input which when strobed triggers a DMA transfer) w/o CPU intervention.  
 IMO it would be an advantage to route the 'fifo full' signal (or whatever it is that currently is routed to IRQ2 (on my devel. board)) also to one of the DTINs (pins 72 or 74 at the DIMM connector).

STANFORD LINEAR ACCELERATOR CENTER U.S. DEPARTMENT OF ENERGY STANFORD UNIVERSITY STANFORD, CALIFORNIA		CAD FILE: SD71411430C0	
LCLS RF PAD 4 Chan ADC Board			
ENG	R Akre	DATE	7/31/2006
DFTR	R Akre	DATE	7/31/2006
CHKR		APPROVAL	
LAST MOD	Wednesday, November 08, 2006		SD 714-114-30-C0