

LCLS

Phase and Amplitude Controller PAC

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2K samples X 16 bits = 32K bits * 2 = 72Kbits of memory

360 Hz = 2.77mS

Switching to uCDIMM processor board

3 Trigger Modes

- 00 – External Trigger
- 01 – Internal Trigger
- 10 – CPU Trigger

Voltages to monitor

	Source	Type	Range	
0	SSSB Amp	Temperature		
1	IQ Modulator	Temperature		
2	Control Board	Temperature		
3	SSSB Amp	Bulk Supply	+12V	
4	SSSB Amp	Bulk Supply	-12V	
5	RF Board	Bulk Supply	+15V	
6	Control Board	Bulk Supply	+5V	

ColdFire Configuration

The PAC board interface to the Coldfire uses Chip Select, CS1 and Byte Select BS3 and BS2. To properly configure the Coldfire, Port J Register, (PJPAR) must be configured for Byte Select and Chip Select functionality, not IO. This is done by writing an 0xFF to address 0x40100054. Then you must configure the Chip Select Module (CSM) for proper decoding of the base address.

ColdFire Configuration

	Register	Value	Comment
0x40100054	PJPARG	0xFF	Configure PJPARG for Byte and Chip Select, NOT IO
0x4000008C	CSAR1	0x80000000	PAC Base Address
0x40000090	CSMR1	0x00000001	Sets Valid bit
0x40000096	CSCR1	0x000000A0	Set for 16 bit, Not internal TA, Enable BS, No Burst.

Memory Map

Register Number	Memory Address	Use		
	0000 0FFE	I Memory	16 bit Signed Integer	
	1000 1FFE	Q Memory	16 bit Signed Integer	
0	2000	Control Register	16 bit unsigned	
1	2002	DAC Delay	16 bit unsigned	
2	2004	SSSB Delay	16 bit unsigned	
3	2006	SSSB Width	16 bit unsigned	
4	2008	Ext Trigger Delay	16 bit unsigned	
5	200A	Ext Trigger Width	16 bit unsigned	
6	200C	Int Trigger Rate	16 bit unsigned	
7	200E	Reserved		
8	2010	PAC Temperature	16 bit unsigned	
9	2012	IQ Temperature	16 bit unsigned	
10	2014	SSB Temperature	16 bit unsigned	
11	2016	VFWD	16 bit unsigned	
12	2018	VREFL	16 bit unsigned	
13	201A	SSB_PWR	16 bit unsigned	
14	201C	+5V	16 bit unsigned	
15	201E	-12V	16 bit unsigned	
16	2020	CPUTrig address		
17	2022	I Offset	16 bit 2's Comp	V08
18	2024	I Gain	16 bit 2's Comp	V08
19	2026	II Coefficient	16 bit 2's Comp	V08
20	2028	IQ Coefficient	16 bit 2's Comp	V08
21	202A	Q Offset	16 bit 2's Comp	V08
22	202C	Q Gain	16 bit 2's Comp	V08
23	202E	QQ Coefficient	16 bit 2's Comp	V08
24	2030	QI Coefficient	16 bit 2's Comp	V08

Temperature Conversion:

ADC input is 0 to 2.5V, Temp input is 20C to 70C, ADC output is 0 to 16383 counts so the conversion is

$$T (C) = (\text{Count} / 16384) * 2.5 * 20 + 20$$

Voltage Conversion:

ADC input is 0 to 2.5V, Input voltage is 0V to 20V so the conversion is

$$V(\text{in}) = (\text{Count} / 16384) * 20$$

The -12V ADC reading will show a positive 12V since the input is inverted.

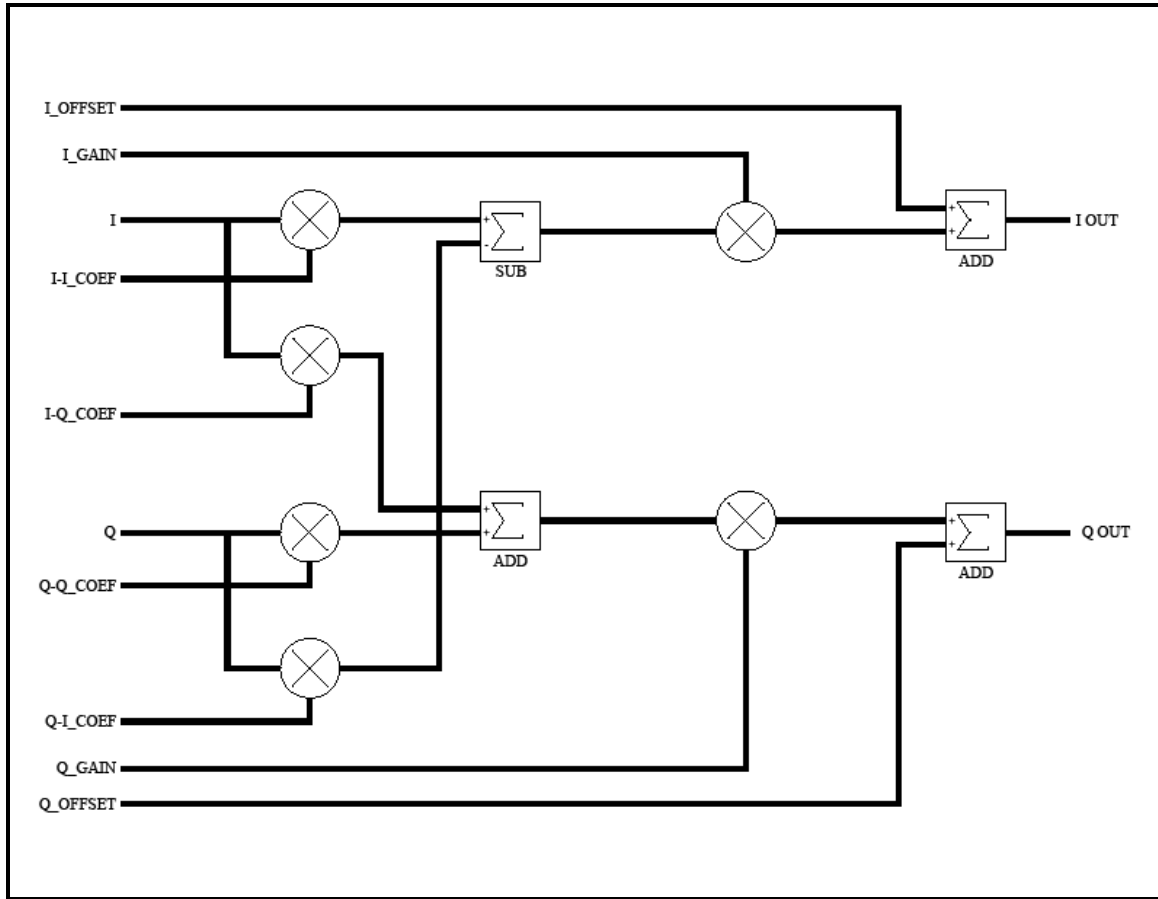
Control Register (2000)

Bit			R/W	
[15..08]	Version Number		R	
[07..05]	Unused			
04	119Mhz missing	Check 119Mhz clock for 90-150Mhz. Latched value '1' => Clears flag	R/W	
03	Ext Trig missing	No transition on Ext Trig in 1sec Latched value '1' => Clears flag	R/W	
02	SSBOverTemp	SSB Over Temperature Latched value '1' => Clears flag	R/W	
[01..00]	Trigger Mode	'10' => CPU Trigger	R/W	
		'01' => Internal Trigger		
		'00' => Normal; External Trigger		

LED's

D1	119Mhz missing	Current status of 119Missing OneShot		
D2	Ext Trig missing	Current status of EXT Trig Missing OneShot		

IQ Calculations



Connector Assignments

H1	SSSB OverTemp		Input	0-20V
H7	Trigger Out		Output	TTL
H9	I Monitor		Analog	
H10	Q Monitor		Analog	
H11	Reset			
H12	IQ Modulator Temperature	AD592	Temp	
J1	Ethernet Port			
J2	119Mhz	10Dbm (min)	Input	RF
J3	External Trigger		Input	NIM
J4	Q Out		Analog	50 ohm
J5	I Out		Analog	50 ohm
J6	SSB Gate	Copy of P5-12		
J7	Trigger Out	Copy of H7	Output	TTL
J11	Alternate Ethernet			
J10	Alternate Trigger			
P1	RS232 Port 0	From Arcturus		
P5	SSB IO			
P6	Power Connector			

P5 Connector Pinout

Pin				
1	SSB Temperature	AD592	Temp	I out
2	SSB Temperature		Temp	Return
6	SSB VFWD		Analog	
8	SSB VREFL		Analog	
10	SSB V+		Analog	
12	SSB Gate	Copy of H6	Output	TTL
14(*)	SSB OverTemp	Same as H1	Input	0-20V

(*) Wire modification on Rev 1 board

P6 Connector Pinout

Pin				
1	+5V			
2	+5V			
3	+5V			
4	-12V			
5	GND			
6	GND			
7	GND			
8	+12V			

Xilinx Version History

	Version			
11/08/06	04	Recompiled firware under ISE8.2		
		Having problems getting over 110Mhz with new ISE??? ReWrote prog_strb using 1 up counter. Got 133Mhz		
	04inv	Discovered glitch on the Q output. Inverted Clock to see if this fixes the timing problem with the DAC clock	OK	
11/08/06	05	Added logic for Stby Trigger		
	06	?		
	07	?		
08/18/08	08	Added internal IQ calculations		

ARCTURUS Configuration:

Sample configuration:

```
B$
B$ printenv
FACTORY=Arcturus Networks Inc.
REVISION=uC5282 Rev 1.0 4MB External Flash SERIAL=X43287EE6-018DA
CONSOLE=ttyS0 KERNEL=0:linux.bin KERNEL_ARGS=root=/dev/rom0
HWADDR0=00:06:3B:00:58:DA
FW_VERSION=180001
_0=10000000:400000:RW
RAMIMAGE=yes
CACHE=on
NTP_SERVER=134.79.16.10
NETMASK=255.255.252.0
DNS_SERVER=134.79.18.40
GATEWAY=134.79.115.1
IPADDR0=134.79.112.71
HOSTNAME=jjolab
INIT=134.79.19.29:/afs/slac:u/el/jjo/LCLS/PAC/epics/ioc/iocBoot/iocPac/
st.cmd

B$
```

Commands to configure:

```
setenv NTP_SERVER 134.79.16.00
setenv DNS_SERVER 134.79.18.40
setenv GATEWAY 134.79.115.1
setenv INIT
134.79.19.29:/afs/slac:u/el/jjo/LCLS/PAC/epics/ioc/iocBoot/iocPac/st.cm
d

setenv IPADDR0 134.79.113.21
setenv HOSTNAME PCD-MARX-GC

--

setenv AUTOBOOT 10 -- Wait 10 seconds before automatically starting OS
```