Application Note

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Migrating from the MCF5272 to the MCF5282

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This application note describes what designers and programmers should consider when migrating from the MCF5272 to the MCF5282. It discusses the differences between the two devices, and, for future MCF5282 users, highlights ways in which their similarities allow the MCF5272 to be used as an interim development solution.

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1.1 Introduction

The MCF5282 is the first microcontroller with integrated Ethernet, Flash, and CAN (controller area network). It is the first MCU in the ColdFire family that incorporates MPU performance and an MPU peripheral set, thus building on the capabilities of existing products such as the MCF5272.

Note that this a preliminary document that may be modified when the MCF5282’s operation can be fully characterized. To locate any published errata or updates for this document, refer to the web site at http://www.motorola.com/semiconductors.

1.2 Differences Overview

There are a number of differences that need to be taken into account when migrating from the MCF5272 to the MCF5282. Table 1 gives an overview of the differences between the two devices.

Table 1. MCF5272/MCF5282 Differences Overview

MCF5272	MCF5282	Comments
ColdFire Version 2 Core		
One stack pointer	Two stack pointers	The core enhancements maintain backwards compatibility with the V2 core on the MCF5272. Therefore, if the new features are not used, then there is no impact on hardware/software reuse. **Note:** The dual stack pointer implementation is disabled in the cache control register (CACR).
ISA_A	ISA_A+	
MAC	EMAC	
Revision A Debug module	Revision A Debug module	No change
On-chip Memory		
4K SRAM	64K SRAM	Much larger SRAM on MCF5282. **Note:** The RAMBAR is now accessed at a different CPU space offset.
No Flash	512K Flash	512K of on-chip Flash allows for single-chip operation. Flash also has security and protection features.
Cache		
1K instruction cache	2K instruction, data, or instruction/data cache	The control bits shared by both devices are in the same locations. New bits in the MCF5282 CACR determine if the cache is used for instructions, data, or both. These new bits are in locations that were reserved on the MCF5272. As long as the reserved bits are all cleared, an MCF5272 cache initialization could be used for the MCF5282 without any change.
Serial Communications		
2 UARTs	3 UARTs	Both devices use the same UART (universal asynchronous receiver transmitter); however, the third MCF5282 UART does not have $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ flow control signals. It does have the ability to trigger DMA (direct memory access) transfers.
None	I^2C	The I^2C (inter-integrated circuit) module used for the MCF5282 is also used on the MCF5307/MCF5407 and other ColdFire devices. The I^2C provides two-wire, half-duplex communication.
QSPI	QSPI	The QSPI (queued serial peripheral interface) modules are the same for the two devices. The only difference is the memory map location of the registers.

Table 1. MCF5272/MCF5282 Differences Overview (continued)

MCF5272	MCF5282	Comments
Interrupt Controller		
1 interrupt controller	2 interrupt controllers	The interrupt controllers for the MCF5272 and MCF5282 are similar in that both interrupt controllers have hard-coded vector numbers for each possible interrupt source. The programming model used by the interrupt controllers, however, is very different. For the MCF5272, each 32-bit interrupt control register (ICR) determines the interrupt level for eight different interrupt sources. For the MCF5282, there is one 8-bit ICR for each interrupt source where the ICR setting determines both a level and priority for the associated interrupt source. The ICRs are similar to those used for the 5307.
6 external interrupts	Edge Port Module	The MCF5282's Edge Port module offers more flexibility for external interrupts. There are seven external interrupt pins on the MCF5282 that generate fixed-level interrupts and can also be used as GPIOs (general-purpose input/outputs). Interrupts can still be programmed to trigger on rising, falling, or both edges, whereas the MCF5272 interrupts trigger only on the rising or falling edge. Although the functionality offered is very similar, the programming model for external interrupt support is different.
External Bus		
8 chip selects	7 chip selects	The MCF5272 uses a different chip select module than previous ColdFire parts. The MCF5282 returns to the standard ColdFire chip select module; therefore, though the chip selects on the MCF5282 differ from the MCF5272, they are the same as those found on the MCF5407.
1 bank of SDRAM	Up to2 banks of SDRAM	The MCF5272 uses a different SDRAM controller than previous ColdFire parts. The MCF5282 returns to the standard ColdFire SDRAM controller; therefore, though the SDRAM controller on the MCF5282 differs from the MCF5272, it is the same as the one found on the MCF5407.
Bus control signals	Bus control signals	Both devices have similar bus interfaces, but some signals are different. The most notable change is that the $\overline{CS}$, $\overline{BS}$, and $\overline{OE}$ signals all transition off of the falling clock edge. This change in the timing makes the address setup and address hold features used by the MCF5272 chip selects unnecessary for the MCF5282.
DMA		
1 channel DMA	4 channel DMA	The functionality and features of the MCF5272 and MCF5282 DMA modules are very similar, but the MCF5272 uses a different DMA module than previous ColdFire parts. The MCF5282 uses the standard ColdFire DMA module with enhanced programmable requests from the UARTs and DMA timers.

Table 1. MCF5272/MCF5282 Differences Overview (continued)

MCF5272	MCF5282	Comments
Timers		
4 16-bit timers	4 32-bit DMA timers	The timer module on the MCF5282 is an enhanced version of the MCF5272 timers. The timers have been expanded to 32-bits, and two additional control registers have been added to accommodate 32-bit operation. Another new feature is that the timer interrupt signals can be used to generate DMA requests.
None	General-purpose timers	The MCF5282 has two 4-channel general-purpose timers (GPTs). Each channel can be configured for input capture and output compare. Two channels can be paired for pulse width accumulation, and another channel supports two modes of pulse accumulation.
None	Programmable interrupt timers	The MCF5282 implements four fully-independent timers (PITs) that provide precise interrupts at regular intervals.
FEC		
Error bits in TxBD (HB, LC, RL, and UN)	Error indication added to interrupt event register (EIR)	For the MCF5282, the heartbeat error, late collision, retry limit, and underrun status bits have been removed from the TxBD and relocated to the interrupt event register (EIR). This is beneficial in that interrupts can be triggered for any of these conditions by clearing the associated interrupt event mask register (EIMR) bit.
Error bits in TxBD (RC and CSL)	MIB counter block	The retry count and carrier sense lost bits have been removed on the MCF5282. The information can be obtained by using the MIB counter block.
Single individual address	Hashing on individual address	Whereas the MCF5272 can only use hashing for multicast frames, the MCF5282 can use hashing for individual MAC (media access controller) addresses. Customers who do not want to use individual address hashing should clear the individual upper address register (IAUR) and individual lower address register (IALR).
Maximum frame length register (MFLR)	Receive control register (RCR)	The maximum frame length and flow control enable are now stored in the MCF5282's RCR.
Transmit FIFO start register	No transmit FIFO start	For transmits on the MCF5282, the start of the FIFO is hard-coded to the beginning of the FIFO.
System Integration/Control		
System Integration Module (SIM)	System Control Module (SCM)	Though both modules encompass similar features, some functionality (detailed below) that is part of the SIM has been reassigned to separate modules in the MCF5282. The module name has been changed to reflect this change in functionality.
MBAR	IPSBAR	The MCF5282 does not use the MBAR CPU space. Instead, IPSBAR is used as the base address for the module registers. The IPSBAR is accessible at the IPSBAR address. IPSBAR defaults to 0x4000_0000 at reset.

Table 1. MCF5272/MCF5282 Differences Overview (continued)

MCF5272	MCF5282	Comments
System configuration register (SCR)	Reset control register (RCR), core reset status register (CRSR), and bus master park register (MPARK)	The last reset indicator bits from the SCR are replaced by the MCF5282's RCR and CRSR registers. The internal bus arbitration is programmed via the MPARK register.
Power management register (PMR) and activate low-power register (ALPR)	Low Power Module	Instead of disabling the clock to each module discretely, the MCF5282 supports four different power modes: run, doze, wait, and stop. The selected mode determines which clocks are disabled. For some modules, the response to low power modes is programmable.
Device identification register (DIR)	Device information loaded into D0 and D1 at reset	Instead of using a dedicated device ID register, the MCF5282 loads device information into general-purpose data registers D0 and D1 at reset.
Watchdog Timer	2 Watchdog Timers	The MCF5282's two watchdog timers provide compatibility with both the ColdFire and M•Core family products. One is the standard ColdFire watchdog timer from the MCF5307/MCF5407 (documented in the SCM section of the MCF5282UM). The second is the watchdog timer previously used on M•Core devices (documented in the watchdog section of the MCF5282UM). Both watchdog timers have programming models and servicing routines that differ from the MCF5272 watchdog timer.
Miscellaneous		
Up to 48 GPIOs	Up to 152 GPIOs	As with the MCF5272, most of the pins on the MCF5282 can be used as GPIOs. To do so, each pin is configured for its GPIO function in pin assignment registers (similar to the P*n*CNT registers on the MCF5272). The primary difference is that the MCF5282 output pins can be set and cleared using the SET*n* and CLR*n* registers.
Bus width and global chip select configuration at reset	Chip Configuration Module (CCM)	Both the MCF5272 and MCF5282 latch in the values of certain pins during reset to determine the chip mode and boot configuration. The MCF5272 uses WSEL and BUSW[1:0] signals that are muxed with some of the QSPI signals to determine the bus width and port size for the global chip select. The MCF5282 uses the same concept, but latches in values from data lines instead of QSPI pins. The MCF5282 also has more boot configuration options than the MCF5272. These options include the following: • Internal vs. external boot • Boot port size • Master mode vs. single chip mode • Clock mode • Chip select/upper address configuration
JTAG	JTAG	The Joint Test Action Group (JTAG) modules on both devices are compliant with the IEEE 1149.1 standard for boundary scan testability. This means the basic JTAG communication is the same; however, the scan chain for each device is different.

1.2.1 MCF5272 Modules Unimplemented on the MCF5282

Table 2 lists the MCF5272 modules unavailable on the MCF5282 and gives suggestions for duplicating their functionality within a MCF5282 design. Note that these options are provided for reference and have not been tested; thus, at this time, they will not be associated with any programming support.

Table 2. MCF5272 Modules Unavailable on the MCF5282

Module	Comments
USB	The following is a list of external devices for duplicating the MCF5272's USB (universal serial bus) functionality with the MCF5282: • The Cypress SL811S USB Slave Controller is a single-chip USB peripheral device that interfaces to microprocessors capable of supporting either full-speed or low-speed transactions. It also supports the Motorola bus. • The Agere USS-820D/USS-820TD (formerly the USS-825) is a USB device controller that provides a programmable bridge between the USB and a local microprocessor bus. Agere also provides an application note that demonstates how the USS-820 can be interfaced to the MC68LC302, (which has an interface similar to the MCF5272). • The National USB Controller (1.0 and 1.1 compliant), USBN9602, is an integrated USB node controller that interfaces to the bus. • The NetChips NET2888 USB Interface Controller allows bulk or isochronous data transfers between a generic local bus and a universal serial bus. NetChips also provides an application note that shows how to interface a MCF5307 with a similar NET2270 device. This application note could serve as a reference for interfacing with the MCF5272.
PLIC	A possible solution is to use an ASIC or other programmable device to implement the physical layer interface controller (PLIC) functionality.
PWM	The pulse width modulation (PWM) functionality can be duplicated by using the GPTs on the MCF5282. The GPTs are capable of implementing PWM on 2 channels with the toggle-on overflow feature.
Soft HDLC	Although the high-level data link control (HDLC) look-up table is not automatically embedded within the MCF5282's internal ROM, it is possible to access the LUT (look-up table) via internal or external memory. The Soft HDLC simply receives or transmits its data from a memory buffer that can be obtained from any appropriate communications channel .

1.2.2 New MCF5282 Modules

Table 3 describes new modules available on the MCF5282 that are not found on the MCF5272. The functionality of these additional modules can simplify and reduce the chip count for MCF5282 designs. Table 3 also provides equivalents for the new MCF5282 functionality that would allow the MCF5272 to be used in designs until the MCF5282 is available.

Table 3. New MCF5282 Modules Unavailable on the MCF5272

Module	Comments
PLL	The phase-locked loop (PLL) module is similar to the module on the MMC2114.
FlexCAN	This new module is similar to the TouCAN module found on the MC68375. Customers using MCF5272 as an interim solution can use the CAN Reference Design daughter card, found at http://www.mot.com/coldfire, for application development.
I^2C	This module is similar to the module on the MCF5307. When using the MCF5272 as an interim solution, the Soft I^2C module may be used as a substitute. Documentation and source code can be found on the MCF5272 product summary page on the Motorola web site.
GPT	This module is similar to the timer module on the MMC2114.
PIT	This module is similar to the PIT module on the MMC2114.
Flash	This is a new module.
QADC	The MCF5282's queued analog-to-digital controller (QADC) module is similar to the module on the MMC2114. The following is a list of external devices that can be used to duplicate the MCF5282's QADC functionality on the MCF5272 for application development: • The Texas Instruments TLV1548 10-bit analog-to-digital (A/D) converter provides a direct 4-wire synchronous serial peripheral interface via the QSPI on the MCF5272. • Although this device is not a 10-bit device, Maxim Integrated Products' MAX155 is an 8-bit, multi-channel, analog-to-digital (A/D) converter that may be a good solution.

1.2.3 Parametric and Mechanical Comparison

Table 4 outlines some of the parametric and mechanical characteristics of the MCF5272 and the MCF5282.

Table 4. Parametric and Mechanical Comparison

	MCF5272	MCF5282
Frequency	66 MHz	66 MHz
Packaging	196-MAPBGA	256-MAPBGA
Capacitive Loading	30 pF	Full or partial loading (25pF/50pF)
I/O Drive Strength	2mA–10mA	Full or partial loading (2mA/4mA)
Operating Temperature	0 C to +70 C or -40 C to +85 C	-40 C to +85 C
Dhrystone 2.1	63 MIPS (SRAM)	63 MIPS (SRAM) 59 MIPS (Flash)
Input Voltage (V_{in})	–0.5 to +5.5	– 0.3 to + 5.0

1.3 Summary

This application note has outlined some of the differences that one must consider when migrating from the MCF5272 to the MCF5282. Particularly, the MCF5282's on-chip Flash, Ethernet, and CAN modules make a wide array of applications possible by bridging the gap between MPU and MCU functionality. For those users who wish to start their development now, this document has also offered some solutions for duplicating MCF5282 functions that do not exist on the MCF5272.

For applications that may require some of the MCU features that the MCF5282 offers, the few changes required to make the migration from the MCF5272 should be well worth the effort.

1.4 References

Table 5 provides a list of references used throughout this application note.

Table 5. References

Motorola Document Number	Title	Revision
MCF5282UM/D	MCF5282 Advance Information Manual	0
MCF5272UM/D	MCF5272 User's Manual	2
CFPRM/D	ColdFire Family Programmer's Reference Manual	2
MCORERM/AD	M•CORE Reference Manual	0

1.5 Document Revision History

Table 6 provides a document revision history for this application note.

Table 6. Document Revision History

Rev. No.	Substantive Change(s)	Date of Release
0	Initial Release	December 2002
0.1	• Table 1, FEC subsection: in the "Single individual address" row, changed "EMAC" in the Comments column to "MAC (media access controller)." • Table 2, Soft HDLC row: changed first sentence to read "Although the high-level data link control (HDLC) look-up table is not automatically embedded within the MCF5282's internal ROM, it is possible to access the LUT (look-up table) via internal or external memory."	January 2003
1	• Rephrased final sentence in Soft HDLC Comments column in Table 2.	October 2003

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