VMIVME-3122
High-Performance 16-bit Analog-to-Digital Converter (ADC)

- 64 differential or single-ended inputs
- 16-bit A/D conversion
- Software-selectable conversion rate (100 kHz maximum)
- Program-selectable scanning of 1, 8, 16, 32, or 64 channels
- Continually digitizes selected input channels and stores the results
- Three trigger modes
  - — Software trigger
  - — External trigger
  - — Interval timer trigger
- Three scan modes
  - — Autoscan
  - — Single scan
  - — Random access
- Programmed VMEbus interrupts
- User-programmable interval timer
- Software-programmable gain 1 and 10
- External trigger to synchronize multiple boards simultaneously
- Jumper-selectable A/D ranges of 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V
- Optional low pass filter
- Overvoltage protected inputs
- 1,024-word data buffer (16-word deep buffer x 64 channels)
- Selectable output coding
- Powers up in autoscanning mode with unity gain

APPLICATIONS

- Factory automation and instrumentation
- Process control
- Laboratory instrumentation
- Machine monitoring
- Data acquisition

INTRODUCTION — This product is designed to support 64 channels of differential or single-ended wide range (±250 mV to ±10 V) analog inputs.

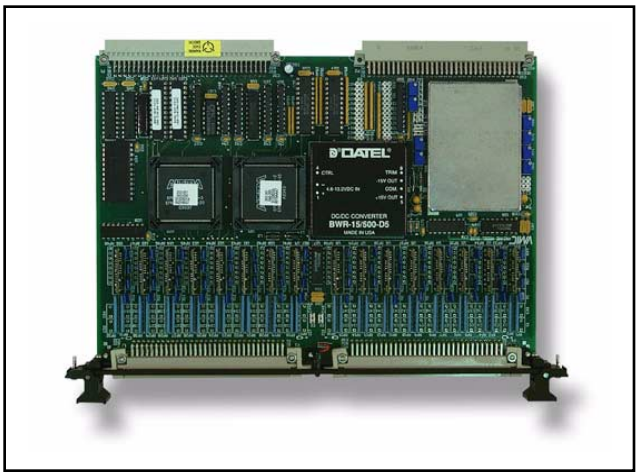
The board supports the following operating modes which are described below:

Trigger Modes
Software Trigger
External Trigger
Interval Timer Trigger

Scan Modes
Autoscan
Single Scan
Random Access

One thousand twenty-four dual-port Data Registers provide storage for continuous scanning of all channels. The trigger and scanning modes are executed automatically at power up, system reset, or are entered under program control. The dual-port registers allow VMEbus access at any time to read the latest stored data.

Channel gain is under software control and can be fixed at x1 or x10 or each channel individually programmed for either gain. Conversion rate is selectable up to 100 kSPS (thousand samples/s) with the high-performance option, and 50 kSPS with the standard performance option. Low pass input filters are available.



A functional block diagram is provided in Figure 1 and the Ordering Options are provided on page 2 of this specification.

FUNCTIONAL CHARACTERISTICS

(At +25 ˚C and rated power supplies, unless otherwise stated.)

Operating Modes:

Trigger Mode:

Software Trigger: The selected scan mode is initiated by writing to the software trigger address.

External Trigger: An external trigger, received on the P2 connector, initiates the selected scan mode.

Interval Timer Trigger: The selected scan mode is initiated each time the programmed time interval expires.

Scan Mode:

Autoscan: This is the default scan mode. All active channels are scanned continuously in sequential order.

Single Scan: A single data burst (scan of all selected channels) is initiated by the selected trigger mode. After all selected channels have been scanned, the scanning process stops and waits for another trigger.

Random Access: A single channel can be selected, digitized, and stored each time the selected trigger mode is enabled.

Channel Autogain: The unique gain code for each channel is loaded from the VMEbus into a gain buffer. The assigned code is retrieved from the buffer in real-time for each channel acquisition.

Ordering Options								
May 8, 2002 800-003122-000 H		A	B	C	–	D	E	F
VMIVME-3122	–				–			

A = Input Filter Option
- 0 = No Filter
- 1 = 10 Hz (-3 dB)
- 2 = 50 Hz (-3 dB)
- 3 = 100 Hz (-3 dB)
- 4 = 500 Hz (-3 dB)

B = Number of Channel Option
- 0 = 64 Channels High Performance
- 1 = 32 Channels High Performance
- 2 = 16 Channels High Performance
- 3 = 64 Channels Standard Performance
- 4 = 32 Channels Standard Performance
- 5 = 16 Channels Standard Performance

C = Input Option
- 0 = Differential Analog Input Channels with 96-pin Nonlatching** Connector
- 1 = Single-Ended Analog Input Channels with 96-pin Nonlatching** Connector
- 2 = Differential Analog Input Channels with 64-pin Latching Connector
- 3 = Single-Ended Analog Input Channels with 64-pin Latching Connector

Connector Data

Style	*Recommended Connecting Component*	*P3 and P4 I/O Connectors*
64-pin IDC	Mating Connector (64-pin)	Panduit 120-964-435
	Strain Relief (For 64-pin Connectors)	Panduit 100-000-072
96-pin Discrete Wire	Mating Connector (96-pin Discrete)	AMP 925486-1
	Female Crimp Contacts (96-pin Discrete)	AMP 530151-6*
	Connector Housing (For 96-pin Connectors)	Harting 09 03 096 0501
96-pin IDC	Mating Connector (96-pin Mass-Terminated)	ERNI 913.031
	0.033-inch Ribbon Cable (96-pin Mass-Terminated)	ERNI 913.049
	Strain Relief Insert (0.033-inch Ribbon Cable)	Harting 09 02 000 9912
	Connector Housing (For 96-pin Connectors)	Harting 09 03 096 0501

PC Board I/O Connector Part Number Panduit 101-096-033A
Panduit is also known as ITW/Pancon.

Notes

*AMP crimp tool part number 90301-2.
** Latches are located on the cable.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

Synchronization: A single scan or burst can be initiated by an external TTL trigger through the P2 connector (External Trigger), or locally through the CSR (Software Trigger). Either event generates a P2 Trigger output, which can be used to synchronize up to 15 boards.

VMEbus Access: Response to address modifiers is jumper selectable as:

A32, A24, or A16 address space
Supervisory or user privilege, or both

VMEbus Compliance: This product complies with VMEbus Specification ANSI/IEEE STD 1014-1987 IEC 821 and 297 with the following mnemonics:

A32/A24/A16:D16/D8 (EO) DTB Slave
Interrupter I(1 to 7) ROAK (DYN)
Interrupter Vector: D08 (O) (DYN)
6U form factor

VMEbus Interrupt: An interrupt request can be generated at the end or middle of a buffer scan. The request can also be initiated after a specific number of samples (1 to 65,535) have been acquired. Response vectors are controlled through Interrupt Vector Registers.

Data Ready Flag: A data ready flag in the CSR is set when the data buffer is filled (endscan) or half-filled (midscan).

Interval Timer: Timed intervals of up to 687 seconds are provided by a programmable interval timer.

Reset Operations: Board reset occurs in response to a system reset or by writing to the Software Reset Address. For programming-free initial operation, a reset operation automatically establishes the following default conditions:

Autoscanning Mode
64-, 32-, or 16-channel block size, depending on option selected
64-, 32-, or 16-channel data buffer, depending on option selected
Channel Gain = x1
Rate = 100 kHz conversion*

The ADC will go through a calibration cycle on either RESET condition. The calibration cycle takes 41 ms after a RESET operation has been initiated.

PGA: Channel gains of x1 and x10 are selected through a Programmable Gain Amplifier (PGA). PGA gain can be software configured for a single gain on all channels, or it can be controlled in real-time with unique gains assigned for each channel.

Panel Indicator: Program-controlled front panel LED is energized during reset, and is extinguished through the CSR.

* The standard performance option can sample at 100 kSPS, but may not convert accurately at rates above 50 kSPS. For the standard performance options, the user must set the sample rate to 50 kSPS or less after reset.

Board Identification: A Board Identification Register (BIR) contains the VMIVME-3122 identification code.

INPUT CHARACTERISTICS

Number of Input Channels: 64, 32, or 16 differential or single-ended channels

Full-Scale A/D Ranges: ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V; jumper selectable

Channel Gain: Software configured for x1 or x10

Full-Scale Input Range: Gain = 1: ±1 to ±10 V Bipolar; 0 to +5 V, 0 to +10 V Unipolar
Gain = 10: ±250 mV to ±1 V Bipolar; 0 to +.5 V Unipolar

Accuracy: Maximum error = ±0.005 percent Reading ± 0.005 percent range ±100 µV

Example: For a +7.000 V reading in the ±10 V range: maximum Error = ±350 µV ±1 mV ±100 µV = ±1.45 mV

Stability: Temperature drift, per degree Celsius = ±10 PPM (ADC reading) plus ±7.5 PPM (ADC range) plus ±2.5 µV

Example: For a +7.000 V reading in the ±10 V range: Temperature drift = ±70 µV ±150 µV ±2.5 µV = ±222.5 µV

Input Noise: (0.4 + 0.3/G)mV; where: G = PGA Gain
Noise is independent of filter option

Input Bias Current: 40 nA maximum at zero input

Input Impedance: 5 MΩ minimum in parallel with 50 pF

Interchannel Crosstalk (DC to 1 kHz):

Option	Adjacent Channel	Alternate* Channel
High Performance (391 to 100 kSPS)	-88 dB	-110 dB
Standard Performance (50 kSPS)	-50 dB	-90 dB
Standard Performance (35 kSPS)	-90 dB	-96 dB

Common-Mode Voltage Range ($IV_{CM}I + IV_{IN}I.G$): ≤10 V

Where: V_{CM} = the common-mode voltage
V_{IN} = the input voltage
G = the gain

*Adjacent channel used as a guard channel.

Common-Mode Rejection: DC to 60 Hz with 350 Ω source imbalance

Gain	Min	Typical
1	90 dB	100 dB
10	100 dB	120 dB

Common-Mode Rejection for the ±2.5 V and 0 to +5 V scale is a minimum of 75 dB. This can be field-trimmed to the same common-mode rejection as the gain of 1.

Overvoltage Protection: ±35 V, sustained
Power On/power Off
±80 V, transient (1 s maximum)

Input Filters: Optional low pass single-pole filters:
-3 dB at 10 Hz
-3 dB at 50 Hz
-3 dB at 100 Hz
-3 dB at 500 Hz

These values apply for differential inputs. Frequency doubles for single-ended (pseudo-differential) applications. The cutoff frequency has a tolerance of ±25 percent. Typical *no filter* input bandwidth (20 Vp-p) is 5 kHz (standard performance) or 40 kHz (high performance).

Common-Mode/Floating Input Protection: On the high-performance option, the low side of each input is pulled to ground through a 22 MΩ resistor. On the standard performance option, the user must control the common-mode voltage and not let inputs float.

TRANSFER CHARACTERISTICS

Resolution: 16 bits

Input Sampling: Sequential, starting at channel 00

Input Transfer Function:

$$E_{IN} = E_{LO} + E_{FSR} \times \frac{N_{ADC}}{65{,}536}$$

Where: E_{IN} = Input Voltage
E_{LO} = Lower End of Input Range
E_{FSR} = Full-Scale Input Range
N_{ADC} = A/D Converter Reading

EXAMPLE: For a N_{ADC} value of D99A HEX (55,706 decimal) in the ±10 V range:

E_{IN} = -10 + [20.000 x (55,706/65,536)] = +7.000

Integral Nonlinearity: ±0.005 percent maximum; from best straight line

Differential Nonlinearity: ±0.0015 percent
No missing codes at 16-bit resolution

A/D Conversion Rate: 381 to 100 kSPS; high-performance option: 381 to 50 kSPS; standard performance option

Channel Sample Rate (Maximum): 100 kSPS (100 kSPS ÷ number of channels in scanning block, 1 channel minimum)

Timed Interval: 305 µs to 687 s

Data Coding: Program selectable as two's complement, or straight/offset binary

DATA BUFFER MEMORY

Buffer Size: 16 to 1,024 contiguous 16-bit data words; program controlled

Block Size: 1, 8, 16, 32, or 64 channels; program controlled

Access Time:

Nonscanning: 600 ns maximum

Scanning: 600 ns typical, 1.2 µs maximum

Maximum access time in scanning mode will occur only when VMEbus access occurs in ADC sample window.

VMEbus Access: D8 or D16

Availability: Accessible at any time from the VMEbus. Buffer and block sizes are controlled through a Configuration Control Register (CCR).

PHYSICAL/ENVIRONMENTAL

Temperature: 0 to +65 ˚C (standard VME slot), operating; -40 to +85 ˚C, storage

Humidity: 0 to 80 percent relative, noncondensing

Altitude: Operation to 3,000 m

Cooling: Forced air convection (standard VME slot)

Dimensions: Double height Eurocard (6U) board, 160 x 233.35 mm

Weight: 700 g, maximum

Input Connectors (P3, P4): Input connectors P3 and P4 may be ordered as either 96-pin DIN nonlatching or 64-pin DIN latching. The 96-pin nonlatching connectors offer the center row as ground, while the center row ground is not available on the 64-pin latching connector. When using the 64-pin latching connectors in differential mode, the user may jumper E1 and E2 to provide ground on the front panel, this will result in configuring channels 31 and 63 as single-ended. See the Ordering Options "C" input options.

Power Requirements: 7.0 A (maximum) at +5 VDC

MTBF: 135,900 hours (217F)

UIOC® SUPPORT — In a UIOC, the VMIVME-3122 is used as a monitoring device. During initialization, the UIOC programs the VMIVME-3122 to scan all 64 channels and sets the scan mode to Autoscan. Through UCLIO™ language, the user may set programmable channel gains and command the UIOC to acquire data from any or all of the VMIVME-3122 channels. Through a menu-driven calibration process, the user may create and store channel gain and offset correction factors which are automatically used by the UIOC to provide software gain and offset corrections for each channel.

COMPATIBLE SIGNAL CONDITIONING BOARDS

VMIVME-3417A 16-Channel Isolated Signal Conditioning Board with Optional Current Loop Termination. The VMIVME-3417A provides full-scale input ranges from ±5 mV to ±10 V. Two-pole low pass input filters are available with cutoff frequencies of 4, 40, or 400 Hz. Optional current loop termination input resistors are available, and replace the input filter. See Figure 2 for a typical system implementation of the VMIVME-3417A.

VMIVME-3418 8-Channel Strain Gauge and RTD Isolated Signal Conditioning Board. The VMIVME-3418 provides full-scale input ranges from ±5 mV to ±10 V. Low pass input filters are available with cutoff frequencies of 4, 40, or 400 Hz. See Figure 3 for a typical system implementation of the VMIVME-3418.

VMIVME-3419 32-Channel Signal Conditioning Board with Programmable Gain and Built-in-Test (BIT). The VMIVME-3419 accepts full-scale input ranges from ±5 mV to ±10 V, depending on the gain selected for the A/D board. Low pass filters are available with cutoff frequencies of 4, 40, 400, or 4 kHz. Optional current loop termination input resistors are available. See Figure 4 for a typical system implementation of the VMIVME-3419.

TRADEMARKS

UCLIO is a trademark and UIOC and the VMIC logo are registered trademarks of VMIC. Other registered trademarks are the property of their respective owners.

APPLICATION AND CONFIGURATION GUIDE — The following Application and Configuration Guide is available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

Title	Document No.
Connector and I/O Cable Application Guide	825-000000-006

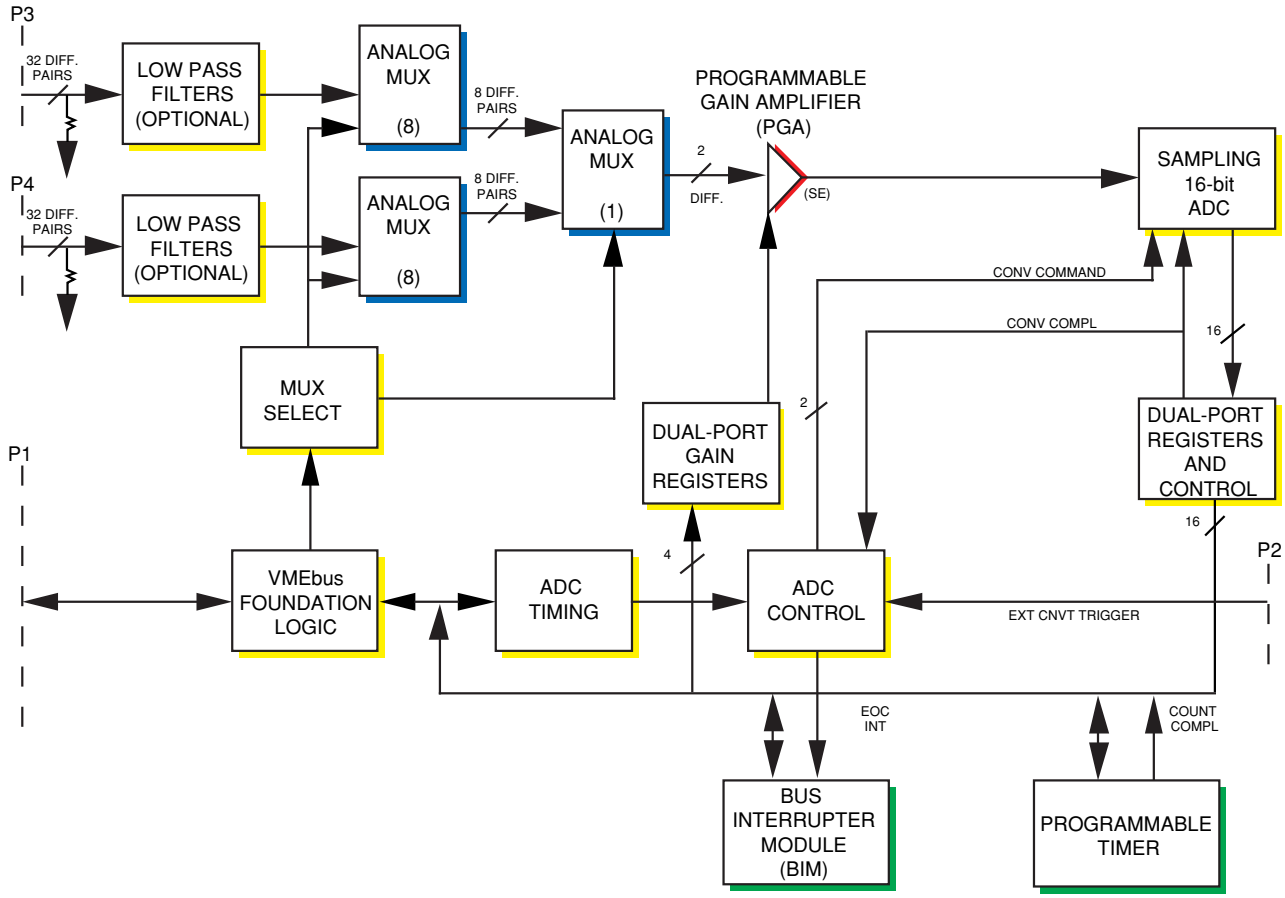


Figure 1. VMIVME-3122 Functional Block Diagram

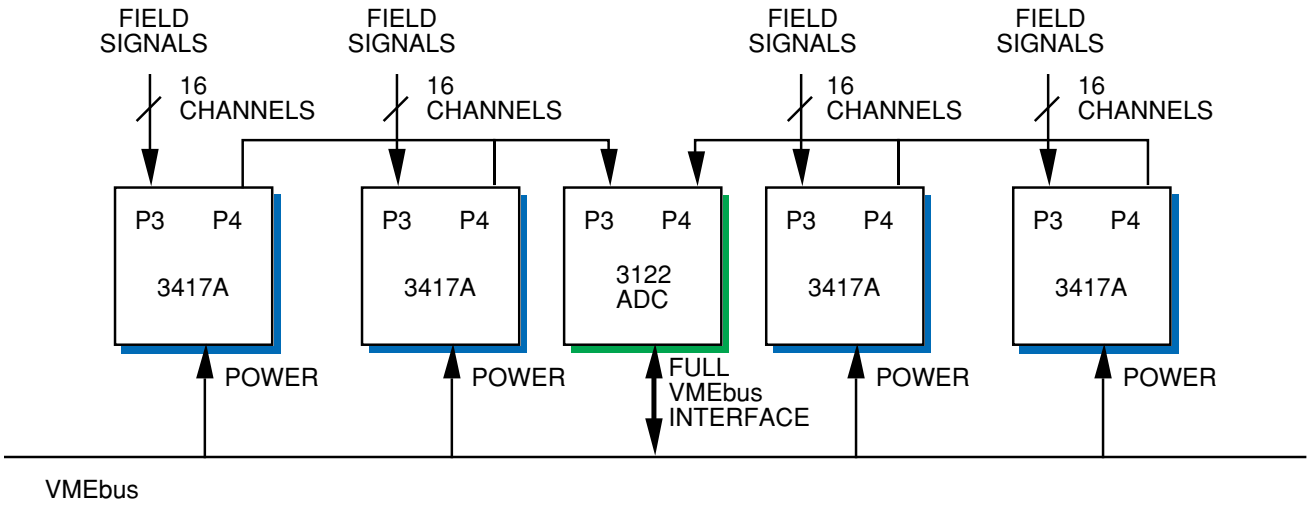


Figure 2. Typical System Implementation Using VMIVME-3122 with VMIVME-3417A

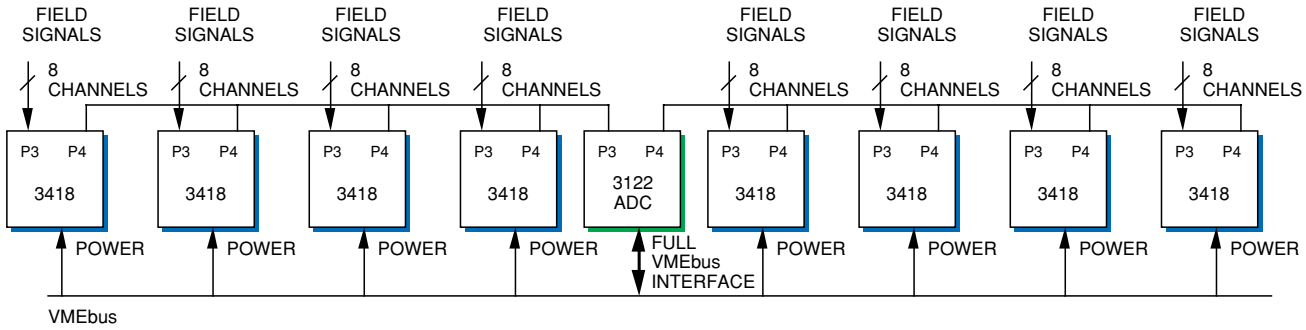


Figure 3. Typical System Implementation Using VMIVME-3122 with VMIVME-3418

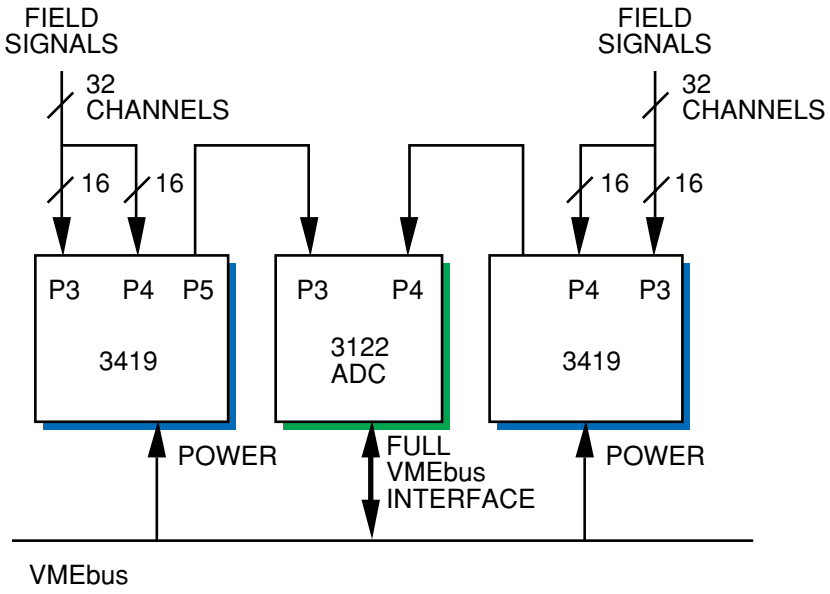


Figure 4. Typical System Implementation Using VMIVME-3122 with VMIVME-3419