Electronics update at ps Timing WS

Session (B) Picosecond Read-Out Electronics Chain

11:40-12:00 *TDC130: High performance Time to Digital Converter in 130 nm*
Christian Mester (CERN)
PPT

12:10-12:25 *Proposed Planicon Anode Design for Fast-Sampling Read-Out*
Fukun Tang (UChicago)
PPT

Posted file has problem

1:30-1:50 *Status and Plans of the Buffered LABRADOR (BLAB) ASICs*
Gary Varner (UHawaii)
PPT

2:00-2:20 *Fast analog memories at Saclay/(Orsay)*
Erik Delagnes (Saclay)
PPT

2:30-2:50 *A Fast Sampling Chip for Picosecond Detectors*
Jean-Francois Genat (IN2P3/UC)
PPT

Simulation only

3:00-3:20 *System Considerations in picosecond timing systems*
Gary Drake (ANL)
PPT

3:30-3:50 *The 10-ps Wavelet TDC:--Improving FPGA TDC Resolution Beyond Its Cell Delay*
Jinyuan Wu (FNAL)
PPT

Don’t understand

4:00-4:10 *Comments on What Have been Heard So Far*
Keith Jenkins (IBM)
PPT

TDC130: High performance Time to Digital Converter in 130 nm

Christian MESTER

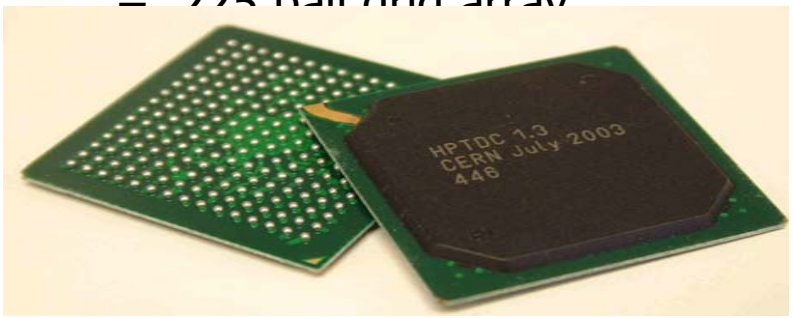
2008-03-27

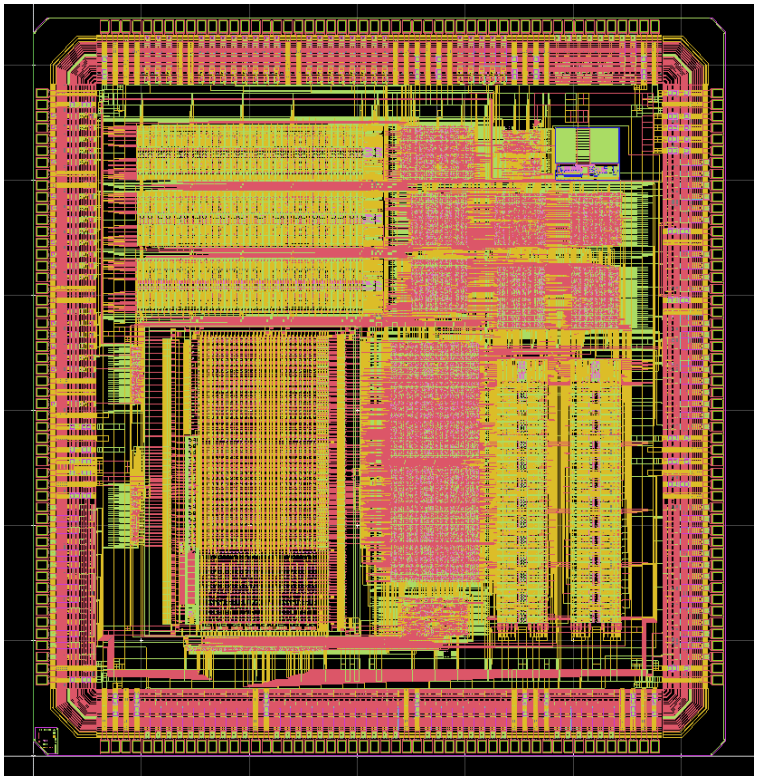
Index

- Introduction:
  - What is a TDC and its use
  - Application example
  - HPTDC implementation
- New TDC130
  - Expected resolution
  - Current state
  - Architecture
  - Focus on DLL
  - Ideas for further improvement of resolution

Current Implementation (HPTDC)

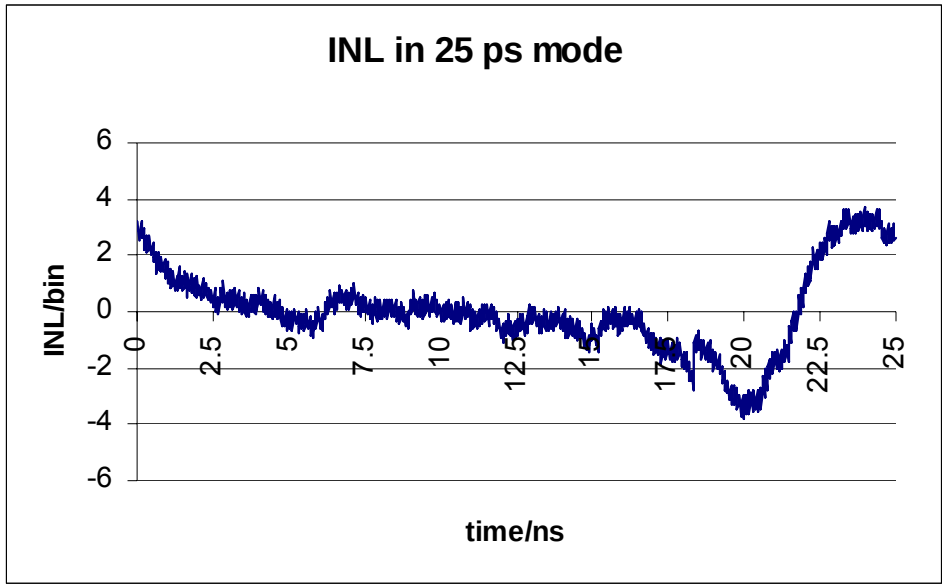
- DLL, hit registers, RC delay
  and PLL implemented as full custom
- 0.25 µm CMOS technology
- 6.5 x 6.5 mm²
- ≈ 1 million transistors
- 225 ball grid array

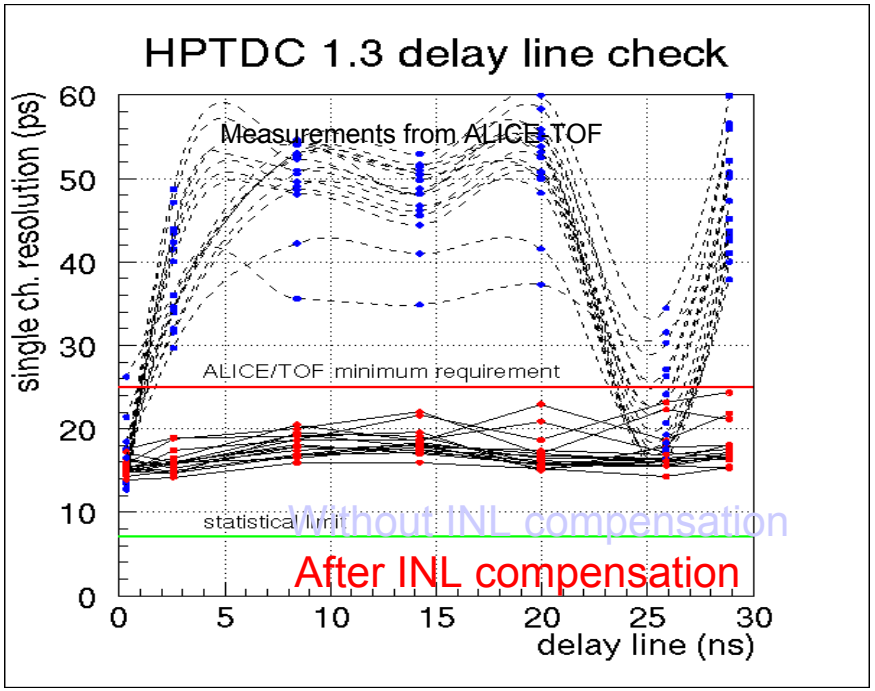




Measurement of HPTDC: INL correction

- Effective RMS resolution:
  - 40 ps without INL correction
  - 17 ps with look-up table INL correction (as a fixed 40 MHz pattern has been observed)





How to improve the resolution?

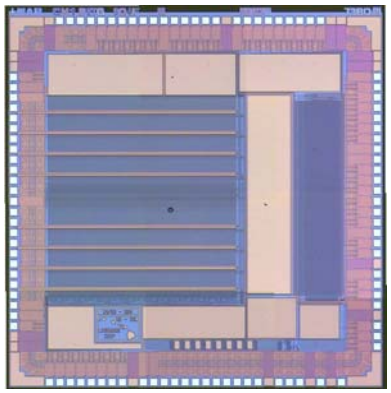
- HPTDC's very high resolution mode:
  - Interpolation using R-C delay elements and 4 normal channels per very high resolution channel
    (→ only 8 instead of 32 channels available in very high resolution mode)
- TDC130:
  - Interpolation — without reducing the number of channels?
  - Ideas:
    - R-C networks: attenuation, low pass: slew rate deteriorates
    - Transmission lines: potentially long, less attenuation
    - Delay elements (like in the DLL)
      - Use a second DLL with slightly less (e.g. 26) delay elements than the main DLL
      - Let the clock signal propagate in both DLLs
      - Distribute the second DLL's control voltage to delay elements in the channels
  - Interpolation factor 4 → ≈6 ps bin size

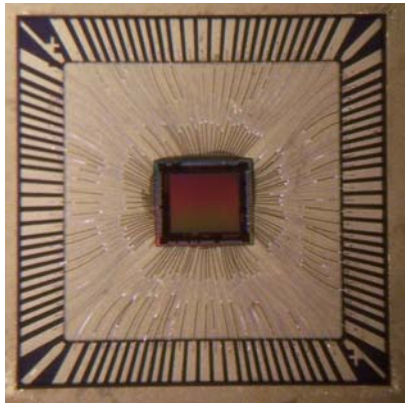
TDC130: Outlook

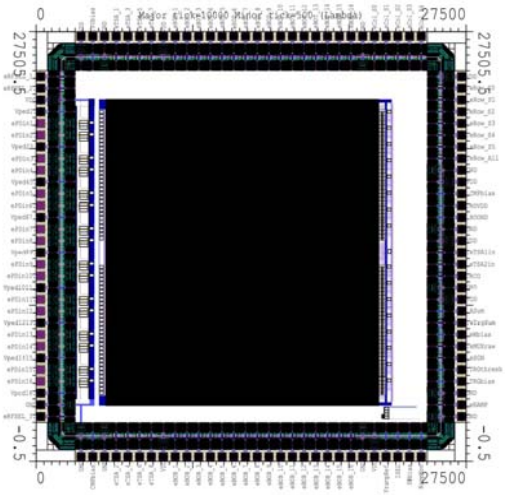
- Final chip
  - General architecture (channel organization, 1 buffer per channel) fixed
  - Will support triggered mode
  - Readout: to be discussed

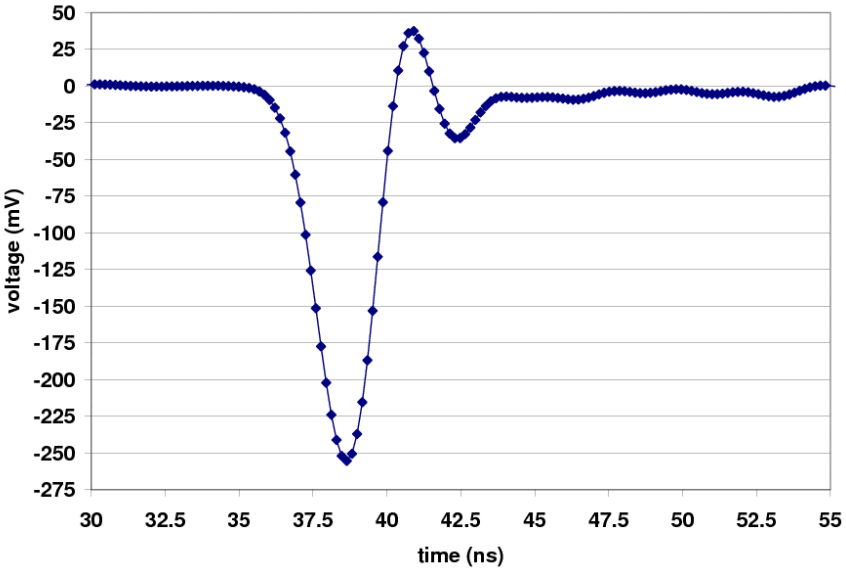
- Future of the development
  - "Client" expectations
  - "Client" involvement
  - "Availability" of manpower
  - "Maintain" expertise

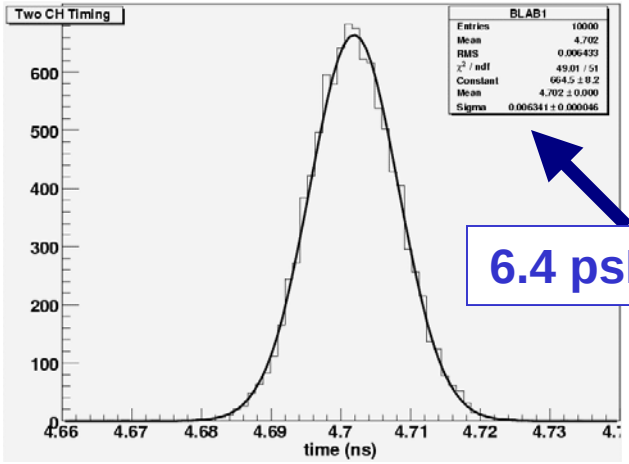
Status and Plans of the Buffered LABRADOR (BLAB) ASICs





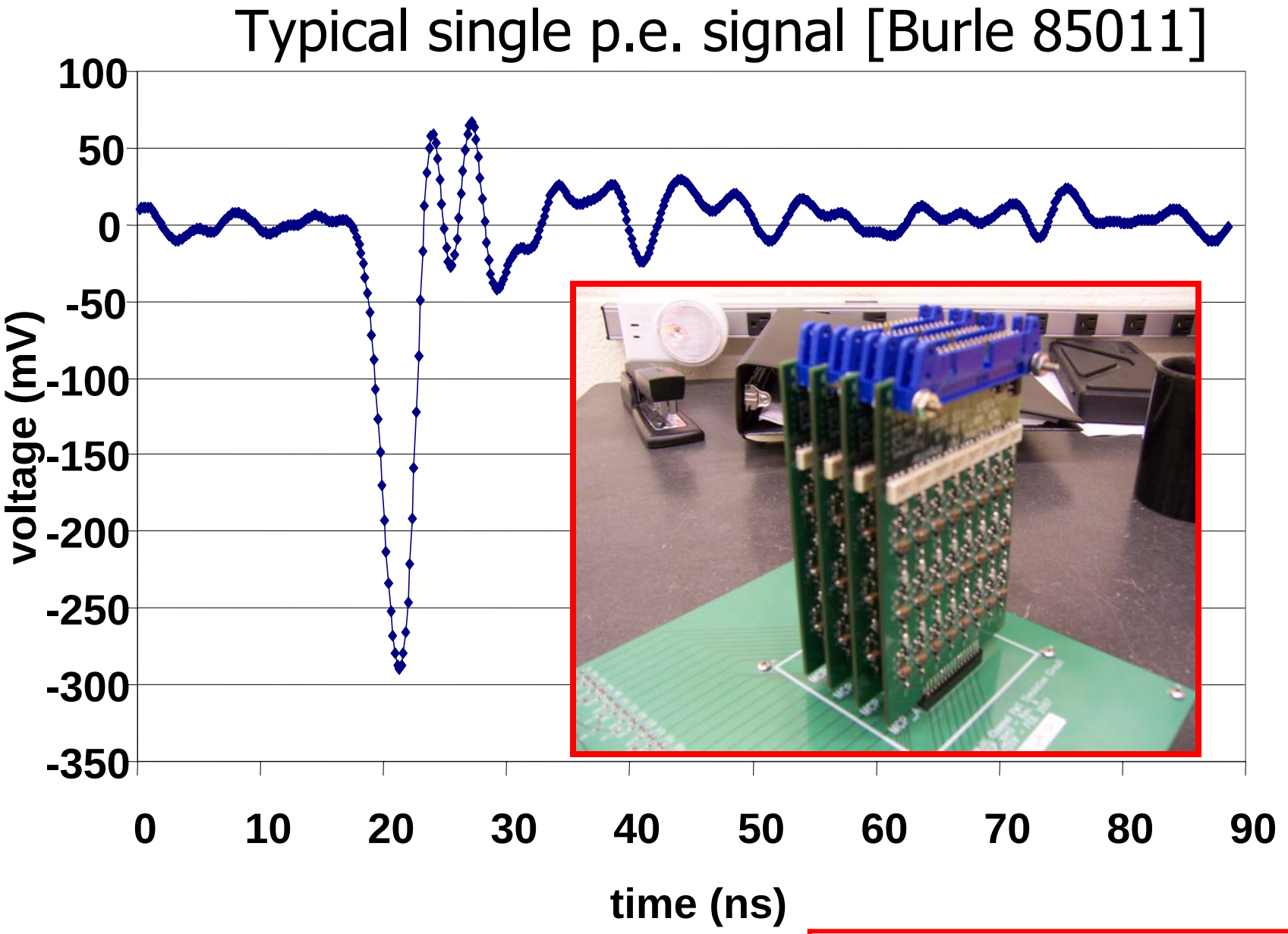






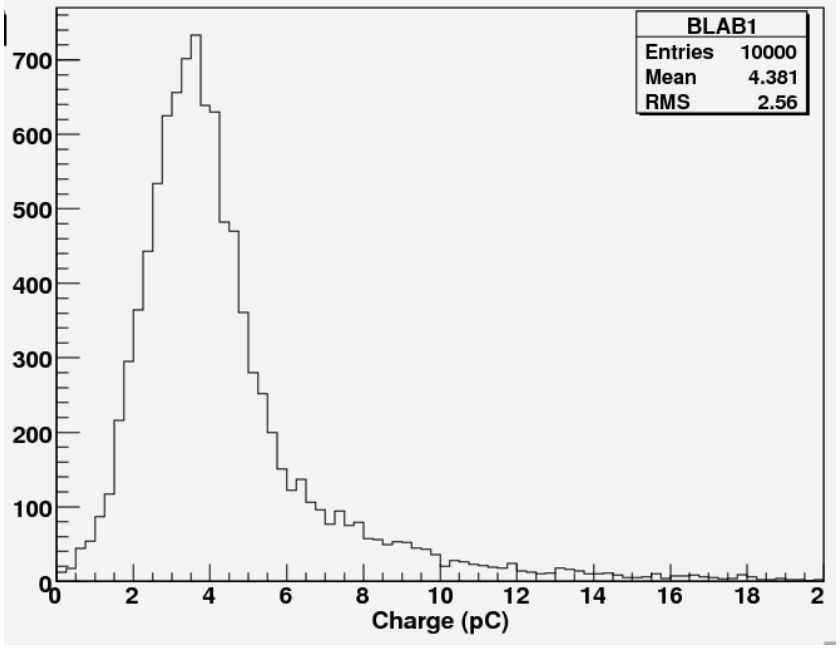
Gary S. Varner
University of Hawaii

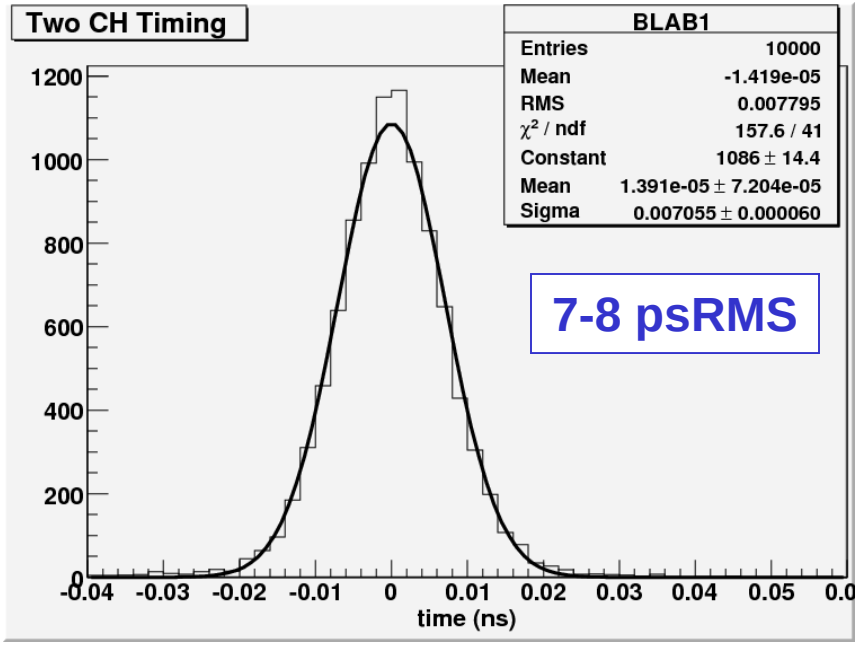
ps Timing Workshop, March 2008



Using RF Amplifier System
(~43dB gain)

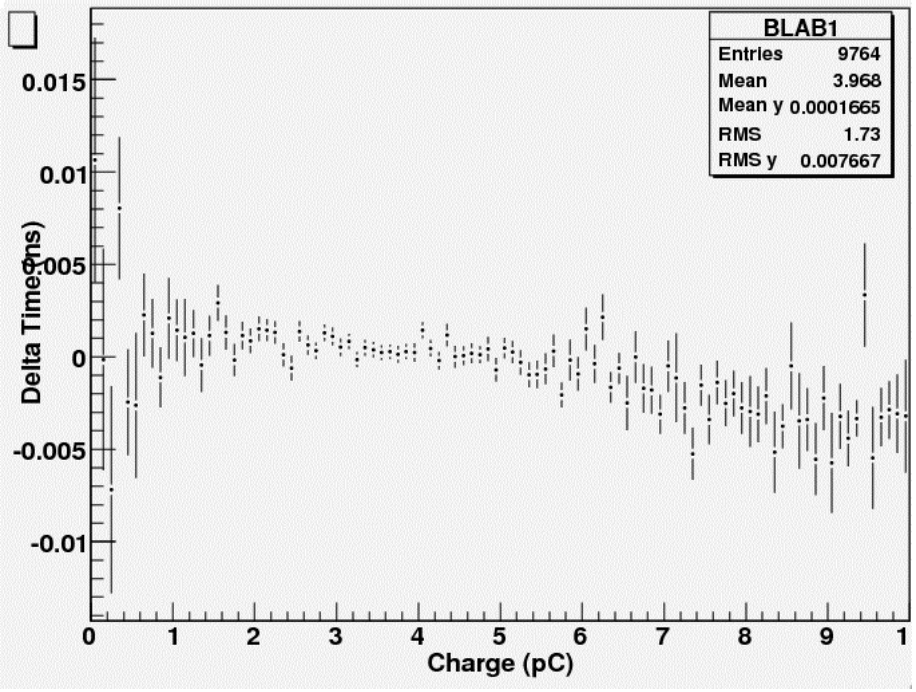
Real MCP-PMT Signals





7-8 psRMS

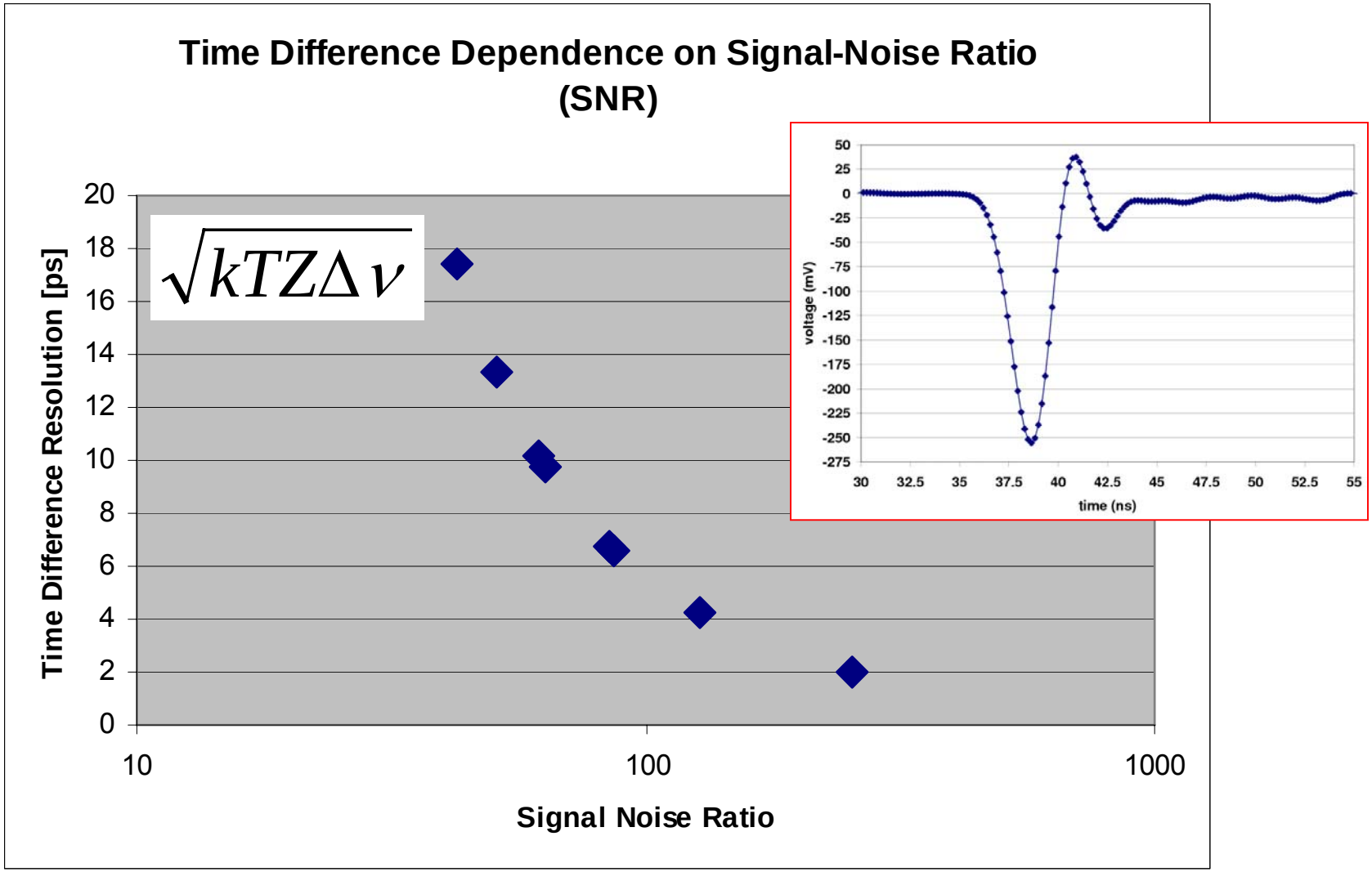
Residual Time Walk



Rather robust for amplitude invariant signals,
TOF still hard, but can shape extract

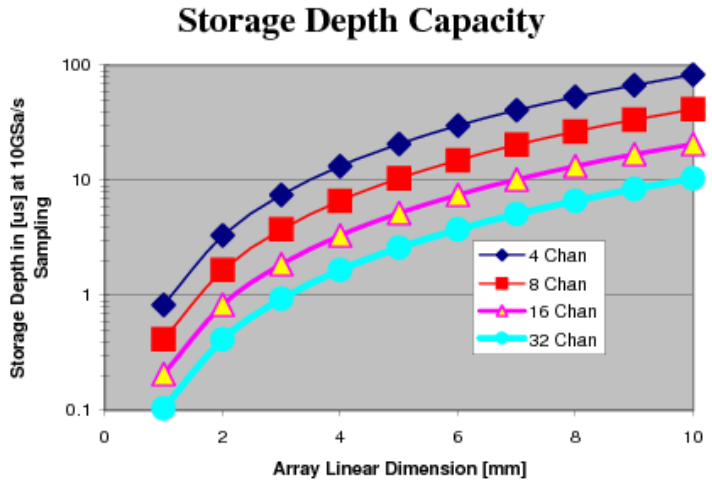
Simulated Performance vs. SNR

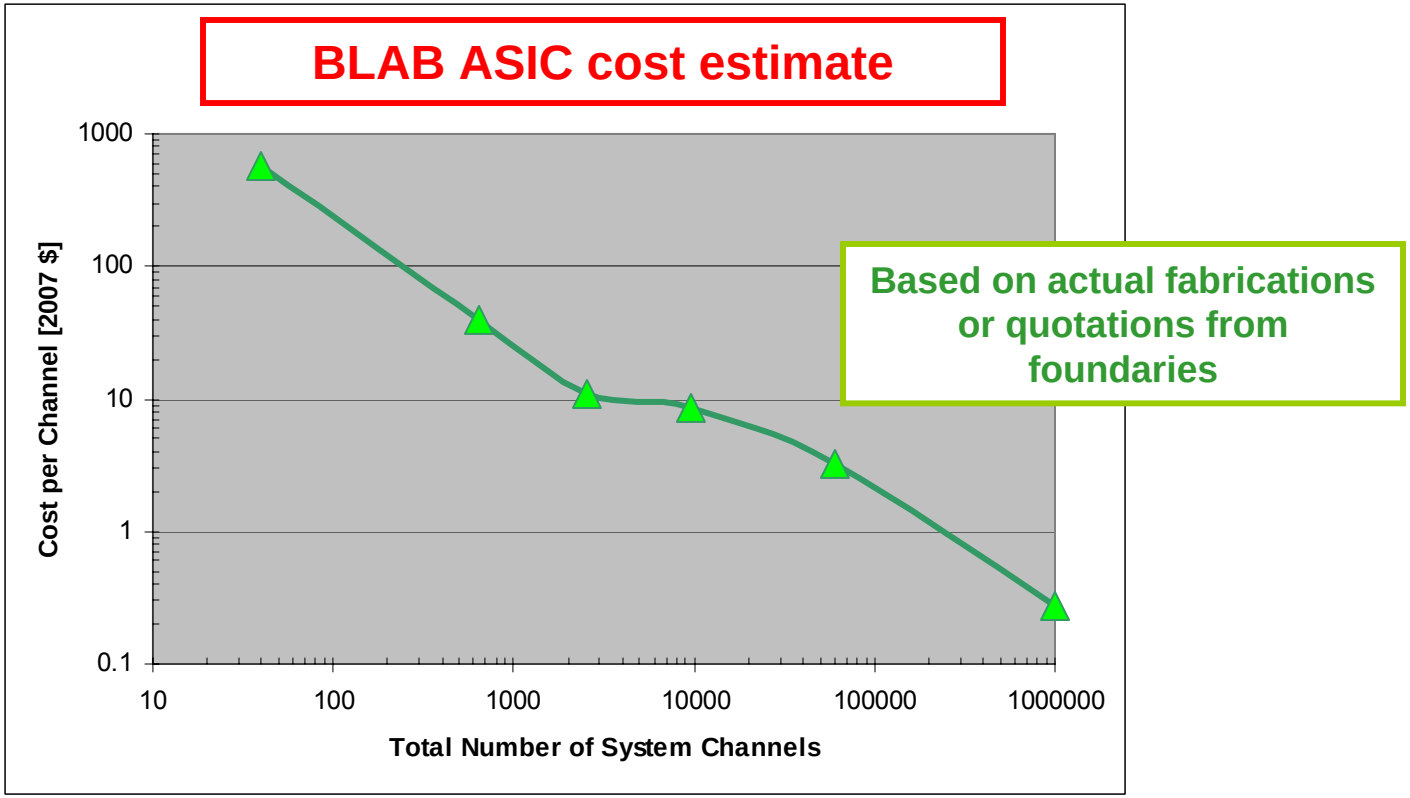
300MHz ABW, 5.9GSa/s



BLAB2 Density and Cost

- 16 input channels
- For large-scale systems, cost very competetive





Fast analog memories at Saclay/(Orsay)

eric.delagnes@cea.fr

Fast Analog Memories in DAPNIA

AFTER : 05-06
TPC of T2K
72 ch/ 512 pts
Fe= 1-50 Mhz,BP = 10 Mhz
Dyn= 10 bits
AMS0.35 µm.
Also includes FE.
500k transitors

ARS0 : 97-98
ANTARES/HESS1
5 ch/ 128 pts

Fe= 1Gs/S
BP = 80 Mhz
Dyn~8-9bits
AMS 0.8 µm

ARS1 : 98-04
ANTARES
4 Ch
system on chip
including ARS0

HAMAC : 93-97
Calo ATLAS
12 canaux/ 144 pts
Fe= 40 Mhz
BP = 10 Mhz
Dyn= 13,6 bits
DMILL **0.8 µm**

SAM 04-05
HESS2
2 ch / 256 pts
Fe= 50 MHz-2GHz
BP = 300 Mhz
Dyn= 12 bits
AMS 0.35 µm

MATACQ : 99-01

Matrix Structure
1 ch, 2560 pts
Fe= 50 MHz-2GHz
BP = 300 Mhz
Dyn= 12 bits
AMS **0.8 µm**
(PATENT)

PIPELINE : 01- 02
METRIX
1 ch
System on chip integrating
1 MATACQ

Collaborations with l' IN2P3/ LAL

Futur

New Architectures

KM3Net

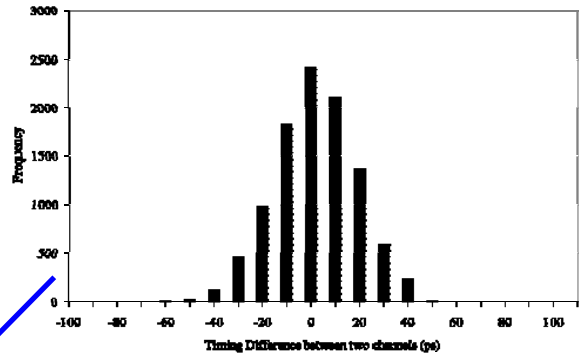
CTA

Continuous Sampler

FastSampler
Fs~ 5-10GHz ,
BW>600MHz
>5000 pts ?
DSM technology

MATACQ: performances and applications.

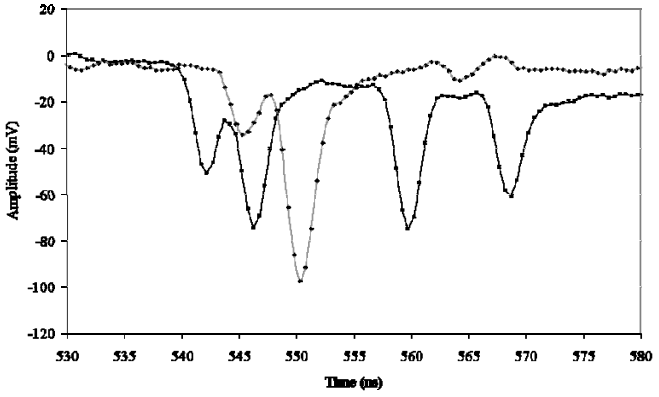
NAME	Quantity	Unit
Input impedance	50	Ohm
Dynamic range	+ / - 1	V
Digitization LSB	125	µV
Noise	<180	µV rms
Signal / Noise	13.4	Bits Rms
Analog bandwidth	300	MHz
Harmonic distorsion for a 10 MHz input signal	< -65	dB
Integral non linearity	<1	LSB
Differential Non linearity	<0.5	per mil
Sampling frequency	50 to 2000	Msample/s
Channel to channel jitter	<20	ps rms
Trigger chain jitter	<50	ps rms
Overall jitter	<60	ps rms



without any correction

Applications:

- Neutron TOF measurements on a 160 channel Micromegas detectors (DEMIN).
- Test of PMT @ IN2P3/IPNO
- Serie-Test of the ATLAS LARG Board, Digitization in CAST (CERN
- Timing on Chimera.
- ….



DEMIN: ~50ps rms. Fs= 2 GHz 12 bits
M. Houry et al, NIMA A 557 (2006) 648–656

Funding from "P2I" for a generic R&D on fast SCA with LAL .

At least 2 projects among these three. Priorities to define:

- 10 GS/s range, "small" depth (<256 samples) Sampler:
  - 7 GS/s reached in simul. with AMS 0.35µm => proto ?
  - waiting for availability of AMS 0.18µm to make a real chip.
  - No clear interest of Saclay physicists (or of CAEN) !
  - Main Issue: input BW: 50 Ohm x 5 pF => 640 MHz.
    - input buffer impossible.
    - need low Zin.
    - Pb of impedance matching inside the chip ?
- Very large depth sampler 2-5GS/s (50000 or more samples)
- Continuous sampler.

Summary of Sampler ASICs

	G. Varner					Delagnes/Breton					S.Ritt
	Hawaii					Saclay/Orsay					PSI
		Blab1	Lab1-2	Lab 3	Planned BLAB2		Hamac	Matacq	Sam	Planned	
Sampling		100 MHz-6 GHz		20 MHz-3.7 GHz	1 - 10 GSa/s		40 MHz	0.7-2.5 GHz	0.7-2.5 GHz	10 GHz	
Analog bandwidth (3db)		300 MHz		900 MHz	850 MHz		50 MHz	200-300 MHz	300 MHz	650 MHz	
Channels		1	8	9	16		8	1	2		
Triggered mode		Yes		Common stop				Yes			
Resolution		10 bit			10 bit		13.3 bit	13.4 bit	11.6 bit		
Samples		128 rows of 512	256	256	4/8 rows of 512		144	2520	256	2048	
Clock				33 MHz			40 MHz	100 MHz			
Max latency		560 us	2.2ms	50us							
Input Buffers		Yes			TIA (5kOhm)		Yes	Yes	Yes	No	
Differential inputs		No	No	No	Pseudo-diff		Yes	Yes	Yes		
Input impedance		50 Ohms	50 Ohms	50 Ohms Ext	30-70 Ohm adj.		10 MOhm/3pF	50 Ohms			
Readout clock		n/a			1 GHz (Wilk clk)		5 MHz	5 MHz	16 MHz		
Readout time		10ms (12-b)		150ms	512us		3ms	650ms			
Locked delays		Ext DAC	Ext DAC	Ext DAC	Ext DLL				Yes		
On-chip ADC		1 GHz (Wilk clk)			1 GHz (Wilk clk)		No		No		
R/W simultaneous		Yes			Yes		Yes		No		
Power/ch		15mW/sample 1.6W/read			20mW (200mW/r)		36 mW	250-500 mW	150 mW		
Dynamic range		1mV/1V			1mV/1V		0.26mV/2.75V	175 uV-2V	0.65mV-2 V		
Xtalk		Inter-rows 0.1%		10%	<0.1%				0.30%		
Sampling jitter		<10ps			TBD		45ps	60ps	40ps		
Power supplies		2.5	2.5V	2.5V	2.5V		-1.7/3.3V				
Process		TSMC 0.25	TSMC 0.25	TSMC 0.25	TSMC 0.25		HP/DMILL 0.8	AMS 0.8	AMS 0.35	AMS 0.18	
Die area		10 mm2	9.8 mm2	10 mm2	12 mm2		19.8mm2	30mm2			
Reset		No									
Temp coeff		0.2%/◦C		0.2%/◦C							
Cost/channel		500$/40 10$/2k			500$/40 10$/2k						

System Considerations in picosecond timing systems

Clock Distribution and Readout

John Anderson
HEP Electronics Group
Argonne National Laboratory

Presented by Gary Drake

CDCE62005 Pico BTS/Data Com Clock

3:5 Frequency Synthesizer/Jitter Cleaner

Features

- Input frequencies from 3MHz to 500MHz
- Crystal Inputs from 2MHz to 42MHz
- Output frequencies from 4.25MHz to 1.175GHz
- Output up to 5 LVPECL/5 LVDS/10 LVCMOS
- Individual phase adjust
- Optional high swing LVPECL mode
- Wide-range integer divide selectable by output
- **Low output skew (~ 20ps, typ)**
- Integrated/External PLL Loop Filter
- **Low jitter (< 1ps RMS)**
- On-chip EEPROM

Benefits

- Fully Integrated twin VCOs support wide output frequency range
- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- Integrated/external loop filter provides flexibility
- EEPROM saves default start-up settings
- SPI interface provides in-system programming
- QFN-48 package, Tem -40 to 85 C

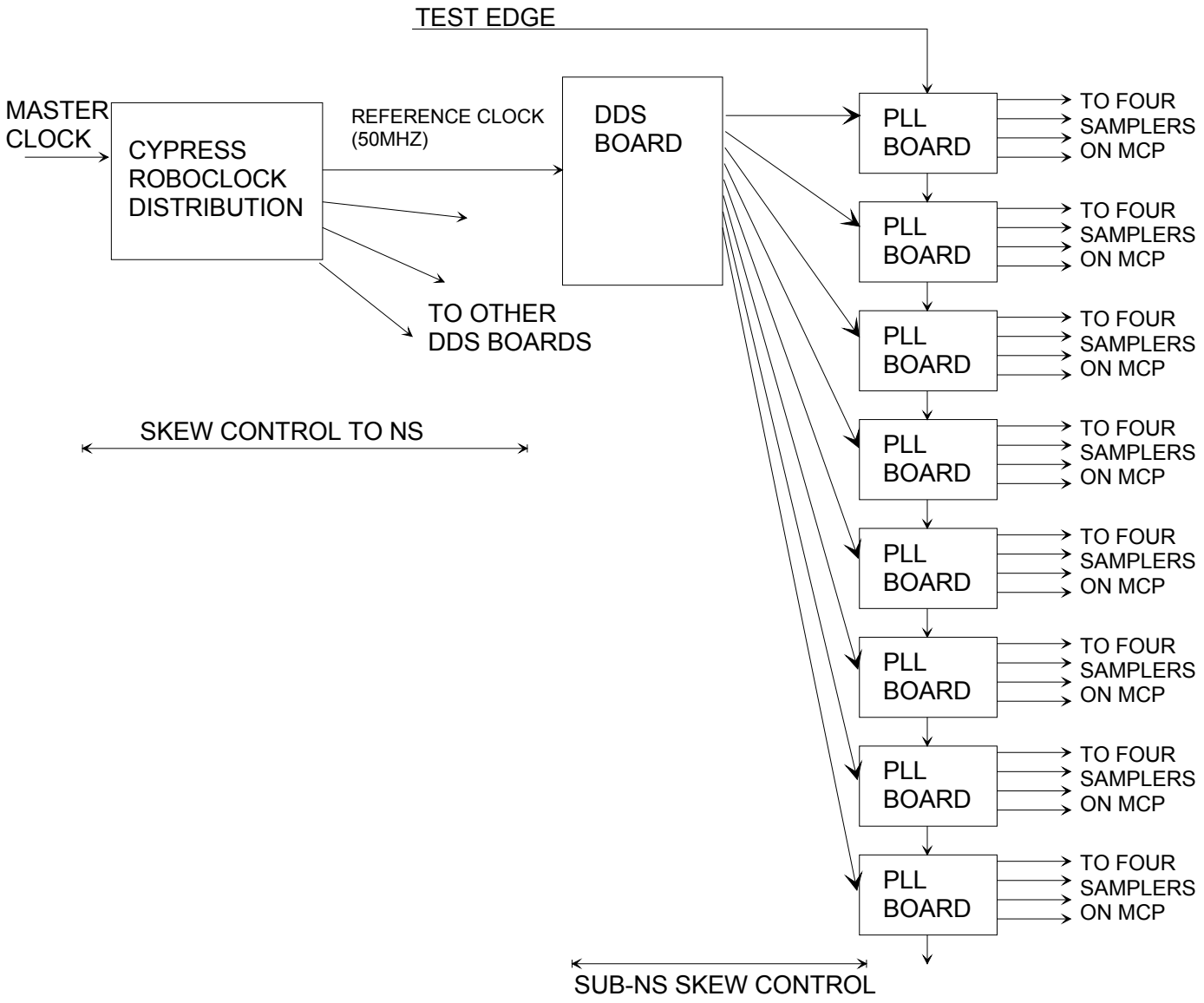
Applications

- Wireless BTS
  (Pico, WiMax cells, Macro Base band)
- Data Communications
- Medical
- Test Equipment
- Jitter Cleaners

Oct/07 Sampling

May/08 In Production

Clock Distribution System



System Calibration and Readout

- Skew between clocks controlled by combination of coarse skew and fine phase adjustment in Roboclock and DDS boards
- Control skew between MCP channels by careful routing
- Use a fifth digitizer in each PLL board to sample a test pulse that is routed using only known cable delay (single terminator at end).
  - Assume fifth digitizer is phase-locked to the four MCP digitizers of each PLL board
  - Set clock skew so that each digitizer measures the test pulse at a delay consistent with the fixed cable delays in the system
  - Where applicable cross-check with a point optical source that has equidistant path to all MCPs
- Coarse timing and event timestamping provided by FPGAs
- FPGAs collect data from the four digitizers and handle readout
- Use bi-directional SERDES links (e.g. DS92LV18) to provide control and data path unique to each FPGA

Keith Jenkins (IBM) Summary

- CMOS capable of very precise timing
  - Jitter stage-stage of few fs possible
  - Ps level timing routine in high-performance digital circuits
- Continued custom TDC development important
  - Ps level useful
  - Compact
- 40GSa/s ADC in CMOS difficult
  - Bi-CMOS may be better
- On-chip calibration
  - Necessity
  - Not a lot of overhead

My Summary

- General agreement that WFS technique promising
  - Can deal with many, unknown effects
  - Absolutely zero progress on better discriminators
- Precision TDC
  - Can do better
  - In order to realize, need a system design
- Electronics overall
  - Won’t dominate cost
  - Photodetector limit performance