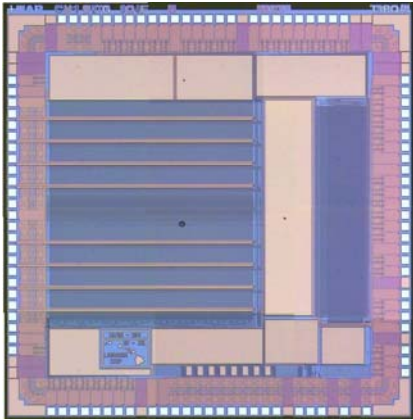
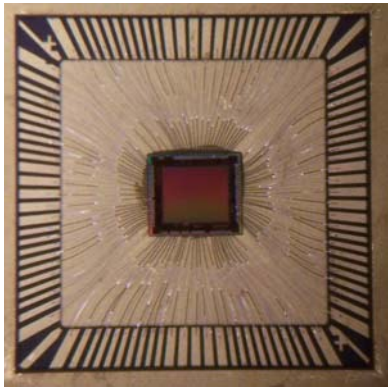


BLAB2 ASIC plans



- BLAB2 ASIC
 - Design specifications, simulation
 - Compact readout system [already covered]
- Upcoming beam test options discussion
 - TOF (2+1 channel) readout module
 - Simple MPPC test bench (March?)
 - SLAC ESA (Sept?)



Larry Ruckman, Gary S. Varner (Univ. of Hawai'i)

Ke Wang (IHEP, Beijing)

SLAC PID Meeting 1-FEB-08



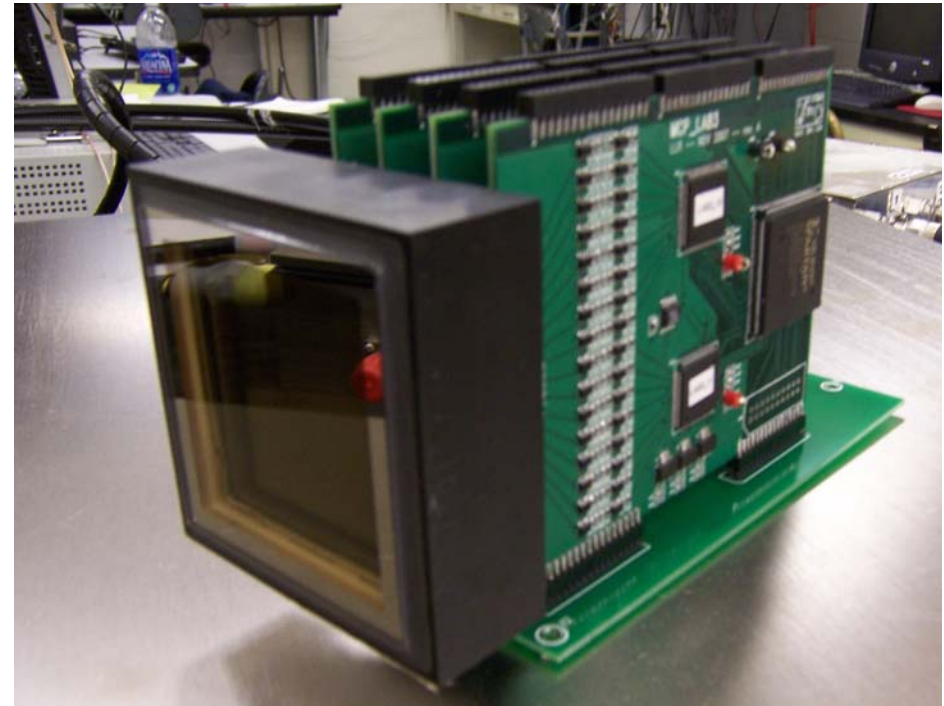
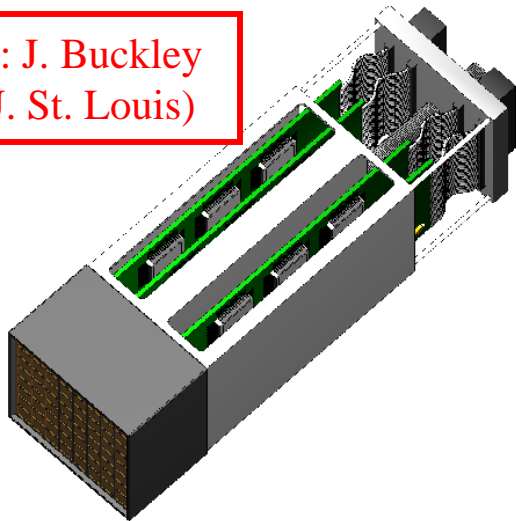
BLAB2

- **Initial Target: New f-DIRC/f-TOP Readout System**

TABLE II: *BLAB2 ASIC Specifications.*

<i>Item</i>	<i>Value</i>
Photodetector Input Channels	16
Linear sampling arrays/channel	2
Storage cells/linear array	512
Sampling speed (Giga-samples/s)	2.0 - 10.0
Outputs (Wilkinson)	32

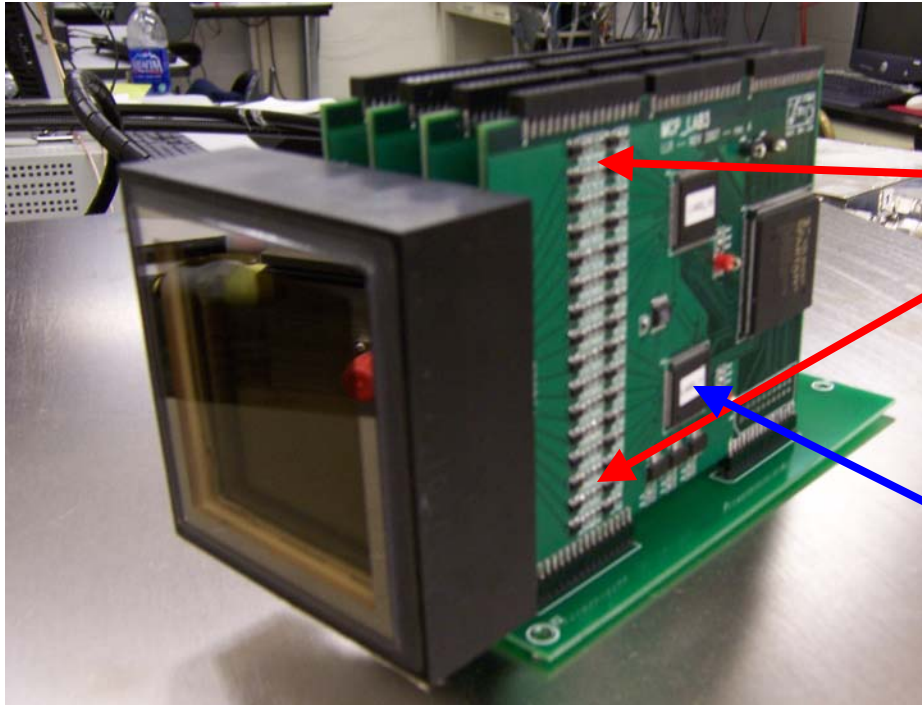
Courtesy: J. Buckley
(Wash U. St. Louis)



Gen. 0 Prototype (LAB3)

Target Submission: Feb. 11, 2008 → Apr. 4

Gain Needed



Amplifiers dominate board space

Readout ASIC tiny (14x14mm for 16 channels)

- What gain needed?
 - At 10^6 gain, each p.e. = 160 fC
 - At 2×10^5 gain (better for aging), each p.e. = 32 fC
 - In typical ~ 5 ns pulse, $V_{\text{peak}} = dQ/dt * R = 32 \mu\text{A} * R = 32 \text{mV} * R [\text{k}\Omega]$ (6.4mV)

Gain Estimate	
Rterm	1 p.e. peak
50	1mV
1k	20mV
20k	400mV

RGC_TIA Circuit

Power : about 17mW/ch
BW : 2pf input 2pf output : 867 MHz
4pf input 2pf output : 768 MHz
Input Impedance : 34ohm
Transimpedance : 5K
Max Input cu50uA
Output range : about 0.65-1.7

Optimized
BW : 2pf input 2pf output : 920 MHz
2pf input 1pf output : 1.05GHz

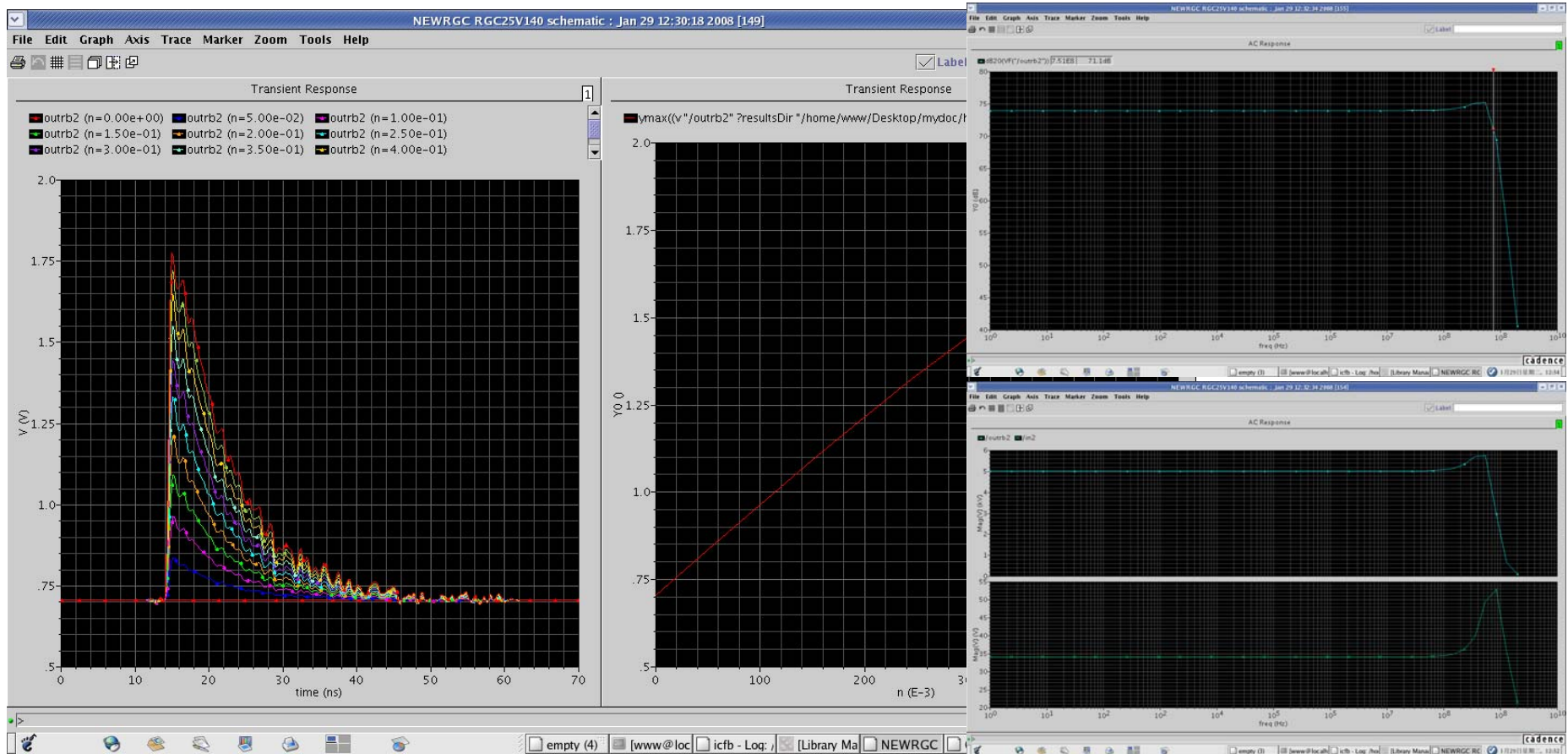
Ke Wang (IHEP)

The schematic shows a differential input stage with NMOS transistors (NM54, NM56, NM57, NM58) and PMOS transistors (PM53, PM54, PM55, PM56). It includes a feedback network with resistors (R18, R19, R20, R21, R22) and capacitors (C19, C20, C21). The circuit is powered by VDD and VSS, and includes a current source (V26) and a load resistor (R23). The output is taken from the differential nodes (outb2, outb1) and is connected to a load (V27).

mouse L: schSingleSelectPt() M: schHiMousePopUp() R: schZoomFit(1.0 0.9)

www@loc: icfb - Log: [文件浏览] Library Ma Virtuoso®: Virtuoso®, 1月30日星期三, 23:10

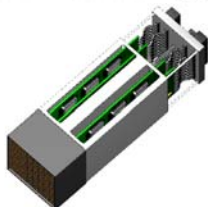
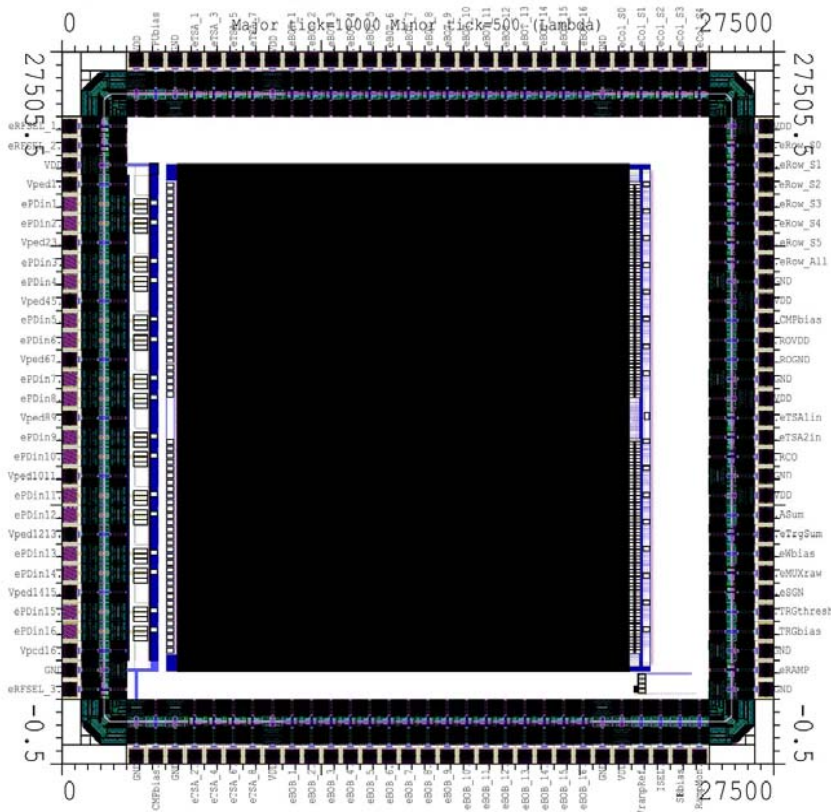
Simulated Performance



- Meets specs on previous slide
- $5k \rightarrow \sim 100mV$
- Sample noise $\sim 1mV$, if match input noise: $6pA/\sqrt{Hz}$
- SNR is then 100:1

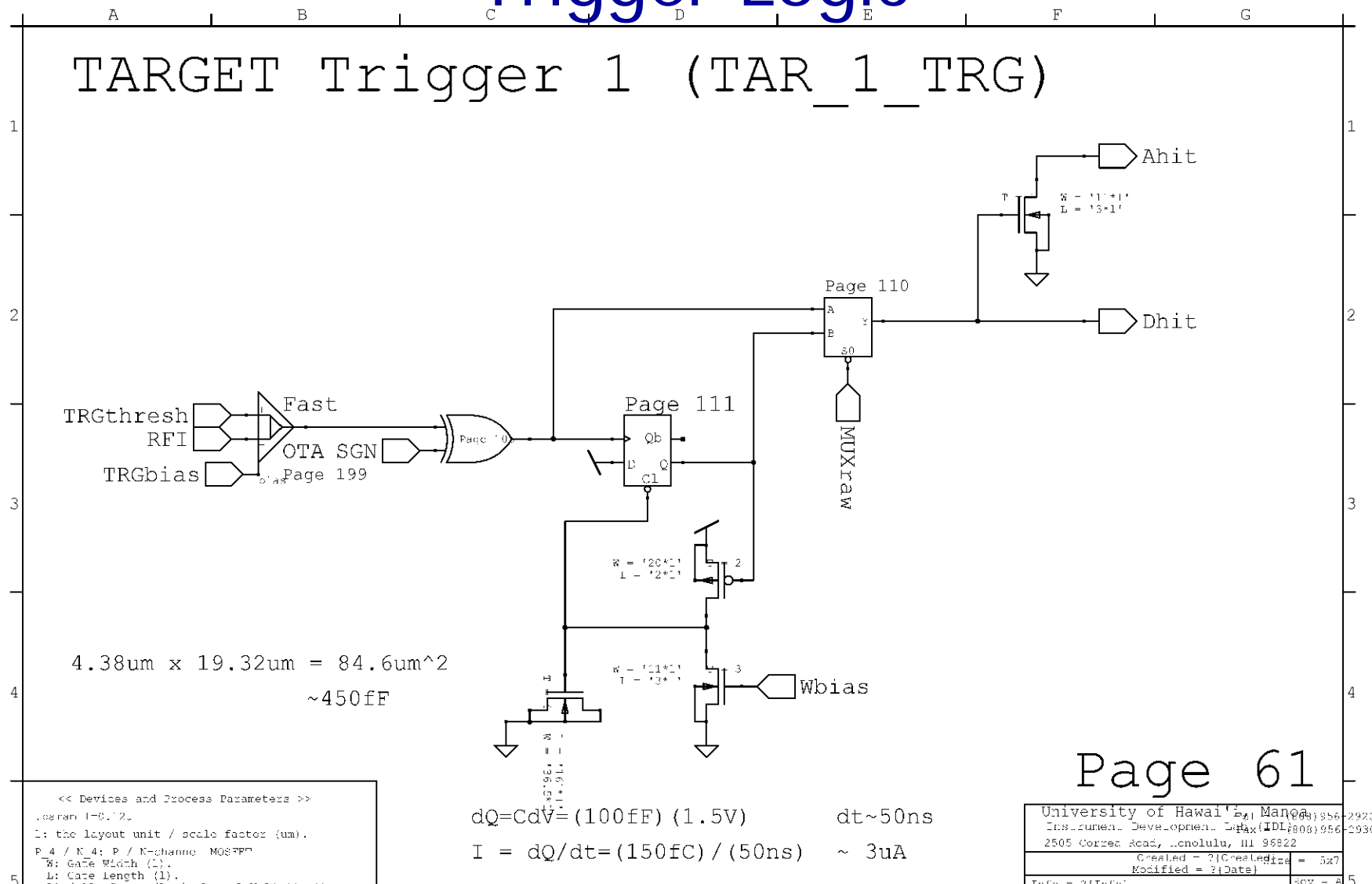
Triggering Capability

Could be incorporated – already doing so for TeV- γ application prototype (TARGET)



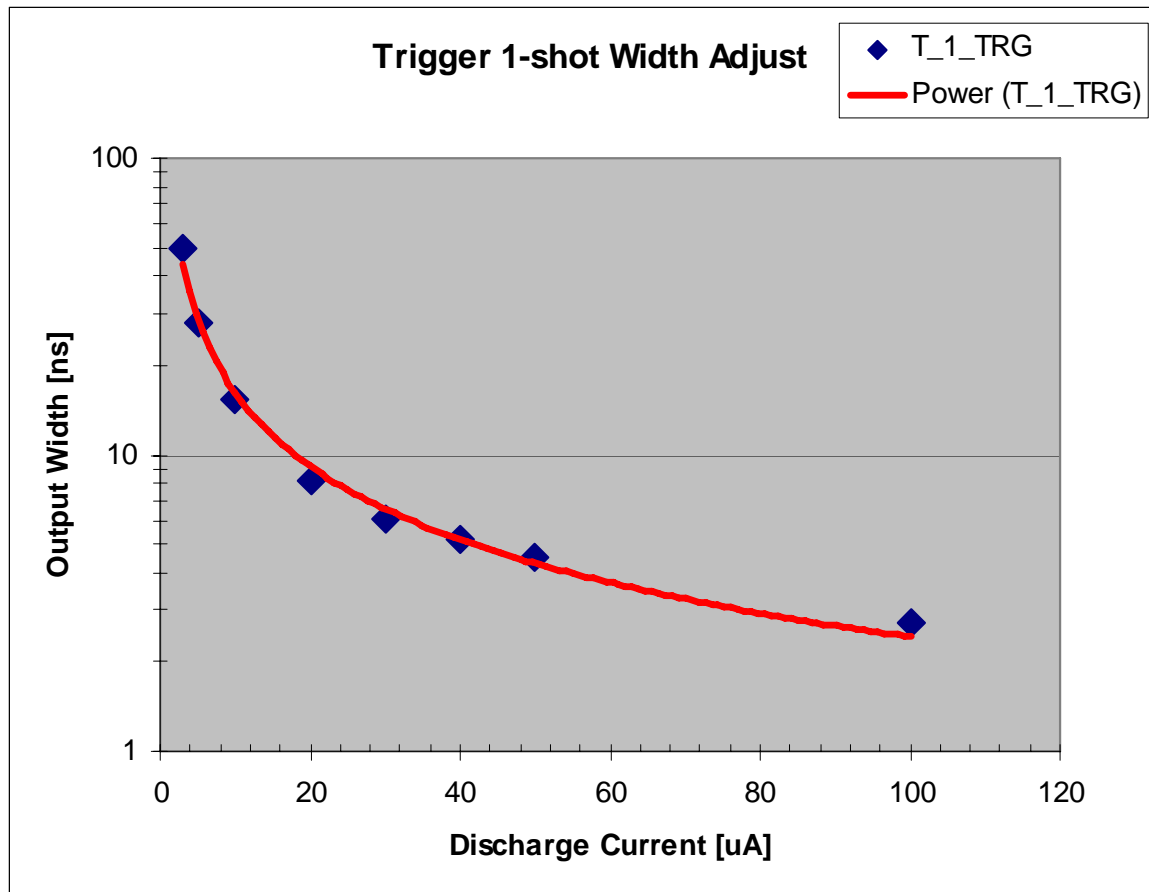
- Need 100 telescopes, each with 10,000 photodetection channels (1M channels)
- Detailed Cost exercise
 - For >10,000 channels, price drops drastically
- Trigger functionality needed
- Very large “dark sky” background, but can still trigger! (use same scheme in Belle2?)

Trigger Logic



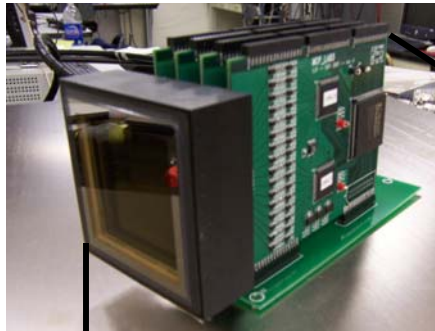
- Analog (Sum of # Ch. ON) & Digital OR output
- 1-Shot or Raw comparator output

Trigger Simulation

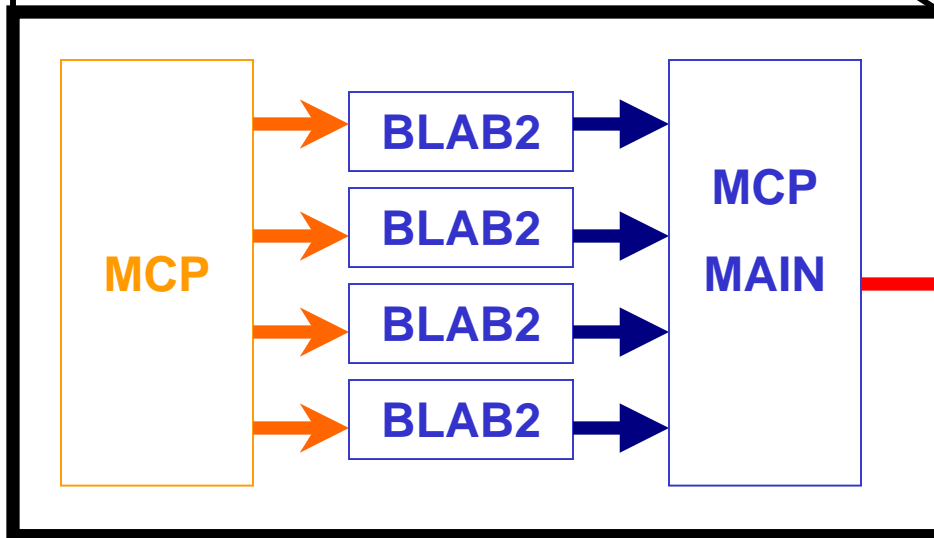
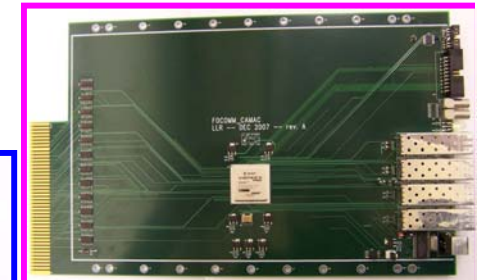
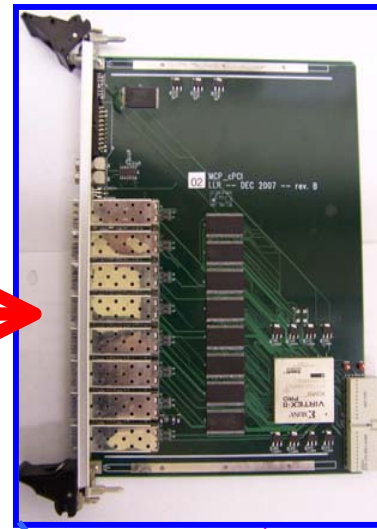


- **Good Adjustment Range**
 - Reasonable current values
 - Preliminary Design (could also buffer out analog), use FPGA as Discrim. [ANITA] Journ. Instr. Vol 1, P07001 (2006).

Test System Block Diagram



**Giga-bit
Fiber**



x7

**cPCI
CARD**

**cPCI
Crate
(Linux)**

x1

**CAMAC
CARD**

**CAMAC
Backplane**

- Up to 7x64 channels per cPCI card
- CAMAC card for SLAC beam test
- Up to 32,256 channels/cPCI crate

**Very cost effective, board hardware
already exists**

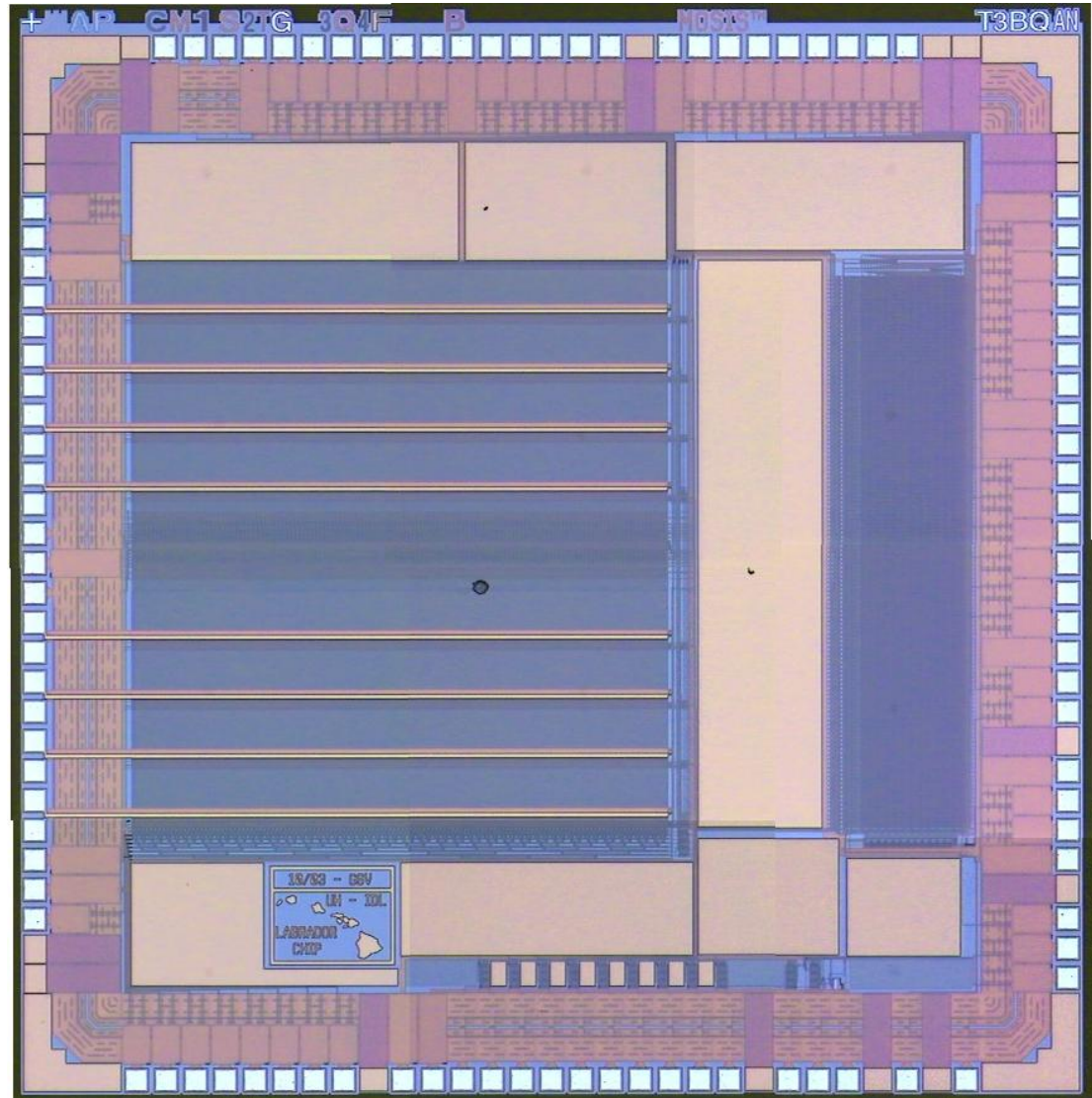
Summary

Building toward a major system (beam) test

- BLAB2 design almost done (final amplifier, trigger decisions)
- Delay has made design better, also beating the bushes for the ~25k\$ needed
- No show-stoppers
- Get serious about a “~1k channel” system test?
- What needed for demonstration in light of upcoming TDR(s)?

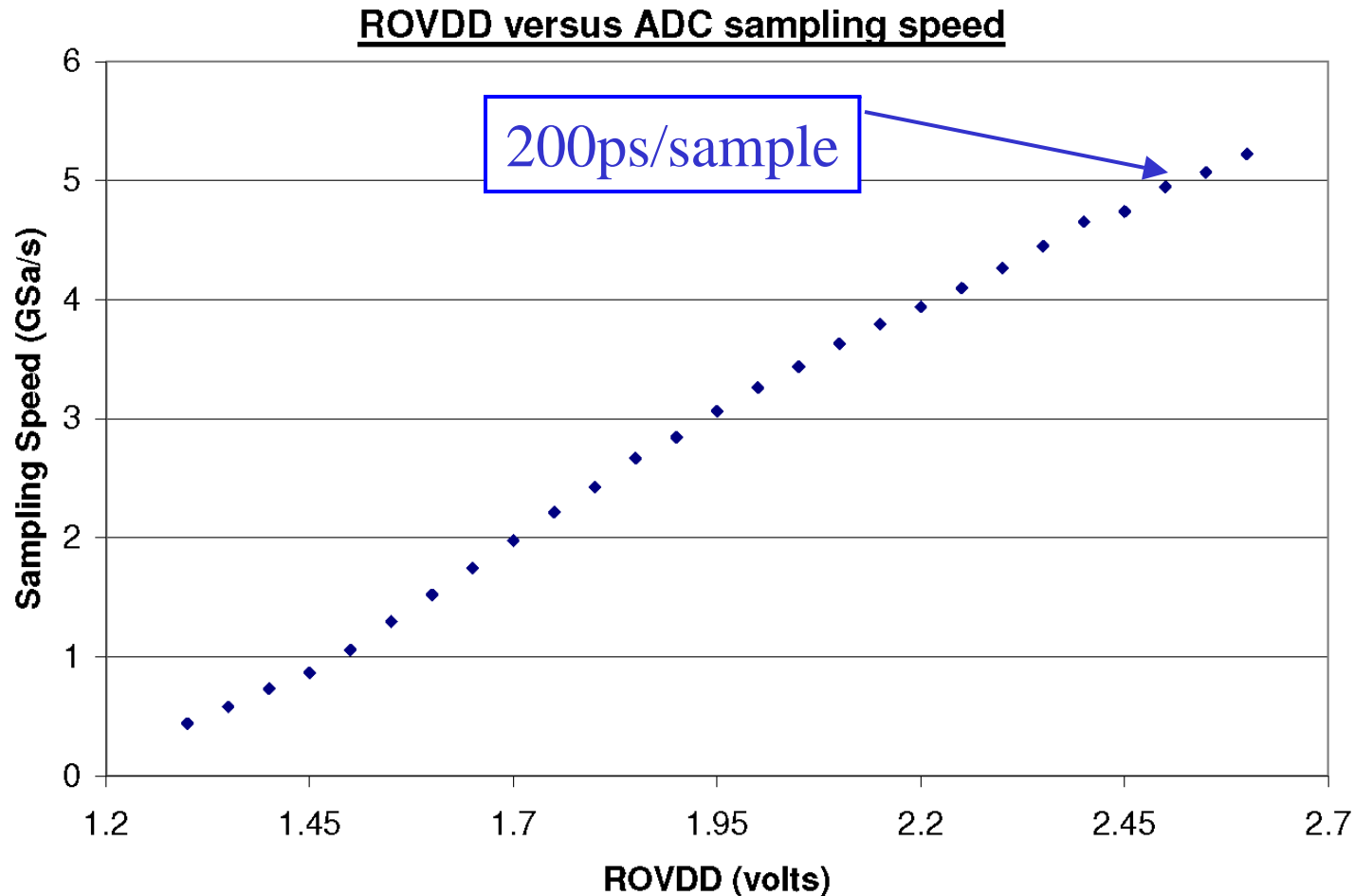


Back-up slides



BLAB1 Sampling Speed

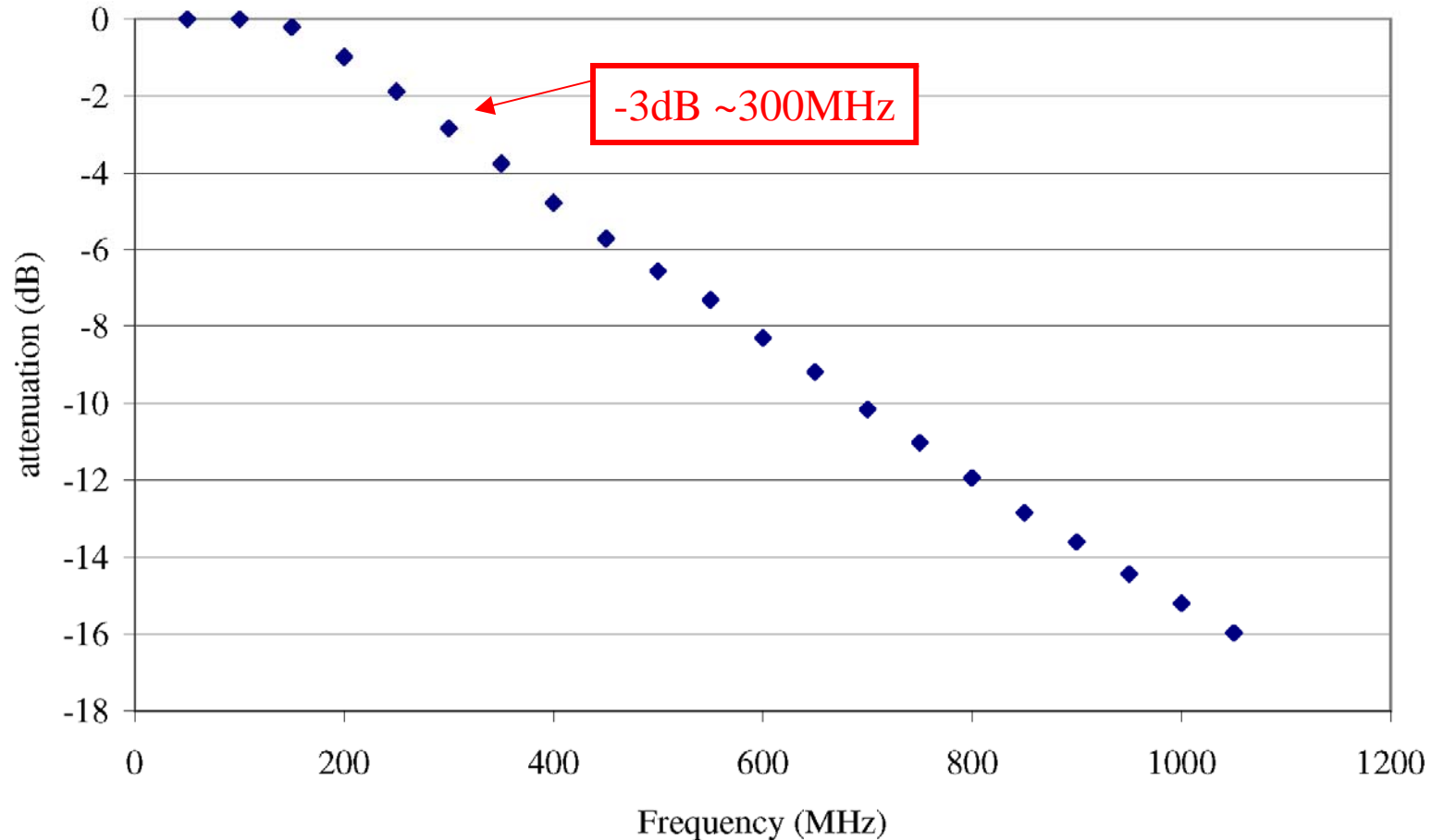
Can store 13us at 5GSa/s (before wrapping around)



Single sample:
 $200/\text{SQRT}(12)$
 $\sim 58\text{ps}$

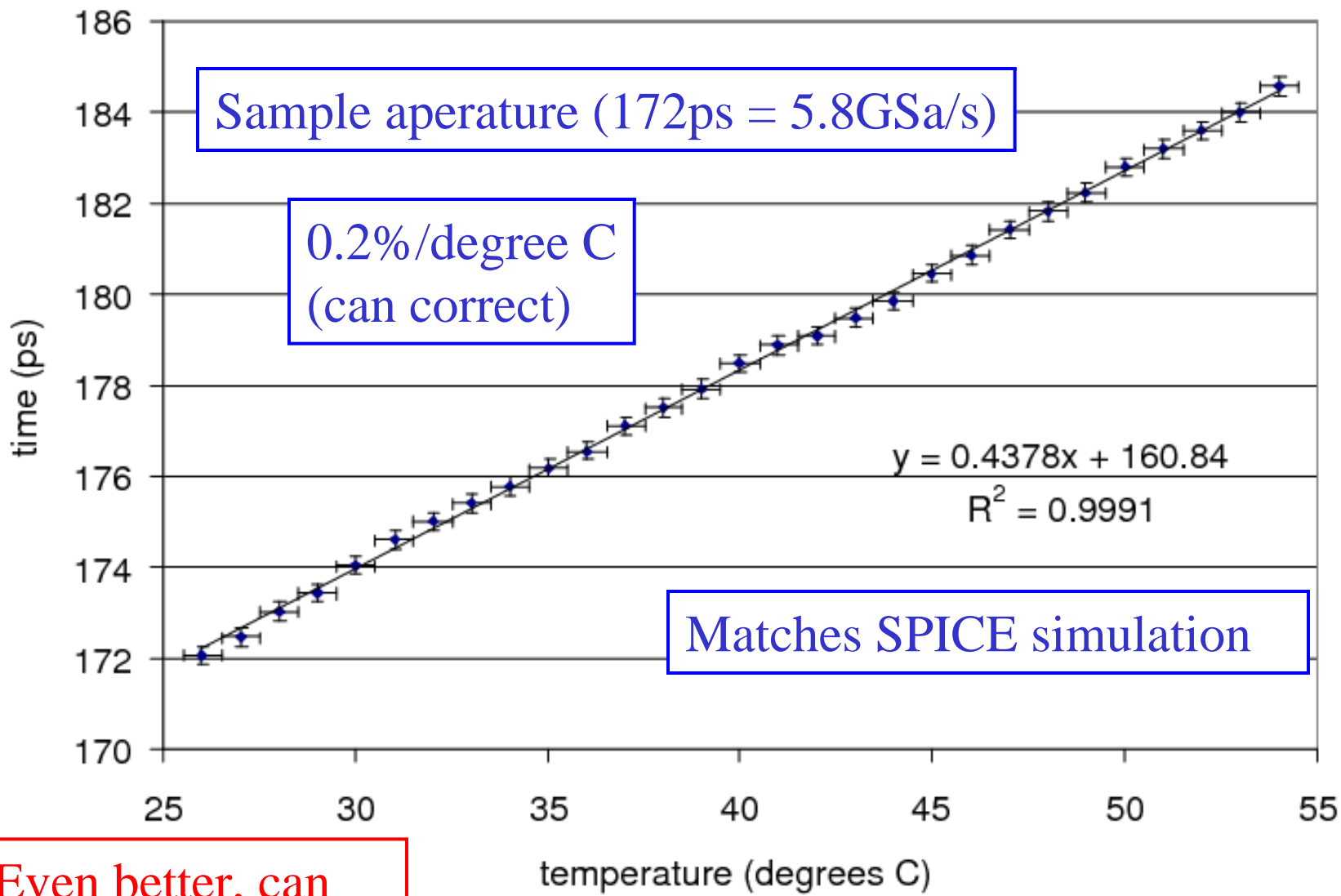
But, have
Complete
Waveform
Information

BLAB1 Analog Bandwidth



- A few fixes (lower power, **higher BW**)
- Multi-channel: BLAB2 (16), TARGET (16 w/ gain), LARC (32) and PrX

Temperature Dependence



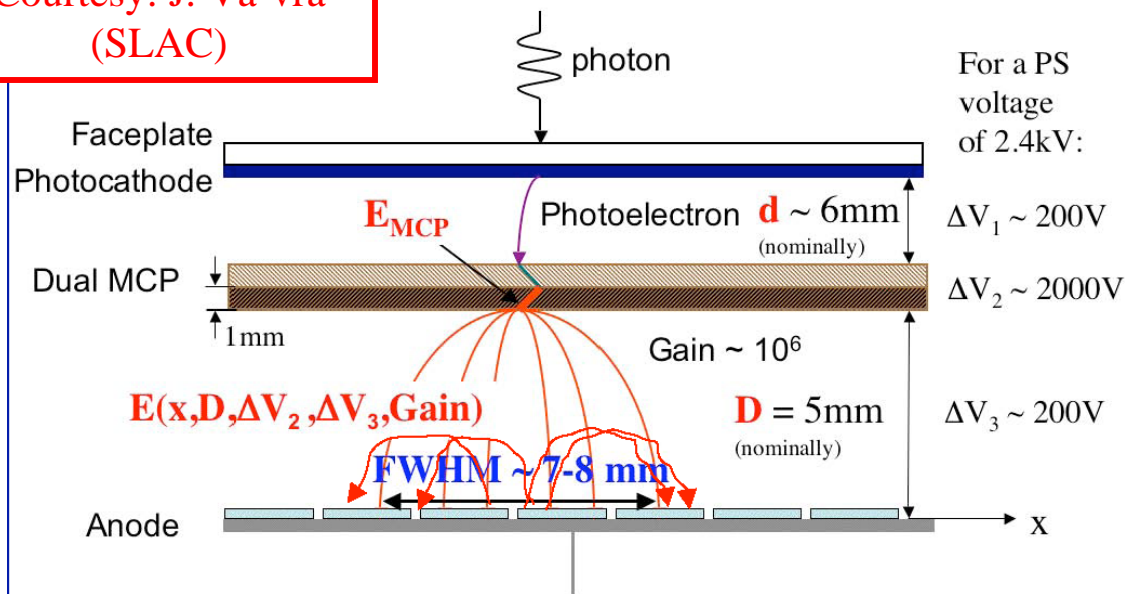
Even better, can
delay lock

Limitations 1: Analog Bandwidth

Difficult to couple in Large BW (C is deadly)

At what point stop getting useful information?

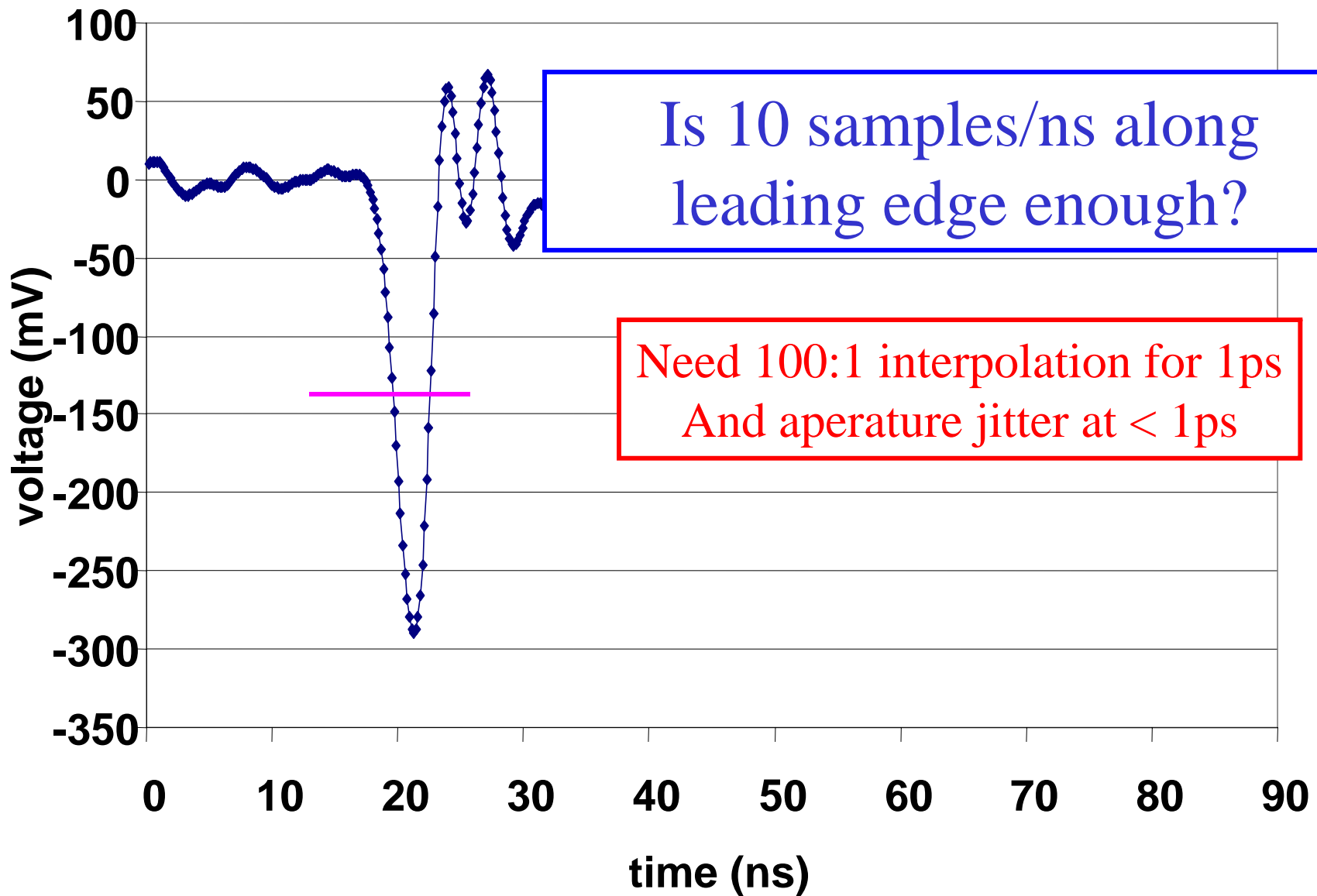
Courtesy: J. Va'vra
(SLAC)



$$f_{3\text{dB}} = 1/2\pi ZC$$

Limitations 2: Interpolation Error

Tied to Bandwidth Issue

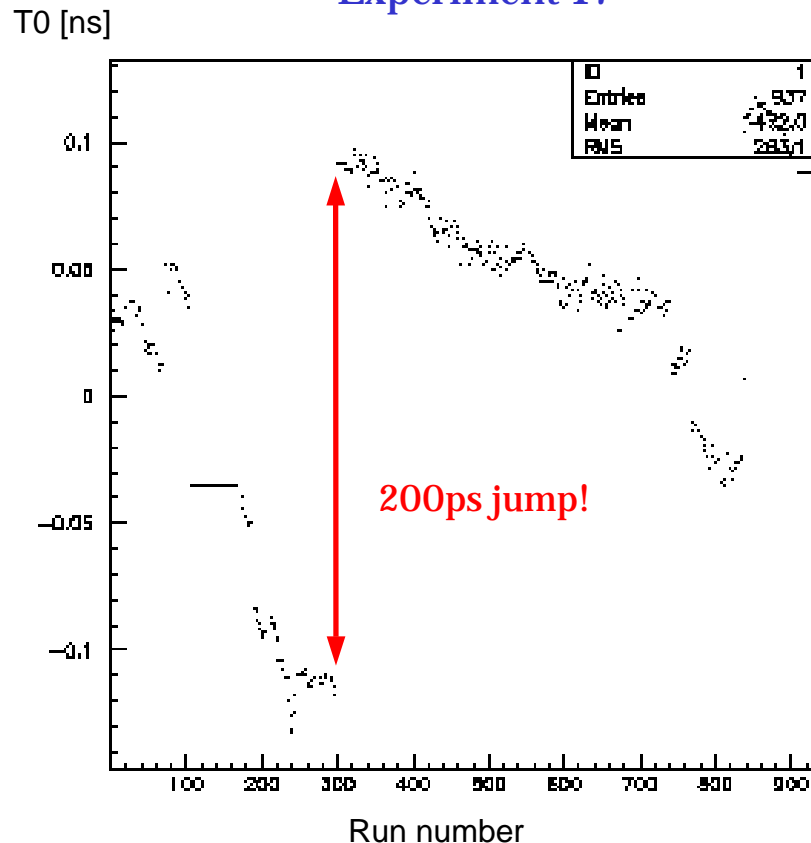


Limitations 3: Systematic Errors

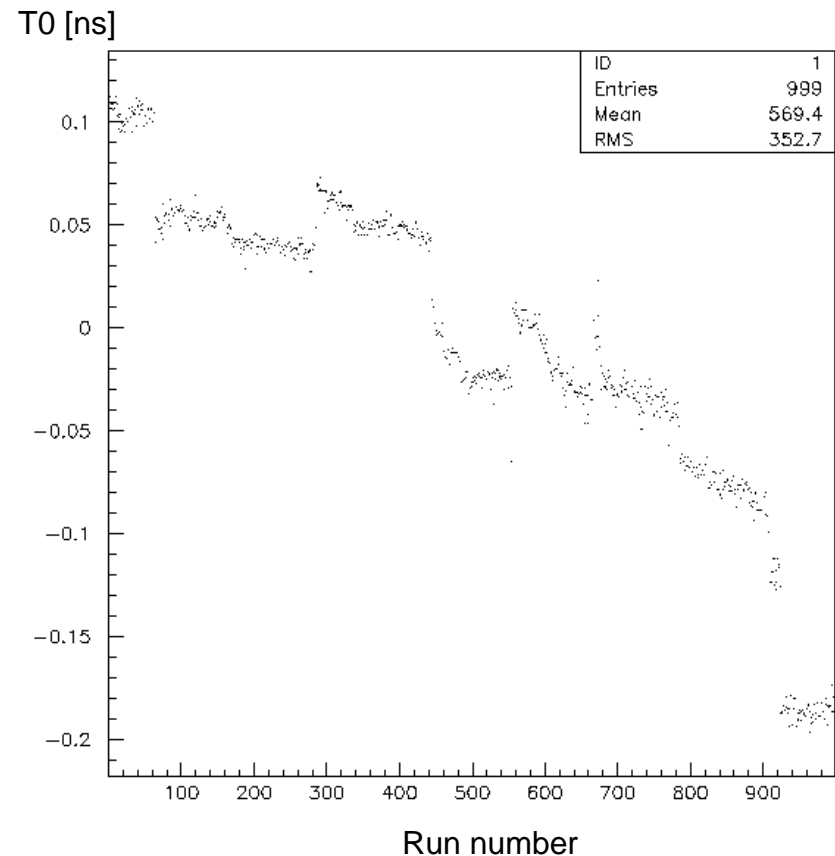
Experience with running Belle TOF System for ~ a decade

Any jitter/shift/jump in reference time is fatal? (differential measurements)

Experiment 17



Experiment 19

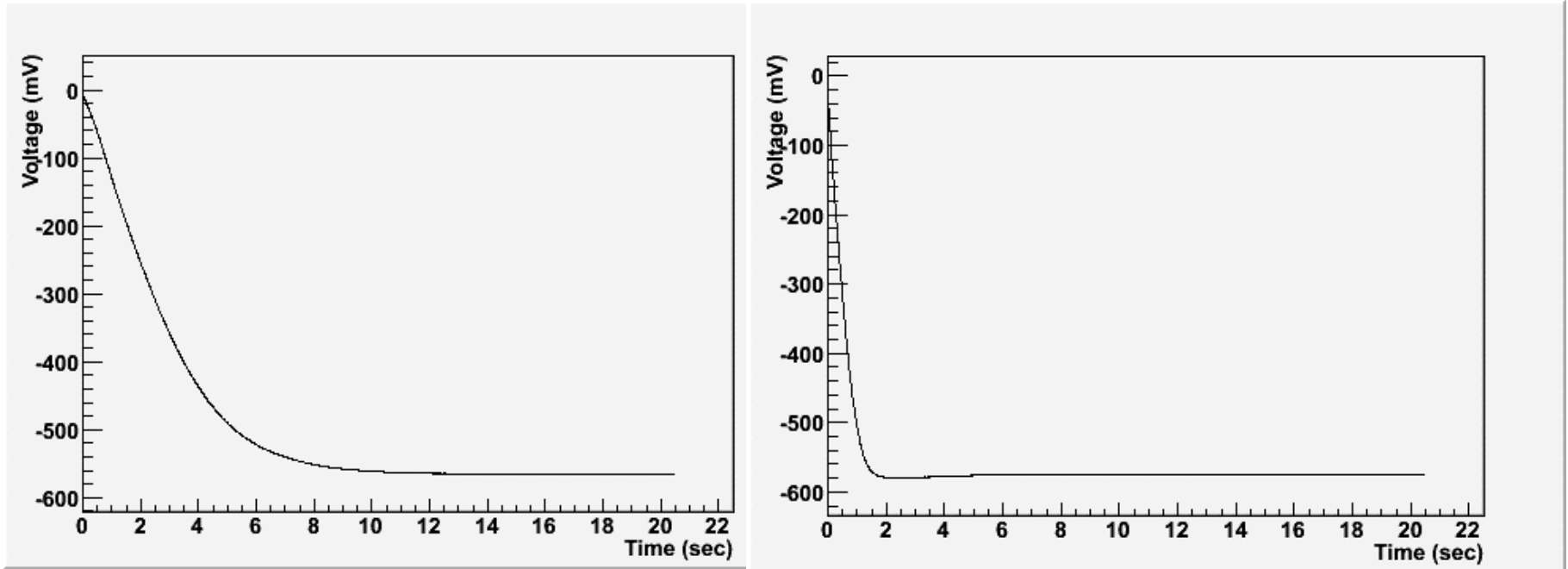


- Run-by-run T_0

Limitations 4: Leakage Current

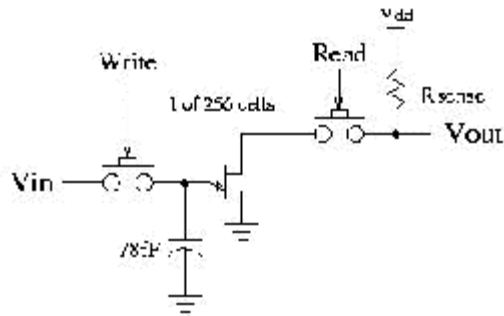
Need small C for Input Coupling

Can Improve? (readout faster)



Limitations 5: kTC Noise

Need small C for Input Coupling



$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

$$C_{store} = 78fF$$

