ep-BPM

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1.0 Introduction

The electron-positron beam position monitor (epBPM) has been designed to measure position of single electron and positron bunches for the SLC, LINAC, PEP-II injection lines and final focus. The epBPM module has been made in CAMAC standard, single width slot, with PDU timing connector. The required dynamic range is from $5 \cdot 10^8$ to 10^{11} particles per bunch (46dB). The epBPM input signal range is from ± 2.5 mV to ± 500 mV. The pulse-to-pulse resolution is less than 2 μm for $5 \cdot 10^{10}$ particles per bunch for the 12 cm long striplines, covering 30° at 9 mm radius.

The epBPM module has four input channels X+, X-, Y+, Y- (Fig. 1), named to correspond with coordinates of four striplines - two in horizontal and two in vertical planes. The epBPM inputs are split for eight signal processing channels to catch two bunches, first - the positron, then the electron bunch in one cycle of measurements. The epBPM has internal and external trigger modes of operations. The internal mode has two options - with or without external timing, catching only the first bunch in the untimed mode. The epBPM has an on board calibration circuit for measuring gain of the signal processing channels and for a timing scan of the programmable digital delays to synchronize the trigger and the epBPM input signal's peak. There is a mode for pedestal measurements. The epBPM has 3.6 μs conversion time.

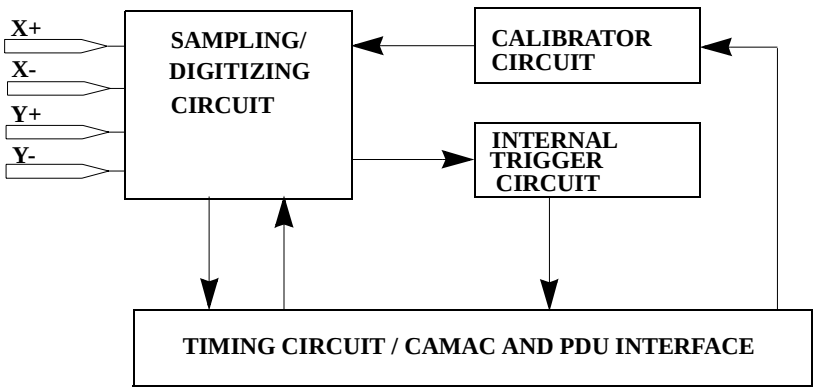

FIGURE 1. The block diagram of the epBPM module.

2.0 Signal Processing and Digitizing Circuit

The input signal from the stripline electrode “X+” propagates through the Splitter/ Combiner S/C1 (5MHz - 500MHz bandwidth) and Bessel Lowpass Filter (40 MHz bandwidth) (Fig. 2). This signal goes to the Signal Amplifier (OA1, gain 5) and to the Trigger Amplifier (OA2, gain 2). The S/C2 accepts the calibration signal, S/C3 accepts signals from the stripline electrode “X-”. The Signal Amplifier feeds a 27 ns delay line (74 MHz bandwidth). Delayed signal goes to two fast sample-and-hold amplifiers S/H_AX+ and S/H_BX+ (14-bits accuracy, 30 ns acquisition time).

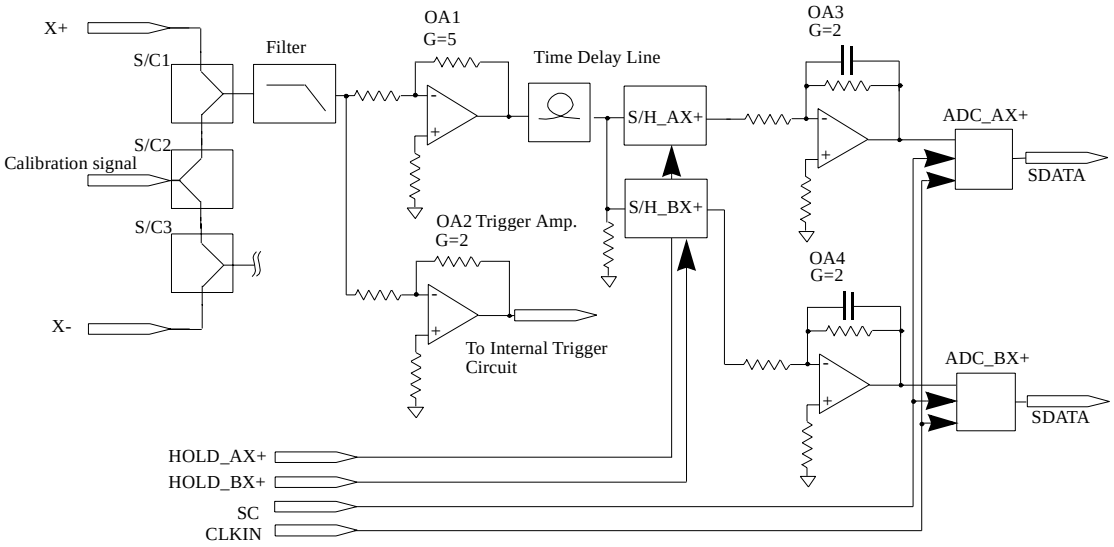

FIGURE 2. The Signal Processing and Digitizing Circuit; X+ Signal Processing Channel.

The delay line compensates propagation delay of the S/H triggering pulse through the Trigger Circuit in order to hold the S/H input signal peak. The “A” and “B” sample-and-hold output signals go to amplifier OA3 and OA4 (gain 2), respectively. Those amplifiers narrow the signal bandwidth to 4 MHz to meet the ADC bandwidth (1.5 MHz). The ADC has 14 bit resolution (13 bits plus sign), 400 ns acquisition time, 3.2 μs conversion time and serial data output (SDATA). The ADC digitizes the signal synchronously with the Start Conversion pulse (SC). The ADC output data is 16-bits data stream starting with two zeros followed by 14 data bits (MSB first). To read data from the ADC, 16 pulses (5 MHz frequency, TTL format) are supplied to the ADC clock input (CLKIN).

3.0 Internal Trigger Circuit

The internal trigger pulse is the reference for the S/H “Hold” pulse in “gating” and “no timing” modes of operation. The Internal Trigger Circuit derives a trigger pulse from the zero crossing of the epBPM input signals.

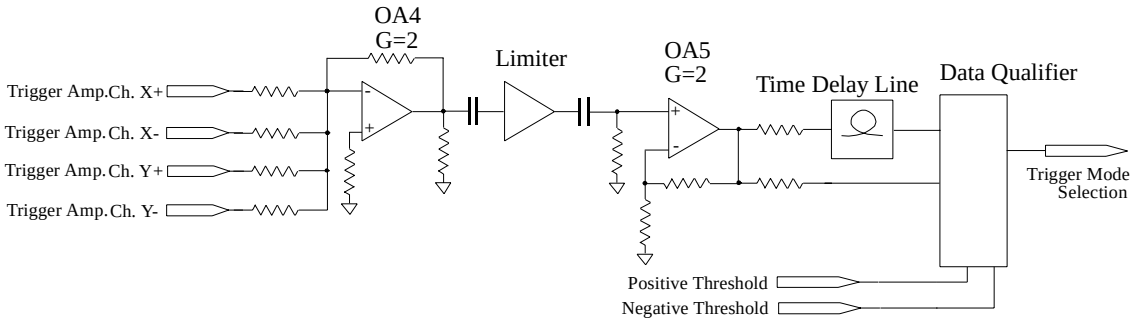

FIGURE 3. Internal trigger Circuit

The summing amplifier OA4 (Fig. 3) output signal (±2 V max) is the sum of the signals from four trigger amplifiers (Fig. 2). The Limiter is a noninverting amplifier with gain 4 and output signal range limited by ±1 V. This increases the dynamic range of the internal trigger circuit. Limiter output goes to a noninverting amplifier OA5 (gain 2), which is used as an input buffer for the Data Qualifier.

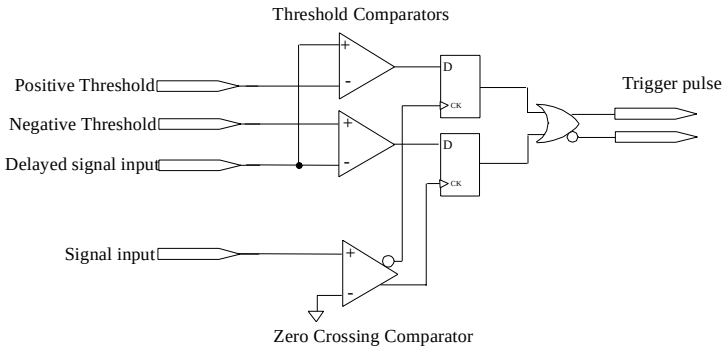

FIGURE 4. Data Qualifier Block Diagram.

The Data Qualifier (Fig 4.) consists of two threshold comparators, one zero crossing comparator and a digital circuit to generate the output pulse. The threshold comparators input signal is delayed for 5ns to set flip-flops D input to logic state “high” before a zero crossing event will be detected. The threshold levels determine the level of the lowest signal which could be “seen” by the Data Qualifier. Potentiometers are used to adjust thresholds levels. The Data Qualifier generates a single trigger pulse (ECL) synchronously with the zero crossing event, 35 ns duration time. After generation of one pulse the Data Qualifier is ready for the next zero crossing event.

4.0 Calibrator Circuit

The Calibration Circuit generates a bipolar pulse with a positive or negative first peak. The pulse shape is similar to a positron or electron pulse shape from a stripline electrode. The Calibrator is used for the signal processing channels gain measurements and for tune up of the programmable digitals delays in a trigger pulse chain, to minimize a mismatch between the S/H “Hold” pulse and the input signal peak.

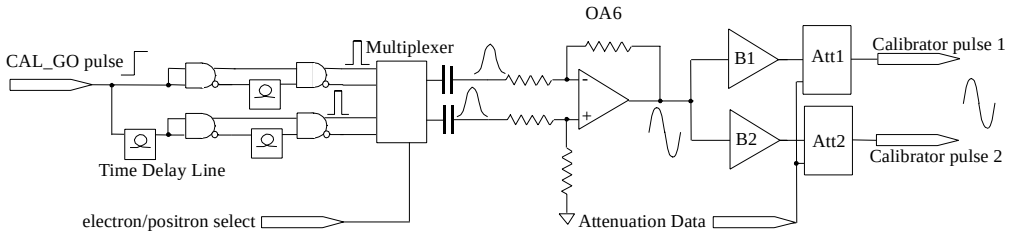

FIGURE 5. The Calibrator Circuit.

Calibration start pulse (CAL_GO) goes to two digital channels (Fig. 5), one delayed from the other for 4ns, deriving two short pulses (4 ns duration time). Multiplexer selects which pulse will be first at one of the differential amplifier OA6 inputs. In the case if the first pulse goes to the positive input and delayed pulse goes to the negative input - OA6 output pulse will be positron-like, if the first pulse goes to the negative input and delayed to the positive, it will be an electron-like pulse. OA6 output signal feeds two buffers. The buffers output signals goes to programmable attenuators, 30dB dynamic range, both attenuators have the same input data. The Calibrator attenuated signal supplies two S/C (channels X+, X- and Y+, Y-). The Calibrator output signal maximum amplitude is ± 3 Vpp (modules 1 to 10) and ± 1.5 Vpp all other modules, 4ns between peaks.

5.0 Trigger Modes Selection and Timing Adjustment Circuit

The epBPM module has three options for triggering the S/H amplifier synchronous with the epBPM input signal peak. The sources of triggering pulses are - external PDU gates, internal trigger pulse or combination of the PDU gate and the internal trigger pulse. Those triggering modes are called - External Trigger, No Timing and Gated respectively.

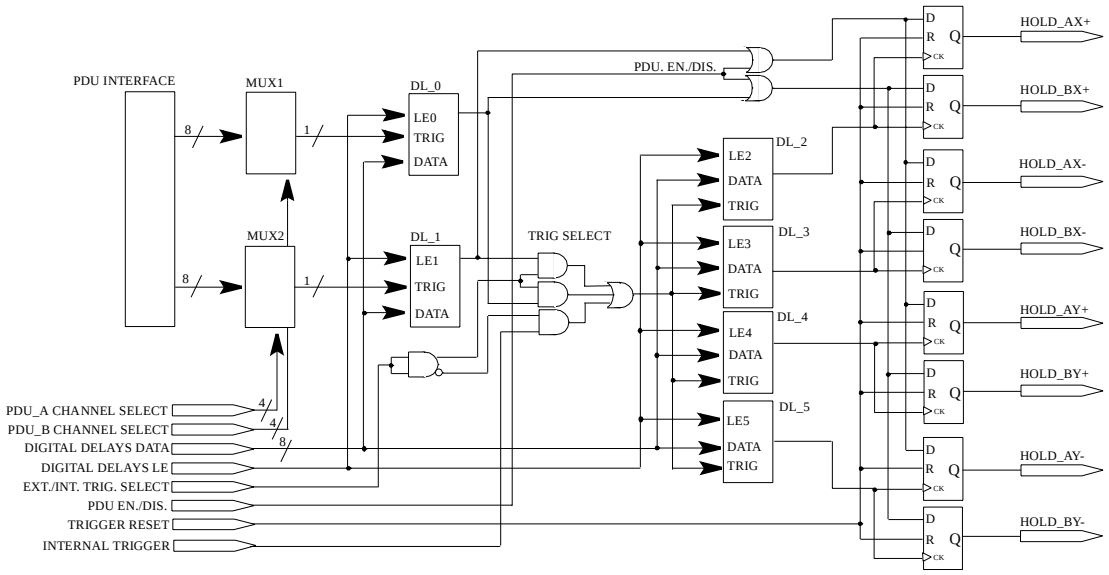

FIGURE 6. Trigger Modes Selection and Internal Delays Adjustment Diagram.

PDU interface is a 16-channels bus. The first signal's (A) PDU gate channels are 0 to 7 and the second signal's (B) PDU gate channels are 8 to 14 (Fig. 4), channel 15 is reserved for pedestal measurement. Multiplexers MUX1 and MUX2 select specific A and B channels respectively. MUX1 and MUX2 outputs go to trigger inputs of the programmable delays DL_0 and DL_1. The purpose of those delays is to compensate external gate cables mismatch. DL_0 and DL_1 output signals and the internal trigger pulse go to trigger mode select gates (TRIG SELECT). Depending on selected trigger mode (EXT/INT TRIG SELECT state) the TRIG SELECT output signal ("OR" gate output) is DL_0 or DL_1 or internal trigger pulse. The selected signal comes to the trigger (TRIG) input of the programmable delays DL_2 to DL_5. Delays DL_2 - DL_5 output signals go to D flip-flops clock (CK) inputs. Those flip-flops drive the S/H clock inputs. Also, DL_0 and DL_1 output signals go through the PDU enable/disable "OR" gates if enabled. DL_0 and DL_1 output signal goes to "A" and "B" channels D flip-flops "D" input respectively. If the PDU is disabled the "OR" gates outputs are in "high" state. The trigger modes selection truth table is shown below.

TRIGGER MODE	EXT/INT TRIG SELECT	PDU EN/DIS
EXTERNAL TRIGGER	1	0
GATED	0	0
NO TIMING	0	1

TABLE 1. Trigger Mode Selection Truth Table

The programmable delays DL_2 to DL_5 are used for the epBPM internal timing adjustment - to match the S/H "Hold" pulse and the S/H input signal peak. An individual delay is used for each signal processing channel. Calibrated delay data is stored in

programmable read only memory (EPLD). Every module has an individually burned EPLD. Delay data loads automatically at power on or at module reset.

The delays DL_0 to DL_5 output signal duration is 20 ns, programmable delay value could vary from 0 to 9.8 ns with 38 ps steps, digital data 0 to 255 respectively.

6.0 Pedestal Trigger Circuit

Timing channel 15 is reserved for pedestal measurements. Pedestal trigger follows the same chain as an external gate. Synchronous with pedestal trigger the S/H stores the input signal value with no beam or calibrator pulse present. The ADC returns this value, which is the “zero” offset of the signal processing and digitizing channel.

7.0 Time Diagram

Two bunches come to each epBPM input (Fig. 7). The trigger pulse front edge, adjusted to be in synchronous with the S/H input signal peak, switchs the S/H to Hold mode. The Timing circuit waits for 400 ns (Ta) after A and B - channel S/Hs switch to Hold mode, then sends a start conversion pulse (SC) and 16 pulses to clock out ADC data (CLKIN) to all ADCs. Clock pulse frequency is 5 MHz. At the third clock pulse the MSB is latched in a shift register, at the 16th pulse the LSB is latched. At this time the Timing circuit tick reaches 3.6μs and sets the Reset input of the S/H driving D flip-flops to “high” state, thus Q sets to “low” state which switches the S/Hs to “sample” mode. When CAMAC command - read last ADC comes, the Reset input sets to “low” state and Q sets to Qn+1=Qn, then the module is ready for next cycle of measurements.

The digitized data stores in 16 bits shift registers, located in a Field Programmable Gate Array (FPGA) chip.

In No Timing mode the module digitizes only the first triggered signal, therefore the “Hold” signals to the “A” and “B” channels S/Hs come at the same time, so “A” and “B” channels data are the same. In the No Timing mode there is an option to read ADCs 0 to 3, or 4 to 7. In this case the module will be reset by the ADC3 or ADC7 read commands.

The purpose of starting “A” and “B” channels ADC conversion at the same time - is to prevent corrupting of “B” channels data due to increased noise, generated by SC and CLKIN pulses. The “A” channels stored signal value maximal droop is approximately between 1 mV and 3 mV at 800 ns and between 0.5 mV and 1.5 mV - for “B” channels at 400 ns. This is less then ADCs minimum input signal - ± 25 mV.

The S/H droop rate is proportional to the inverse of the total hold capacitor value, which is 62 pF. Specified droop rate for 15 pF internal hold capacitor for temperature up to +85 C degree is from ± 5 mV/μs to ± 15 mV/μs.

Time between bunches (Tbb) varies from 58ns to 400 ns, the input signal propagation time to S/H input (Td) is approximately 39 ns, the ADC acquisition time (Ta) is approximately 400 ns, conversion clock pulses are delayed from SC pulse for 100 ns (Tclkd), total conversion time (Tconv) is 3.6 μs, D flip-flops reset time (Treset) depends on particular system application software.

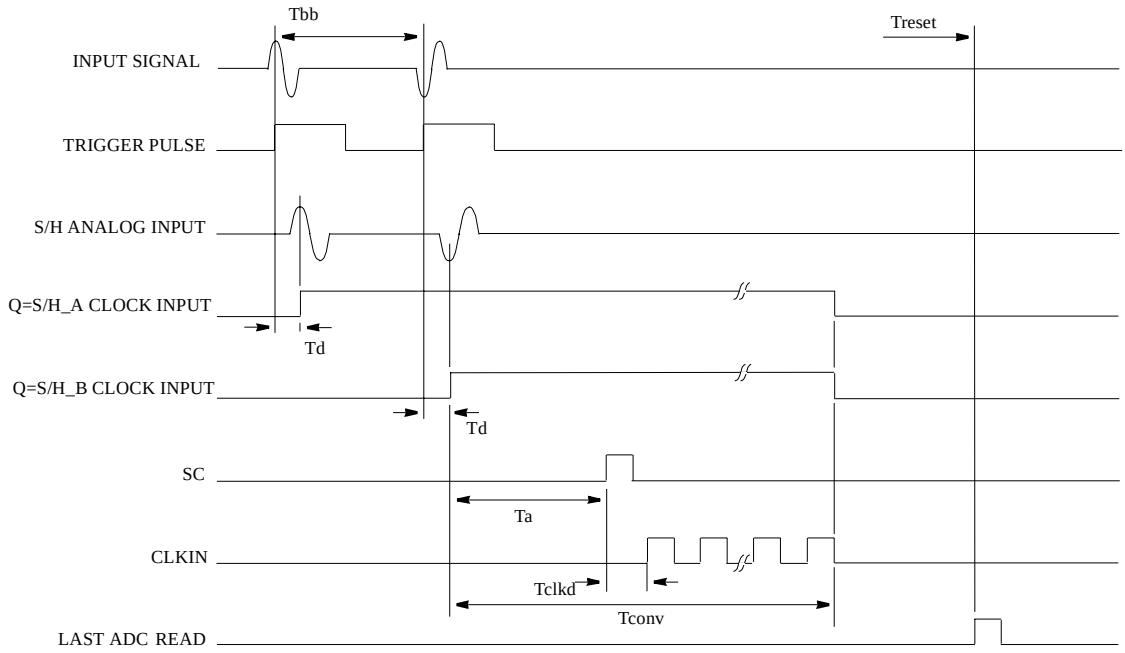

FIGURE 7. The epBPM signal processing time diagram

8.0 CAMAC Interface and Timing Circuit.

CAMAC instructions decoding, timing distribution and ADCs data storage are performed in a Field - Programmable Gate Array (FPGA). The following blocks are programmed in the FPGA: CAMAC instructions decoding; power startup (to load calibrated delay data); Calibrator control - to send CAL_GO pulse, to set attenuators values and to select pulse polarity; ADC control - to read data from the ADC, to reset the S/H driving “D” flip-flops; Pedestal Trigger control - to start pedestal calibration; Trigger Mode control - to select trigger mode; Delays control - to load data to delays DL_0 to DL_5.

Special preconditions are programmed in FPGA for No Timing mode - the module does not recognize internal trigger pulse during CAMAC N - cycle.

The CAL_GO pulse is delayed from CAMAC S2 pulse by 2.2 μs. During the signal processing channels gain calibration the module automatically sets to No Timing mode at 16 ns before GAL_GO pulse. The No Timing window duration is 570 ns.

9.0 Module Requirements and Specifications

The requirements for the epBPM [1] are shown in table 2, also the module must acquire two pulses during the same cycle. The circuit must work over the required beam current and position dynamic range and preprocess the digitized values.

Item	Value	Description
Resolution @ $5 \cdot 10^{10}$ ppp	5 μm rms	minimum movement measurement
Position stability (Linac)	50 μm	apparent movement at different beam currents
Position stability (PEPII)	1mm	apparent movement at different beam currents
Position dynamic range	0 - 1/3 aperture	maximum beam offset ($N < 5 \cdot 10^{10}$)
Dynamic range (Linac)	$2 \cdot 10^{9}$ - $5 \cdot 10^{10}$ ppp	particle per pulse dynamic range
Dynamic range (PEPII)	$5 \cdot 10^{8}$ - 10^{11} ppp	particles per pulse dynamic range
Maximum pulses ratio	10 dB	current ratio between e- and e+
Repetition rate	120 Hz	maximum machine cycle
Sampling cycle	60 ns	electron/positron separation
Analysis time	1 ms	maximum time for data processing

TABLE 2. Beam position measurement requirements.

The specifications estimates for the epBPM module are based on calculations of the circuit noise level [2].

The ADC signal-to-noise plus distortion ratio (SINAD) is 78 dB at 50 kHz input sinusoidal signal, 300 kHz sampling rate. The effective number of bits (N_{eff}) from the SINAD:

$$N_{eff} = \frac{SINAD - 1.76}{6.02} \approx 12.7$$

The quantization error σ is: $\sigma = \frac{q}{\sqrt{12}} \cdot 2^{(N_{id} - N_{eff})} = 0.7 \cdot q$,

where q is the ADC quanta's size (least significant bit), N_{id} - ideal ADC number of bits (14 bits in our case). Least significant bit value is:

$$q = \frac{10}{2^{14}} = 610 \mu V.$$

The ADC noise value is:

$$\sigma \approx 434 \mu V \quad \text{rms.}$$

The OA3 (Fig. 2) input noise in 4 MHz bandwidth is 22 μV rms, the S/H noise is specified as 65 μV rms, OA1 input noise in 100 MHz bandwidth is 25 μV rms, noise generated by resistors is 14 μV rms. Total noise value at the input of the ADC is 54 μV rms or 15.4 dB, referred to 50 Ohms resistance noise value in 100 MHz band. The signal processing channel gain is 10, so the equivalent ADC input noise is 540 μV rms.

The dynamic range as the ratio between the ADC maximum input signal and circuit noise at the ADC input is $6.5 \cdot 10^3$ or 76 dB.

Resolution (Δx) is:

$$\Delta x = \frac{a}{2\sqrt{2}} \cdot \frac{V_N}{V_0},$$

where V_N - is the rms noise value at the OA1 input, V_0 - is the bunch peak voltage for the beam in the center, $a = 9mm$ - half of the beam pipe aperture.

The following calculations are based on the signal measurements from the Linac stripline electrode, connected in series with S/C and Filter. At $1.5 \cdot 10^{10}$ ppb, beam in the center, the peak signal amplitude is approximately 68 mV. Calculated resolution for different number of particles per bunch is shown in a table 3.

N, particles per bunch	x, μm	comments
$5 \cdot 10^8$	75	PEPII min. specified N
$2 \cdot 10^9$	18	Linac min. specified N
$1.5 \cdot 10^{10}$	2.5	measured
$5 \cdot 10^{10}$	0.8	Linac max. specified N
10^{11}	0.4	PEPII max. specified N

TABLE 3. Resolution for different numbers of particles for bunch.

Measured resolution at $2 \cdot 10^{10}$ ppb, beam in the center, is approximately 4 μm worse than 1.9 μm from calculation, but better than 12.5 μm, calculated from requirements. The resolution limiting factor is the difference of the propagation delay between peak and zero crossing for electron and positron pulses in the Internal Trigger circuit. The result is different programmable delays values for the pulses with different polarity of the first peak. To achieve the best resolution for both pulses, an average delay value is used.

The measured dynamic range in the External Trigger mode with a Test Pulse Generator (TPG) is 68 dB (TPG dynamic range), in the Internal Trigger mode - 48 dB. In the Internal Trigger and Gated mode dynamic range is limited by noise, coming from the digital part of the epBPM board and from external sources.

10.0 Programming

10.1 Measurements

10.1.1 10.1.1 Preset programmable delays

- Function code: F17
- Module address: A0 for DL_0 and DL_1, A2, A3, A4, A5 for delays DL_2, DL_3, DL_4, DL_5 respectively.
- Data: 8 bits, DL-1 data use bits 8 to 15, DL_0, DL_2, DL_3, DL_4, DL_5 data use bits 0 to 7.
- To load delays DL_0 and DL_1 use data code: dataDL_0 + 256 x dataDL_1

10.1.2 Read programmable delays

- Function code: F1
- Module address: A0, A1, A2, A3, A4, A5 for delays DL_0, DL_1, DL_2, DL_3, DL_4, DL_5 respectively.
- Data: 0, returned data - 8 bits (0 (LSB) to 7)

10.1.3 Select PDU channel

- Function code: F17
- Module address: A9
- Data: 8 bits, PDU_A channels are 0 to 7, PDU_B channels are 8 to 14, channel 15 is reserved for pedestal trigger pulse
- To select PDU channel use: PDU_A channel # + 256 x PDU_B channel #

10.1.4 Select Trigger mode

- Function code: F17
- Module address: A6
- Data: 0 - external trigger mode, 1 - gated mode, 2 - no timing mode

10.1.5 Read Trigger mode

- Function code: F1
- Module address: A6
- Data: 0, retuned data - 2 bits (0 (LSB) and 1)

10.1.6 Read ADC data

- Function code: F0

- Module address: A0, A1, A2, A3 - ADC AX+, AX-, AY+, AY- (first bunch); A4, A5,A6,A7 - BX+, BX-, BY+,BY- (second bunch)
- Data: 0, returned data - 16 bits, unsigned, bits 2 to 15 - ADC data

10.2 Calibration

10.2.1 Electron/positron select and attenuator preset

- Function code: F17
- Module address: A8
- Data: 5 bits, bits 0 to 3 are attenuator data, 0000 - attenuation 0, 1111 attenuation 30dB (2dB step); bit 4 - electron/positron selection, bit4=0 (default) - electron, bit 4 = 1 - positron
- To load attenuator data and to e/p select use data code: att.data + 15 x e/p select data

10.2.2 Pedestal trigger start

- Function code: F25
- Module address: A0
- Data: 0

10.3 Others

10.3.1 Serial number

- Function code: F0
- Module address: A10
- Data: 0, returned data - 8 bits

10.3.2 Reset

- Function code: F9
- Module address: A0
- Data: 0

10.3.3 X and Q return

- X returns true if function F and address A decoded correctly in the module
- Q returns true for read ADC commands if ADCs data conversion occurred and data stored in a shift registers; Q=X for all other CAMAC commands

11.0 REFERENCES

[1] “epBPM Manual”, Roberto Aiello, work note, SLAC, 1995

[2] “epBPM Noise, Dynamic Range, Resolution Estimates”, Evgeny Medvedko, work note, SLAC, 1996