XVME 203/293

Counter Module with Quadrature

P/N 74203-002B

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Chapter 1

MODULE DESCRIPTION

1.1 INTRODUCTION

The XVME-203 is a single-high, VMEbus-compatible module and the XVME-293 is a double-high, VMEbus-compatible module that contains ten independent counting channels. These counters can be used alone or in groups to perform a variety of high-level measurement and control functions, including:

XVME-203	XVME-293
- Ten counting channels - Event counting - Frequency measurement - Period measurement - Position measurement (quadrature decoding) - Duty cycle generation - Pulse train generation - Eight of the channels can generate interrupts - Flexible interrupt controller - Complete VMEbus interrupter - Software selectable interrupter level - Programmable IACK vector - IACK vector changes with source of interrupt - Eight of the channels have off-board sources - Eight of the channels outputs can drive signals off board - Status and Control registers - On board crystal oscillator	- Ten counting channels - Event Counting - Frequency measurement - Period measurement - Position measurement (quadrature decoding) - Duty cycle generation - Pulse train generation - Eight of the channels can generate interrupts - Flexible interrupt controller - Complete VMEbus interrupter - Software selectable interrupter level - Programmable IACK vector - IACK vector changes with source of interrupt - Eight of the channels have off-board sources - All ten of the channels outputs and the FOUT frequency divider signals can drive signals off board - Status and Control registers - On board crystal oscillator

The two System Timing Controllers (STC) on the module can generate outputs that can cause interrupts to the VMEbus.

Detailed information for the System Timing Controller is available with the Am9513 Handbook included with the module.

1.2 MANUAL STRUCTURE

The first chapter is an overview introducing the user to the XVME-203/293 general specifications and functional capabilities. Successive chapters develop the various aspects of module specifications and operation in the following manner:

Chapter One - A general discussion of the module including complete functional and environmental specifications, VMEbus compliance information and detailed block diagrams

Chapter Two - Module configuration information covering specific system requirements, jumpers, and connector pinouts

Chapter Three - Discussion of module memory map components

The Appendices are designed to provide additional information in terms of the backplane signal/pin descriptions, a block diagram and assembly drawing, module schematics, and quick reference guide.

1.3 RELATED DOCUMENTS

The following documents should prove helpful in the understanding of the operation of the XVME-203/293 Counter Module:

Publisher	Title	Date
Advanced Micro Devices	Handbook, The Am9513A System Timing Controller*	1986
Advanced Micro Devices	Handbook, The Am9519A Universal Interrupt Controller*	1986

* Xycom part nos. 91366-001 and 91581-001 (one copy of each provided with each XVME-203/293 board)

1.4 MODULE OPERATIONAL DESCRIPTION

Figure l-l shows an operational block diagram of the XVME-203 Counter Module and Figure 1-2 shows an operational block diagram of the XVME-293 Counter Module.

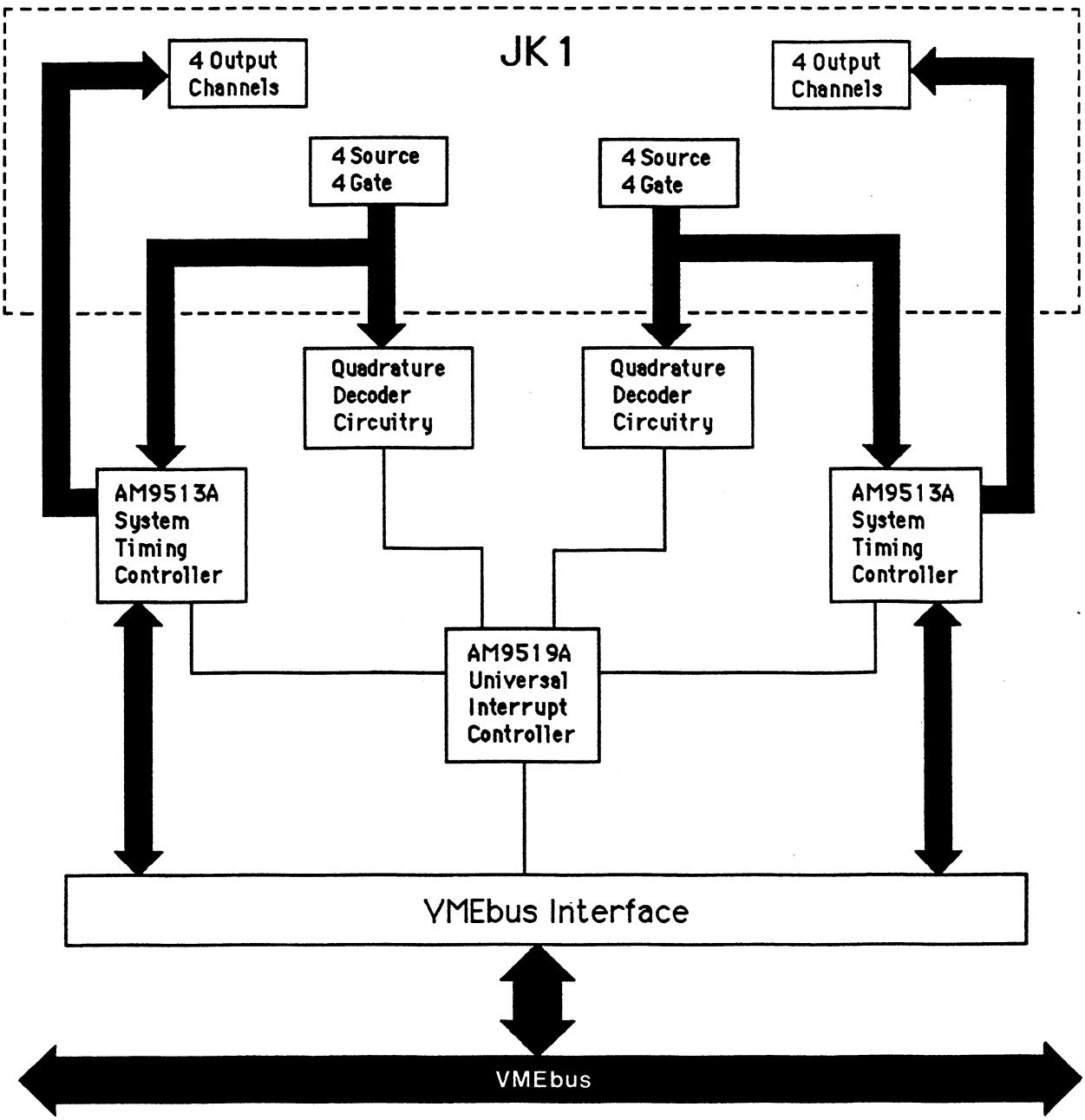


Figure 1-1. XVME-203 Module Block Diagram

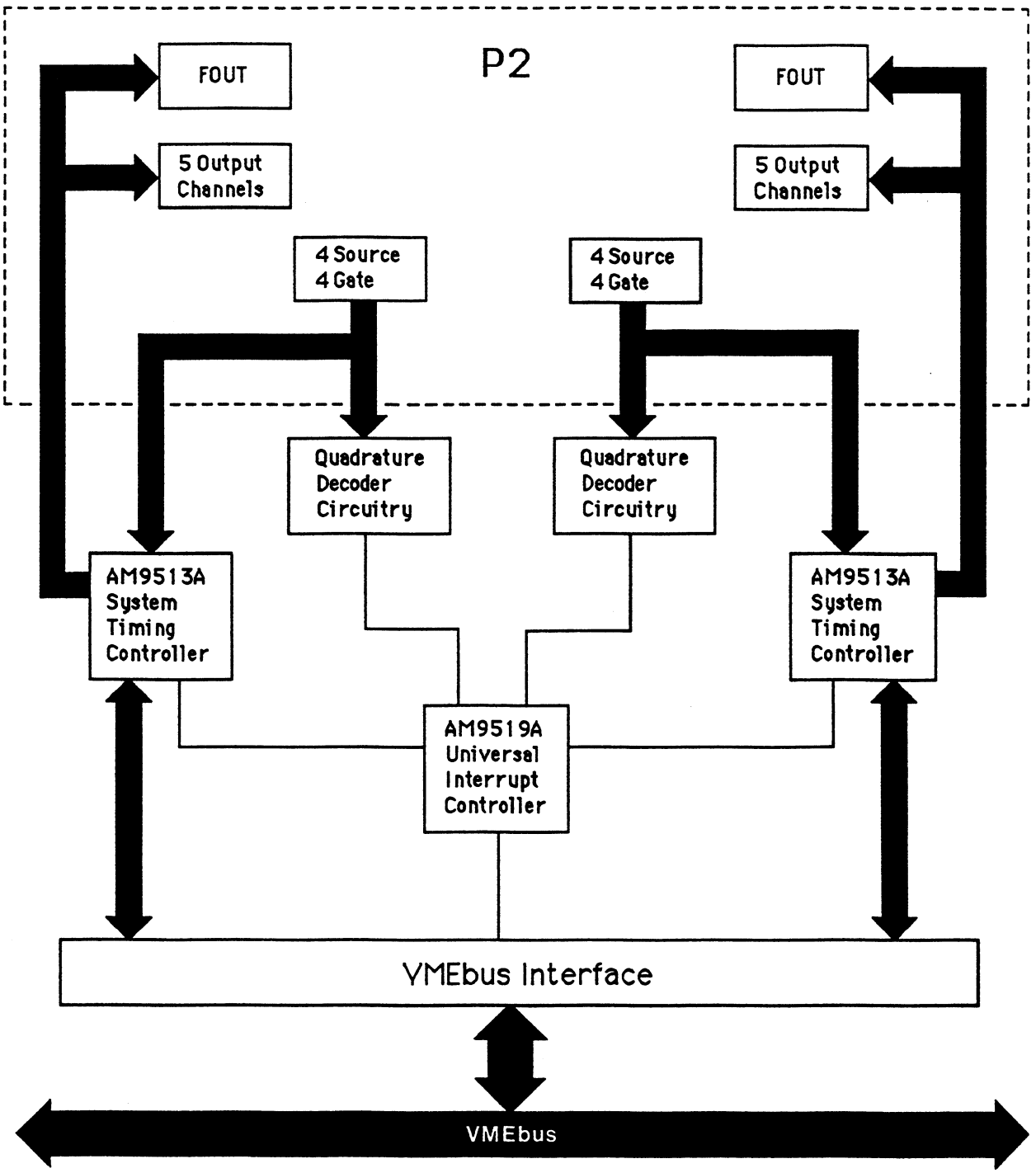


Figure 1-2. XVME-293 Module Block Diagram

1.4.1 Application Circuitry

As Figure l-l and 1-2 shows, the circuitry on the XVME-203/293 consists of the following parts:

- VMEbus interface circuitry
- Two Am95 13A System Timing Controllers
- An Am95 19A Universal Interrupt Controller
- Quadrature Decoder

1.5 SPECIFICATIONS

1.5.1 Mechanical Specifications

The XVME-203 module uses a standard single-high Xycom front panel (a double-high front panel is optional). The I/O signals are connected in the front of the panel (via one 50-pin flat-ribbon connector) to JKl.

The P2 connector for the XVME-293 will accept the I/O signals via the user defined VMEbus pins on rows A and C (discussed in greater detail in Chapter 2). The P2 connector is a standard VMEbus P2 backplane connector with 96-pins (3 rows). The P2 connector is designed to interface with a VMEbus defined P2 backplane.

Board Dimensions	XVME-203: Single-height size (150 x 116.7 mm)
	XVME-293: Double-height size (160 x 233.4 mm)

1.5.2 Electrical Specifications

Unless specified, **all** values are for **both** the XVME-203 and XVME-293.

Number of Channels	XVME-203	XVME-293
Input	1 0	10
Output	8	10
Interrupt	8	8
FOUT	0	2
Timer/Counter Devices	2 (Am9513A System Timing Controllers)	
Interrupt Control Device	1 (Am9519A Universal Interrupt Controller)	
Maximum Counting Rate	5 MHz	

Power Requirements	
XVME-203	+5v +5%
Typical	1.85A
Mean	1.8A
Maximum	2.1A
Standard Deviation	.069A
XVME-293	+5v +5%
Typical	1.90A
Mean	1.82A
Maximum	2.13A
Standard Deviation	.073A
Input Buffers	
Voltage	
Low-level Max.	0.8V
High-level Min.	2.4V
Hysteresis (Min.)	200mV
Input Current	
Low-level	-2OOuA
High-level	+20uA
Output Buffers	
Voltage	
Low-level Max.	0.5v
High-level Min.	2.ov
Output Current	
High-level	-15mA
Low-level	+24mA

1.5.3 Environmental Specifications

Temperature	
Operating	0 to 65°C (32 to 149°F)
Non-operating	-40 to 85°C (-40 to 185°F)
Humidity	
Operating	5 to 95% RH, non-condensing (Extremely low humidity conditions may require special protection against static discharge.)
Shock	
'Operating	30g peak acceleration 11 mSec duration
Non-operating	50g peak acceleration 11 mSec duration
Vibration	
Operating	5 to 2000Hz .015 in. peak-to-peak 2.5g max
Non-operating	5 to 2000Hz .030 in. peak-to-peak 5.0g max
Altitude	
Operating	Sea level to 10,000 f t (3048m)
Non-operating	Sea level to 50,000 ft (15240m)

1.5.4 VMEbus Compliance

- Complies with VMEbus specification Revision C.l
- A16:DO8(0) DTB Slave
- Interrupter - I(l-7) [static]
- Interrupter Vector - Programmable
- Form Factor - SINGLE (XVME-203)
- Form Factor - DOUBLE (XVME-293)

Chapter 2

INSTALLATION

2.1 GENERAL

This chapter describes the various components on the XVME-203/293, and includes information for configuring the module before installation.

2.2 SYSTEM REQUIREMENTS

The XVME-203/293 10 Channel Counter Module is a VMEbus-compatible module. To operate, it must be properly installed in a VMEbus backplane. The minimum system requirements for operation of the module are one of the following (A or B):

A) A host processor installed in the same backplane

**** AND ****

A properly installed controller subsystem. An example of such a subsystem is the XYCOM XVME-010 System Resource Module.

**** OR ****

B) A host processor which incorporates an on-board controller subsystem (such as the XVME-600 or XVME-601 68000 Processor Module).

2.3 LOCATIONS OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers and connectors on the module are illustrated in Figure 2-1 (XVME-203), and Figure 2-1A (XVME-293).

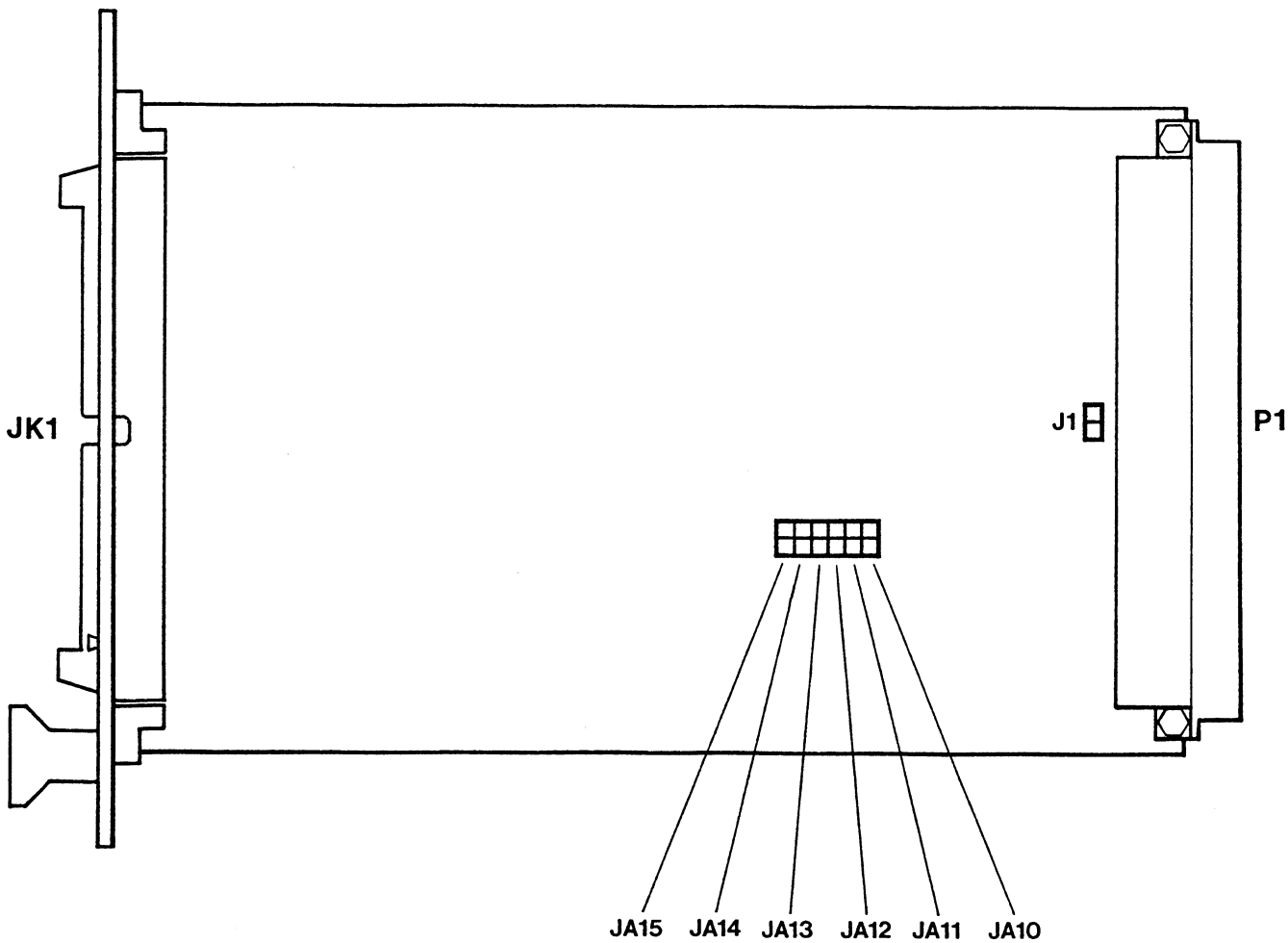


Figure 2-1. XVME-203 Jumpers and Connectors

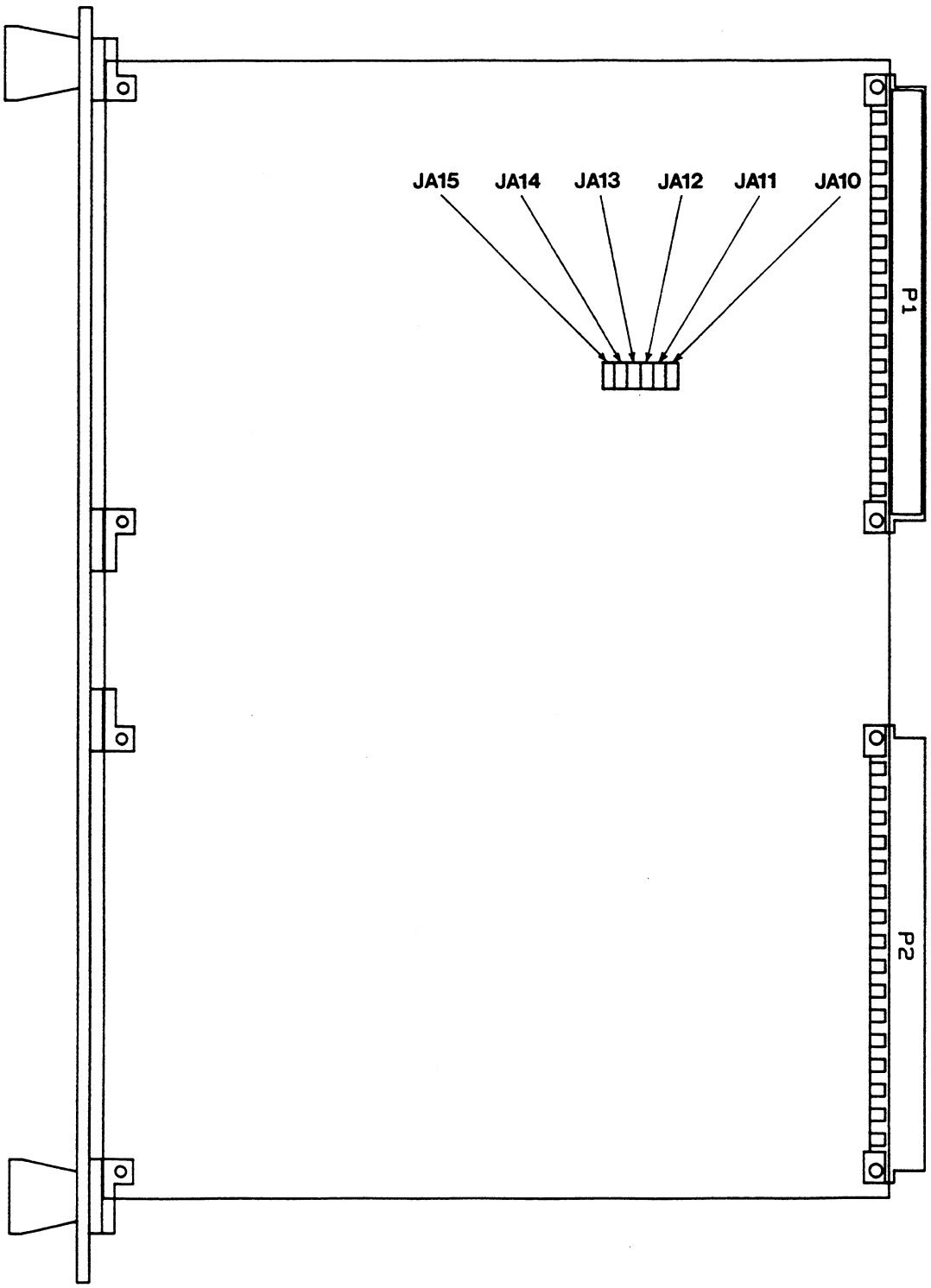


Figure 2-1A. XVME-293 Jumpers and Connectors

2.4 JUMPERS

Prior to installing the XVME-203/293 module, several jumper options must be configured. The configurations of the jumpers are dependent upon the module capabilities required for a particular application.

Table 2-1 lists the various jumpers and their uses.

Table 2-1. XVME-203/293 Jumper Options

VMEbus OPTIONS	
Jumpers	Use
JAl0, JAl1, JA12, JA13, JA14, JA15	Module base address select jumpers (refer to section 2.4.2)
Jl	This jumper allows the module to respond to supervisory access only (when installed) or to both supervisory and non-privileged access (when removed; Section 2.4.3)

2.4.1 VMEbus OPTIONS

The XVME-203/293 is designed to be addressed within the VMEbus Short I/O Memory Space. Since each module connected to the bus must have its own unique base address, the base-addressing scheme for XVME input modules has been designed to be jumper-selectable. When the XVME-203/293 is installed into the system, it will occupy a lK-byte block of Short I/O Memory Space.

The XYCOM base address decoding scheme for input modules is such that the starting address for a module will always reside on a IK boundary. Thus, the module base address may be set for any one of 64 possible 1K boundaries within the Short I/O Address Space.

2.4.2 Module Base Address Selection Jumpers (JAl5, JA14, JA13, JA12, JA11, JAl0)

The module base address is selected by using the jumpers JAl5-JAlO (see Figure 2-1 for the locations on the XVME-203 and Figure 2-1A for the XVME-293). Figure 2-2 shows a close-up of the base-address jumpers and how each jumper relates to the address lines.

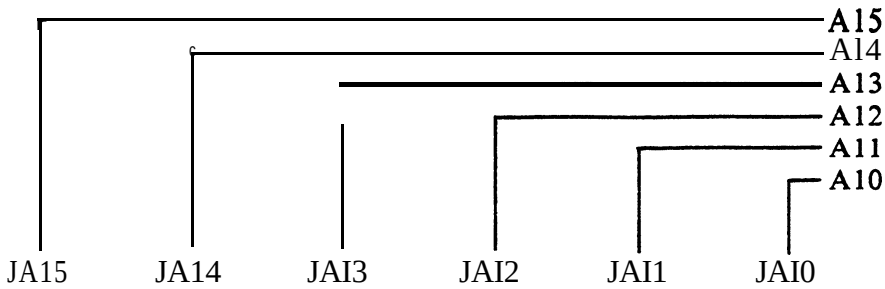


Figure 2-2. Base Address Jumpers

When a jumper is INSTALLED, the corresponding base address bit will be logic '0'. However, when a jumper is REMOVED, the corresponding base address bit will be logic '1'.

Table 2-2 shows a list of the 64 IK boundaries which can be used as module base addresses in the Short I/O Address Space (as well as the corresponding jumper settings for each address).

Table 2-2. Base Address Jumper Options

Jumpers						VME base address in VME Short I/O Address Space
JA15	JA14	JA13	JA12	JA11	JA10	
IN	IN	IN	IN	IN	IN	0000H
IN	IN	IN	IN	IN	OUT	0400H
IN	IN	IN	IN	OUT	IN	0800H
IN	IN	IN	IN	OUT	OUT	0C00H
IN	IN	IN	OUT	IN	IN	1000H
IN	IN	IN	OUT	IN	OUT	1400H
IN	IN	IN	OUT	OUT	IN	1800H
IN	IN	IN	OUT	OUT	OUT	1C00H
IN	IN	OUT	IN	IN	IN	2000H
IN	IN	OUT	IN	IN	OUT	2400H
IN	IN	OUT	IN	OUT	IN	2800H
IN	IN	OUT	IN	OUT	OUT	2C00H
IN	IN	OUT	OUT	IN	IN	3000H
IN	IN	OUT	OUT	IN	OUT	3400H
IN	IN	OUT	OUT	OUT	IN	3800H
IN	IN	OUT	OUT	OUT	OUT	3C00H
IN	OUT	IN	IN	IN	IN	4000H
IN	OUT	IN	IN	IN	OUT	4400H
IN	OUT	IN	IN	OUT	IN	4800H
IN	OUT	IN	IN	OUT	OUT	4C00H
IN	OUT	IN	OUT	IN	IN	5000H
IN	OUT	IN	OUT	IN	OUT	5400H
IN	OUT	IN	OUT	OUT	IN	5800H
IN	OUT	IN	OUT	OUT	OUT	5C00H
IN	OUT	OUT	IN	IN	IN	6000H
IN	OUT	OUT	IN	IN	OUT	6400H
IN	OUT	OUT	IN	OUT	IN	6800H
IN	OUT	OUT	IN	OUT	OUT	6C00H
IN	OUT	OUT	OUT	IN	IN	7000H
IN	OUT	OUT	OUT	IN	OUT	7400H
IN	OUT	OUT	OUT	OUT	IN	7800H
IN	OUT	OUT	OUT	OUT	OUT	7C00H
OUT	IN	IN	IN	IN	IN	8000H
OUT	IN	IN	IN	IN	OUT	8400H
OUT	IN	IN	IN	OUT	IN	8800H
OUT	IN	IN	IN	OUT	OUT	8C00H
OUT	IN	IN	OUT	IN	IN	9000H
OUT	IN	IN	OUT	IN	OUT	9400H
OUT	IN	IN	OUT	OUT	IN	9800H
OUT	IN	IN	OUT	OUT	OUT	9C00H
OUT	IN	OUT	IN	IN	IN	A000H
OUT	IN	OUT	IN	IN	OUT	A400H
OUT	IN	OUT	IN	OUT	IN	A800H
OUT	IN	OUT	IN	OUT	OUT	AC00H
OUT	IN	OUT	OUT	IN	IN	B000H
OUT	IN	OUT	OUT	IN	OUT	B400H
OUT	IN	OUT	OUT	OUT	IN	B800H
OUT	IN	OUT	OUT	OUT	OUT	BC00H
OUT	OUT	IN	IN	IN	IN	C000H
OUT	OUT	IN	IN	IN	OUT	C400H
OUT	OUT	IN	IN	OUT	IN	C800H
OUT	OUT	IN	IN	OUT	OUT	CC00H
OUT	OUT	IN	OUT	IN	IN	D000H
OUT	OUT	IN	OUT	IN	OUT	D400H
OUT	OUT	IN	OUT	OUT	IN	D800H
OUT	OUT	IN	OUT	OUT	OUT	DC00H
OUT	OUT	OUT	IN	IN	IN	E000H
OUT	OUT	OUT	OUT	IN	IN	F000H
OUT	OUT	OUT	OUT	IN	OUT	F400H
OUT	OUT	OUT	OUT	OUT	IN	F800H
OUT	OUT	OUT	OUT	OUT	OUT	FC00H

NOTE

IN = Logic "0"
OUT = Logic "1"

2.4.3 Supervisor/Non-Privileged Mode Selection

The XVME-203/293 can be configured to respond only to Supervisory accesses, OR to both Supervisory and Non-Privileged accesses. The key is the installation or removal of jumper **J1.** Table 2-3 shows access options controlled by **J1.**

Table 2-3. Access Options

Jumper J1	Access Mode Selection	Address Modifier Code
Installed	Supervisory Only	2DH
Removed	Supervisory or Non-Privileged	2DH or 29H

2.4.4 VMEbus Interrupt Options

The XVME-203/293 has the capability to generate interrupts on any one of seven levels (as allowed by the VMEbus specification). Interrupt levels for the module are set by the three least significant bits in the Status/Control register. Table 2-4 defines the interrupt options controlled by these bits.

Table 2-4. Interrupt Level Options

Bits (Set in Status/Control register)			
LS2	LS1	LS0	VMEbus Interrupt Level
0	0	0	None, Interrupts Disabled
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

2.5 CONNECTOR JKl

The counter input channels are accessible on the front of the XVME-203 via the single, 50-pin mass termination header labeled, JKl. Table 2-5 defines JKl's pin-out.

Table 2-5. Input Connector JKl

Pin Number	Signal	Pin Number	Signal
1	Ground	26	BCLOCK 0
2	ACLOCK 0	27	Ground
3	Ground	28	BGATE 0
4	AGATE 0	29	Ground
5	Ground	30	BCLOCK 1
6	ACLOCK 1	31	Ground
7	Ground	32	BGATE 1
8	AGATE 1	33	Ground
9	Ground	34	BCLOCK 2
10	ACLOCK 2	35	Ground
11	Ground	36	BGATE 2
12	AGATE 2	37	Ground
13	Ground	38	BCLOCK 3
14	ACLOCK 3	39	Ground
15	Ground	40	BGATE 3
16	AGATE 3	41	Ground
17	Ground	42	BOUT 0
18	AOUT 0	43	Ground
19	Ground	44	BOUT 1
20	AOUT 1	45	Ground
21	Ground	46	BOUT 2
22	AOUT 2	47	Ground
23	Ground	48	BOUT 3
24	AOUT 3	49	Ground
25	Ground	50	Ground

2.6 EXTERNAL CONNECTORS Pl and P2

2.6.1 Pl Connector

Connector Pl is mounted at the rear edge of the board (see Figure 2-1). The pin connections for Pl (a 96-pin, 3-row connector) contains the standard address, data, and control signals necessary for the operation of VMEbus-defined NEXP modules. (The signal definitions for the connector are found in Appendix A of this manual.) The Pl connector is designed to mechanically interface with a VMEbus defined Pl backplane (see Table 2-6).

Table 2-6. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DO0	BBSY *	DOS
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	Dl0
4	DO3	BGOIN*	Dll
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG20UT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
I1	GND	BG3OUT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A l1
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl”	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

2.6.2 P2 Connector (XVME-293 Only)

The P2 connector is mounted on the rear edge of the XVME-293 module and is a 96-pin, 3-row connector. This connector is functionally the same as the JKl except the signals are routed out the back of the module and the XVME-293 has five Output Channels (versus four for the XVME-203) and an FOUT. Row B is used as power and ground as per VMEbus specifications. Table 2-7 shows the pin designations for the P2 connector.

Table 2-7. Pin Assignment for P2 (XVME-293)

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
P2A-1	ACLOCKO	P2B-1	v c c	P2C-1	GND
P2A-2	AGATE0	P2B-2	GND	P2C-2	GND
P2A-3	ACLOCKl	P2B-3	NO CONNECT	P2C-3	GND
P2A-4	AGATE1	P2B-4	NO CONNECT	P2C-4	GND
P2A-5	ACLOCK2	P2B-5	NO CONNECT	P2C-5	GND
P2A-6	AGATE2	P2B-6	NO CONNECT	P2C-6	GND
P2A-7	ACLOCK3	P2B-7	NO CONNECT	P2C-7	GND
P2A-8	AGATE3	P2B-8	NO CONNECT	P2C-8	GND
P2A-9	AOUTO	P2B-9	NO CONNECT	P2C-9	GND
P2A-10	AOUTl	P2B-10	NO CONNECT	P2C-10	GND
P2A-11	AOUT2	P2B-11	NO CONNECT	P2C-11	GND
P2A-12	AOUT3	P2B-12	GND	P2C-12	GND
P2A-13	BCLOCKO	P2B-13	v c c	P2C-13	GND
P2A-14	BGATEO	P2B-14	NO CONNECT	P2C-14	GND
P2A-15	BCLOCKl	P2B-15	NO CONNECT	P2C-15	GND
P2A-16	BGATE1	P2B-16	NO CONNECT	P2C-16	GND
P2A-17	BCLOCK2	P2B-17	NO CONNECT	P2C-17	GND
P2A-18	BGATE2	P2B-18	NO CONNECT	P2C-18	GND
P2A-19	BCLOCK3	P2B-19	NO CONNECT	P2C-19	GND
P2A-20	BGATE3	P2B-20	NO CONNECT	P2C-20	GND
P2A-21	BOUT0	P2B-21	NO CONNECT	P2C-21	GND
P2A-22	BOUT1	P2B-22	GND	P2C-22	GND
P2A-23	BOUT2	P2B-23	NO CONNECT	P2C-23	GND
P2A-24	BOUT3	P2B-24	NO CONNECT	P2C-24	GND
P2A-25	NO CONNECT	P2B-25	NO CONNECT	P2C-25	GND
P2A-26	AOUT4	P2B-26	NO CONNECT	P2C-26	GND
P2A-27	AF'OUT	P2B-27	NO CONNECT	P2C-27	GND
P2A-28	BOUT4	P2B-28	NO CONNECT	P2C-28	GND
P2A-29	BFOUT	P2B-29	NO CONNECT	PC2-29	GND .
P2A-30	NO CONNECT	P2B-30	NO CONNECT	P2C-30	GND
P2A-31	NO CONNECT	P2B-31	GND	P2C-31	GND
P2A-32	NO CONNECT	P2B-32	v c c	P2C-32	GND

2.7 JUMPER LIST

The following table summarizes all the XVME-203/293 jumpers and their functions.

Table 2-8. XVME-203/293 Jumper List

Jumper	Description
J1	IN = supervisory only; OUT = supervisory or non-privileged
JAI0	Module base-address selection jumper (A10)
JAI1	Module base-address selection jumper (A11)
JA12	Module base-address selection jumper (A12)
JA13	Module base-address selection jumper (A13)
JA14	Module base-address selection jumper (A14)
JA15	Module base-address selection jumper (A15)

2.8 MODULE INSTALLATION

XYCOM XVME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-203 Module is a single-high VMEbus module, and as such, only requires the Pl backplane. The XVME-293 Module is a Double-high VMEbus module, it also requires the Pl backplane and can use the P2 backplane.

CAUTION

Never attempt to install or remove any module before turning the power to the bus OFF. Power to all related external power supplies should also be OFF.

Prior to installing the module, determine and verify all relevant jumper configurations. Check all connections to external devices or power supplies to make sure they comply with the specifications of the module. (Please check the jumper configuration against the diagrams and lists in this manual.)

To install the module into the cardcage (see Figure 2-3), perform the following steps:

1) Make sure the cardcage slot (which will hold the module) is clear and accessible.

2) Center the module on the plastic guides so the solder side is facing the left and the component side is facing right.

3) Push the card slowly toward the rear of the chassis, until the connectors engage (the card should slide freely in the plastic guides).

4) Apply straightforward pressure to the handles on the front panel front, until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excessive force or pressure to engage the connectors. If the board does not properly connect with the backplane, remove the module. Then inspect all connectors and guide slots for possible damage or obstructions.

5) Once the module is properly seated, secure it to the chassis by tightening the two machine screws at the extreme top and bottom of the module.

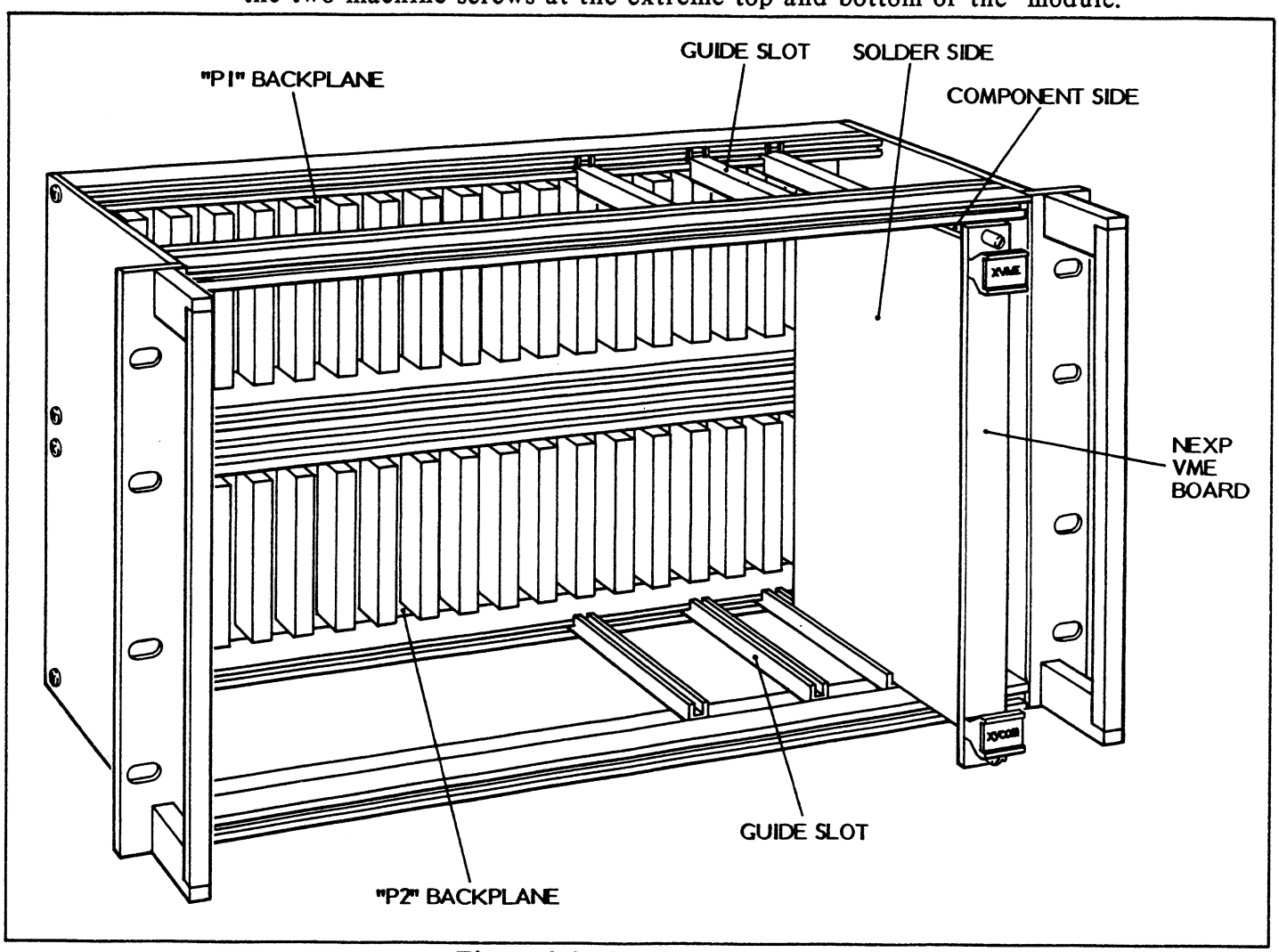


Figure 2-3. VMEbus Cardcage

2.9 INSTALLING A 6U FRONT PANEL KIT (optional XVME-203 Only)

XYCOM Model Number XVME-941 is an optional 6U front panel kit designed to replace the existing 3U front panel on the XVME-203. The 6U front panel facilitates the secure installation of single-high modules in those chassis which are designed to accomodate double-high modules. The following is a step-by-step procedure for installing the 6U front panel on an XVME-203 Module (refer to figure 2-4 for a graphic depiction of the installation procedure).

1. Disconnect the module from the bus.

2. Remove the screw and plastic collar assemblies (labeled #6 and #7) from the extreme top and bottom of the existing 3U front panel (#11), and install the screw assemblies in their corresponding locations on the 6U front panel.

3. Slide the module identification plate (labeled #13) from the handle (#9) on the 3U front panel. By removing the screw/nut found inside the handle, the entire handle assembly will separate from the 3U front panel. Remove the counter-sunk screw (#8) to separate the 3U front panel from the printed circuit board (#12).

4. Line-up the plastic support brackets on the printed circuit board with the corresponding holes in the 6U front panel (i.e. the holes at the top and top-center of the panel). Install the counter-sunk screw (#8) in the hole near the top center of the 6U panel, securing it to the lower support bracket on the printed circuit board.

5. Install the handle assembly (which was taken from the 3U panel) at the top of the 6U panel, using the screw and nut previously attached inside the handle. After securing the top handle, slide the module identification plate in place.

6. Finally, install the bottom handle (i.e. the handle that accompanies the kit (labeled #2) using the screw and nut (#3 & #5) provided. Slide the XYCOM VMEbus I.D. plate in place on the bottom handle. The module is now ready to be re-installed in the backplane.

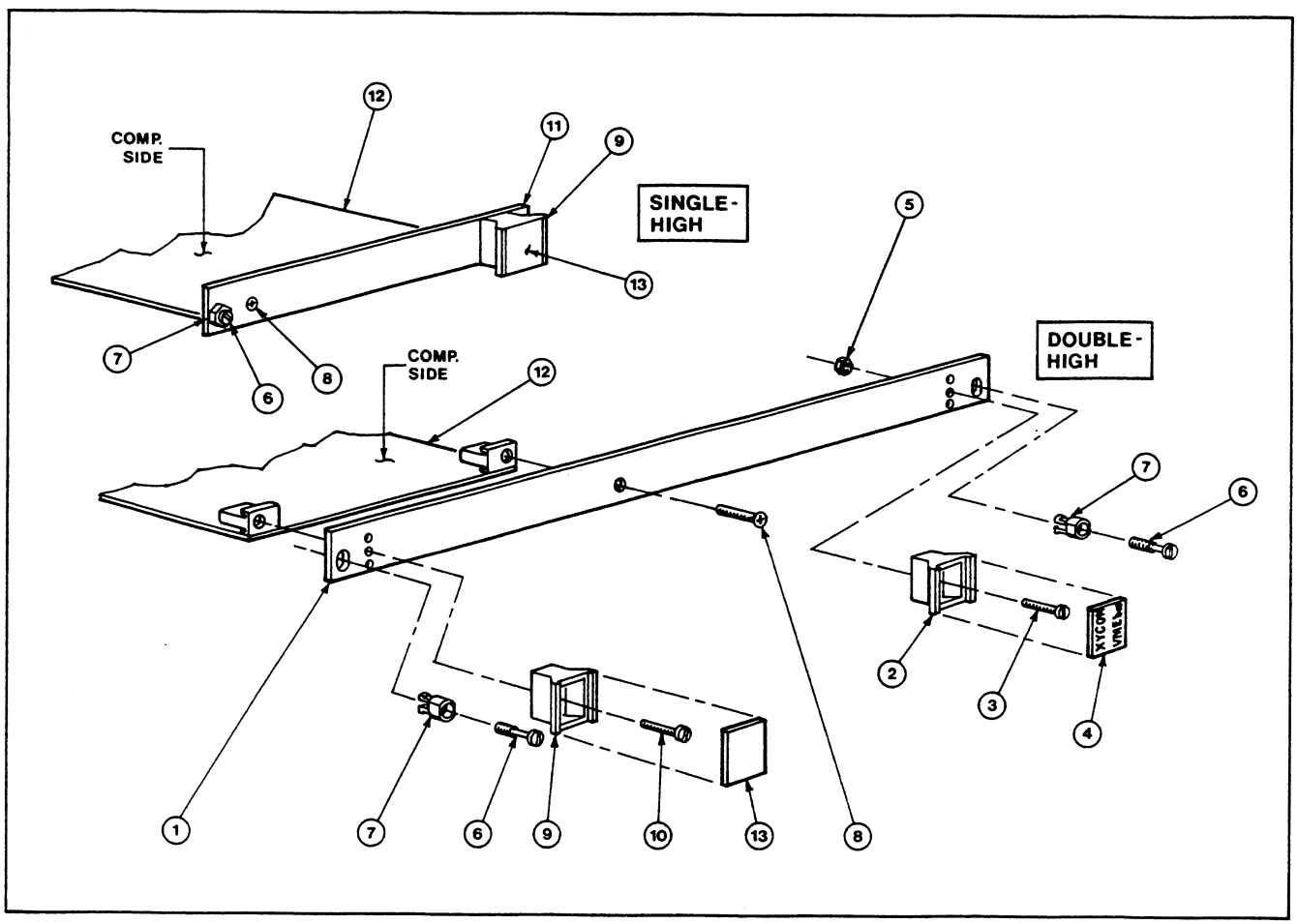


Figure 2-4. Installation of an XVME-941 6U Front Panel

Chapter 3

MODULE PROGRAMMING

3.1 INTRODUCTION

This chapter explains the XVME-203/293 memory map components. For specific information regarding the STC and the Universal Interrupt Controller, see the Am9513A and Am9519A manuals supplied with the board.

3.2 BASE ADDRESSING

The XVME-203/293 10 Channel Counter Module is designed to be addressed within the VMEbus-defined 64K Short I/O Address Space. When the module is installed in a system, it will occupy a 1K byte block of the Short I/O Address Space. The base address decoding scheme for the XVME I/O modules positions the starting address for each board on a 1K boundary. Thus, there are 64 possible base addresses (1K boundaries) for the XVME-203/293 within the Short I/O Address Space. (Refer to Section 2.4.2 for the list of base addresses and their corresponding list of jumper configurations.)

The logical registers utilized for the conversion data on the XVME-203/293 are given specific addresses within the 1K of block-address space occupied by the module. These addresses are offset from the module base address. Figure 3-1 shows a representative memory map for the XVME-203/293 module.

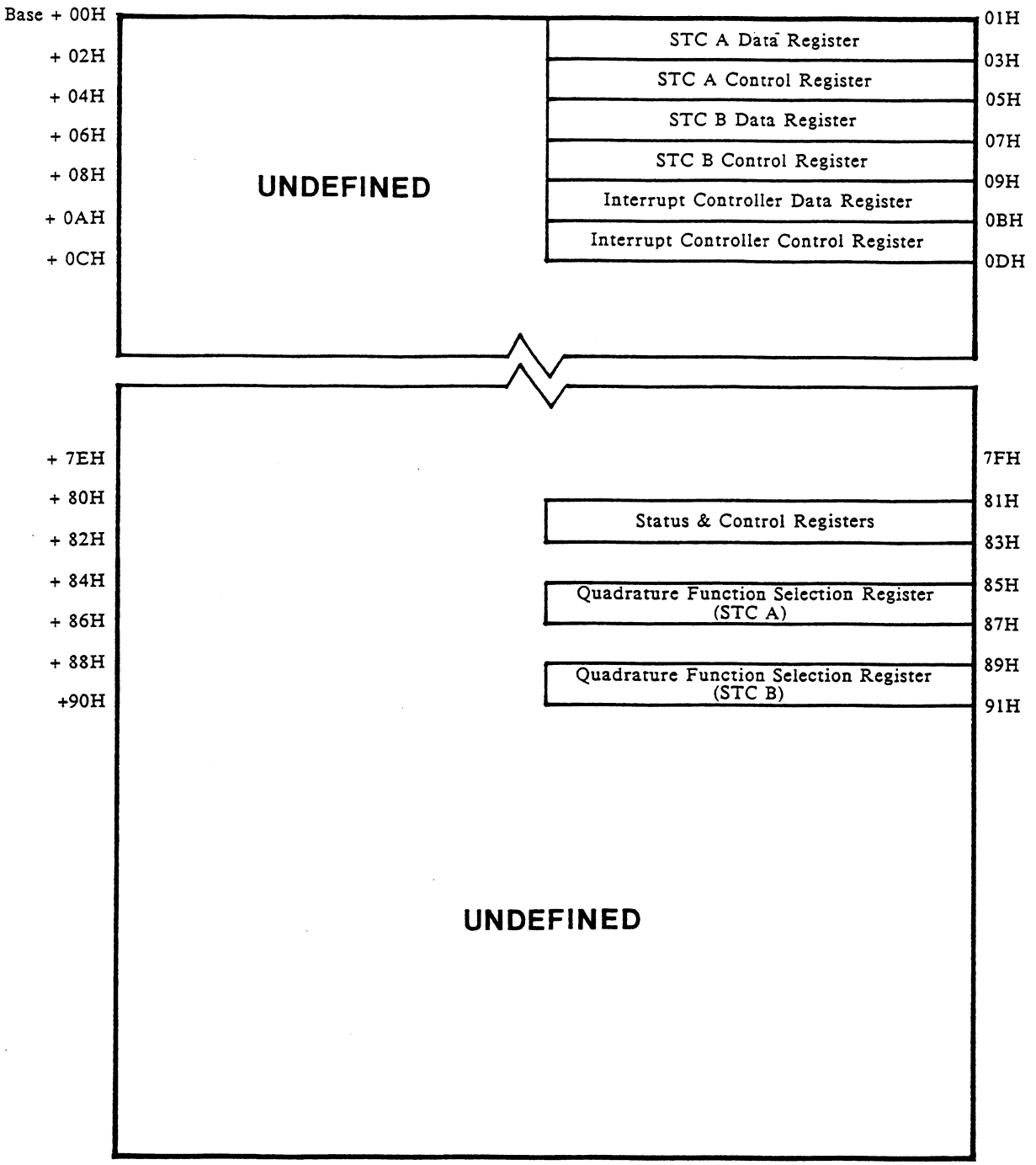


Figure 3-1. XVME-203/293 Memory Map

A specific register on the module can be accessed by simply adding the specific register offset the module base address. For example, the module Status/Control Register is located at address 81H within the I/O interface block. Thus, if the module base address is jumpered to 1000H, the Status/Control Register would be accessible at address 1081H.

(Module base address)		(Register offset)		(Status/Control Reg.)
1000H	+	81H	=	1081H

For memory-mapped CPU modules (such as 68000 CPU modules), the short I/O address space is memory-mapped to begin at a specific address. For such modules, the register offset is an offset from the start of this memory-mapped short I/O address space. For example, if the short I/O address space of a 68000 CPU module starts at F90000H, and if the base address of the XVME-203/293 is set at 1000H, then the actual module base address would be F91000H.

3.3 INTERFACE BLOCK

Each of the following programming locations of the XVME-203/293 interface block (previously shown in Figure 3-1) are defined in greater detail in this chapter's remaining sections. The module is an odd-byte only VMEbus slave. Word, even-byte or odd-byte accesses may be used. However, the module does not respond to accesses on the even bytes.

Status/Control Register (base + 81H): (Section 3.3.1) This register provides eight single-bit locations that enable and disenable STC outputs and determine VMEbus interrupt levels.

Interrupt Controller

Data Register (base + 09H): (Section 3.3.2.1) This eight-bit port corresponds to the Am9519A (universal interrupt controller) data register

Control Register (base + OBH): (Section 3.3.2.1) This eight-bit port corresponds to the Am9519A control register

System Timing Controller

Data Register A (base + OlH): (Section 3.3.3.1) This eight-bit port corresponds to the data register on STC **A**

Control Register A (base + 03H): (Section 3.3.3.1) This eight-bit port corresponds to the control register on STC A

Data Register B (base + 05H): (Section 3.3.3.1) This eight-bit port corresponds to the data register on STC B

Control Register B (base + 07H): (Section 3.3.3.1) This eight-bit port corresponds to the control register on STC B

Ouadrature Selection Registers

STC A (base + 85H): (Section 3.3.4) This eight-bit port determines whether or not a connection is made with the quadrature-select circuitry on STC A

STC B (base + 89H): (Section 3.3.4) This eight-bit port determines whether or not a connection is made with the quadrature-select circuitry on STC B

3.3.1 Status/Control Register

The status/control register on the XVME-203/293 is a dual, eight-bit register. The least significant bits (Bits O-3) allow access to the WRITE-ONLY Control Register. The most significant bits (Bits 4-7) give READ-ONLY access to the Status Register.

The following sections describe the Control Register and Status Register in more detail.

3.3.1.1 Control Register Bit Definitions

The control register selects the VMEbus interrupt levels for the XVME-203/293, and enables the STC output buffers. This is a WRITE-ONLY register. Only the four least significant bits (D3 - DO) can be written to. Figure 3-2 defines the four bit locations.

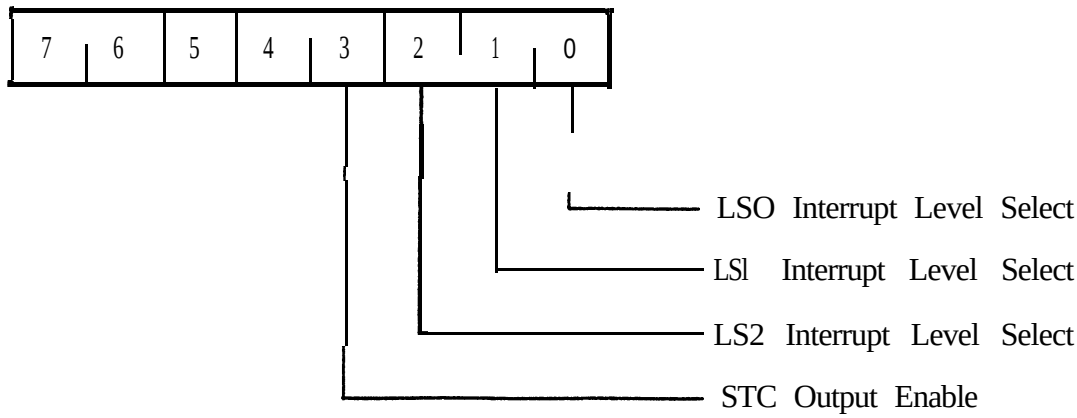


Figure 3-2. Control Register (WRITE ONLY)

The following is a bit-by-bit description of the control register:

Bit Number	Description
DO thru D2	These are the three "least significant bits" (LSO,LSl & LS2). They are used to select the VMEbus interrupt vector level (WRITE-ONLY). For convenience, the table showing the bit settings for selecting interrupts is repeated below (Table 3-1).

Table 3-l. Interrupt Level Options

Bits (Set in Control register)			
LS2	LS1	LS0	VMEbus Interrupt Level
0	0	0	None, Interrupts Disabled
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

D3 This bit provides a means for 'enabling' and 'disabling' the STC outputs to the ribbon connector. A logic '1' written to this location 'enables' STC outputs (WRITE-ONLY).

3.3.1.2 Status Register Bit Definitions

The status register offers READ-ONLY updating of information in the control register (bits D3-DO) and in the four quadrature circuits (bits D7-D4). Figure 3-3 defines the bits read in the status register.

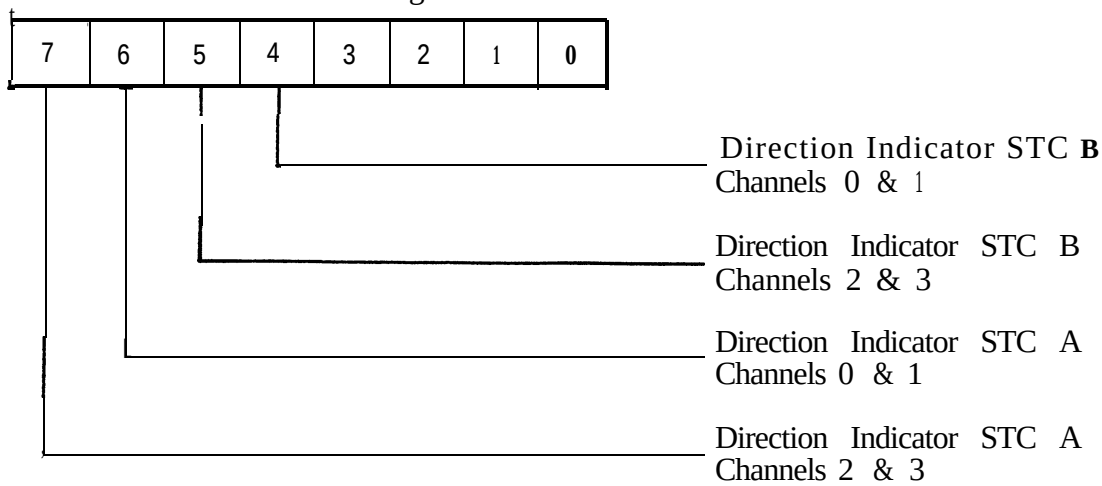


Figure 3-3. Status Register (READ ONLY)

The following is a bit-by-bit description of the status register:

Bit Number	Description
D4 thru D7	These are **READ-ONLY** bits describing the directions of each of the four quadrature circuits in STCs A & B. Table 3-2 shows the settings for the various bits, and their corresponding channels.

Table 3-2. Direction Indicator Bits

	Channel Numbers	Bit Numbers	Clockwise Bit Setting	Counterclockwise Bit Setting
STC B	0&l	7	0	I
	2&3	6	0	1
STC A	0&l	5	0	1
	2&3	4	0	1

3.3.2 **Interrupt Controller**

The on-board interrupt source for the XVME-203/293 is the Am9519A Universal Interrupt Controller. This manual will discuss specific registers for the chip but is not intended to be a full information source. More information, if necessary, can be found in the Universal Interrupt Controller manual provided with the module.

The interrupt controller provides eight interrupt (input) channels. Four of the channels are connected to four 'STC A' outputs. The other four are connected to four 'STC B' outputs. Table 3-3 shows which Am9519A interrupt request channels correspond with which 'STC A' and 'STC B' outputs.

Table 3-3. Interrupt Controller Connections

STC A outputs	STC B outputs	Interrupt Controller Inputs
AOUTO	---	IREQO
AOUTl	---	IREQl
AOUT2	---	IREQ2
AOUT3	---	IREQ3
---	BOUT0	IREQ4
---	BOUT1	IREQ5
---	BOUT2	IREQ6
---	BOUT3	IREQ7

3.3.2.1 Interrupt Controller Control & Data-Registers (Base + 09H, and Base + 0BH)

The control and data registers on the XVME-203/293 are ports that correspond to the Control/Data Input on the Am9519A (universal interrupt controller). Each register is eight bits long. The data port corresponds to the data register on the Am9519A (see the Am9519A Handbook). This control port corresponds to the control register on the Am9519A.

3.3.3 The System Timing Controller (STC)

The XVME-203/293 has two STCs. Each STC contains five 16-bit counters and a 4 bit pre-scaler. The counters may be concatenated to form a single counter (up to 8 0 bits long). Concatenated counters must be arranged in a strict sequential order (1 to 2 to 3 to 4 to 5 to 1 to 2..., etc where 5 always follows 4 and 1 always Follows 5).

NOTE

The System Timing Controller on the XVME-203/293 is a versatile source for coordinating timing sequences. Uses for the STC are expansive. This manual has limited information regarding use of the STC. For more detailed information, refer to the Am9513A manual provided with the module.

Each counter has two inputs (source and gate) and one output (terminal count). All counters can be programmed to accept one of four different count sources. They are:

- the previous counters terminal count output
- any of the counters source inputs SRCl-SRC5
- any of the counters gate inputs GATEl-GATE5
- any of five internally developed frequencies

Four of the SRC and GATE inputs to ‘each STC are derived from four clock and gate inputs to the board. Inputs CLOCK 0 through CLOCK 3 (and GATE 0 through. GATE 3) are connected to source inputs SRCI through SRC4 (and GATE 1 through GATE 4). SRC5 and GATE5 are also used but they are not connected to any off-board signals (see Table 3-4).

Each of the choices in the prior paragraph are made by the programming of the STC counter mode register. In addition to these selections, the XVME-203/293 allows the CLOCK 0 through 3 inputs to be pre-processed by quadrature detection circuitry. CLOCK inputs O/l form the CWO/CCWO quadrature pair. CLOCK inputs 2/3 form the CWl/CCWl quadrature pair.

3.3.3.1 STC Control Registers and Data Registers
(Base + 03H, Base + 07H) (Base + 0lH, Base + 05H)

The STC is addressed by external systems as only two locations: a control port or a data port. Transfers at the control port allow direct access to the command register (write) and status register (read). All other internal locations are accessed for read and write operations via the data port. Transfers to and from the control port are always S-bits wide.

The following paragraphs briefly discuss the roles of the four elements in the control port registers (see page 1-5, STC manual).

The Command Register provides direct control over each of the five general counters (S1- S5). It controls access through the Data Pointer register. Logic '1' on an S-bit indicates the specified counter is active. For a complete list of the commands for this register, see page 1-26 of the STC manual.

The Data Pointer Register consists of a 3-bit 'group' pointer, a 2-bit 'element' pointer, and a l-bit 'byte' pointer. The byte pointer indicates which byte of a 16-bit register is to be transferred through the next Data Port access. The element and group pointers are used to choose which internal register is to be accessed via the Data Port (see figure 1-9, page 1-6, STC manual).

The Pre-fetch Circuit is used for all read/write operations associated with the Data Port to minimize access time to internal STC registers. Pre-fetches are also performed after the "Load Data Pointer" command. After each read/write operation via the Data Port, the Data Pointer register is updated to point to the next register to be accessed.

The Status Register (S-bit, READ-ONLY) register indicates the states of the byte-pointer bit in the Data Pointer and the OUT signals for each general counter. The status register is normally accessed via the Control Port, but may also be read via the Data Port as part of the Control Group (page 1-8 STC manual).

3.3.4 Quadrature Selection Registers
(Base + 85H, Base + 89H)

The Quadrature function select register provides the means to select between the clock inputs or to pre-process the clock inputs through the quadrature detection circuitry. Table 3-4 illustrates the quadrature selection process.

Table 3-4. Quadrature Selection

STC INPUT	Signal name: Quadrature selected	Signal name: Quadrature not selected
SRCl	CLOCK 0	CLOCK 0
SRC2	CLOCK 1	CLOCK 1
SRC3	CW I	CLOCK 2
SRC4	CCW 1	CLOCK 3
SRC5	CW 0	CW 0
GATE1	GATE 0	GATE 0
GATE2	GATE I	GATE 1
GATE3	GATE 2	GATE 2
GATE4	GATE 3	GATE 3
GATE5	CCW 0	CCW 0

STC inputs SRC5 and GATE5 are permanently connected to CW 0 and CCW 0, respectively. They are not connected to any off board clock signals. Although this limits external sources of counting, it does not prevent the selection of any other STC internal source. When the quadrature function is selected, only SRC3 and SRC4 are affected.

3.3.4.1 Quadrature Selection Register Bit Definitions

Both XVME-203/293 STCs are equipped with a quadrature register. The bit assignments for each register are identical. The quadrature function selection register must be programmed to enable the quadrature detection circuitry for either STC.

To enable quadrature detection from this register, the least significant bit must be set to logic '1'. The bit is reset to logic '0' at power-up (disabling quadrature detection).

As Figure 3-4 shows, bits D7 thru Dl on this register are not used by the XVME-203/293.

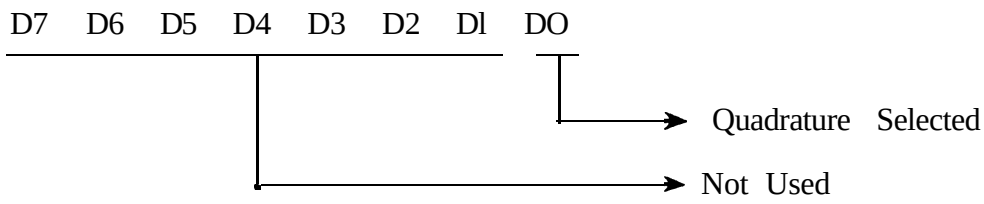


Figure 3-4. Quadrature Selection Register Bits

3.3.4.2 Quadrature Detector

The quadrature detector uses three circuits: Quadrature Detect Logic Array, Digital Delay Line, and Status Register.

A quadrature position transducer generates three signals SIN, COS and INDEX. SIN and COS signals are used to calculate the number of steps a rotating device makes in a clockwise or counterclockwise direction. The COS signal is 90 degrees out of phase with the SIN signal. The INDEX signal is active when the transducer shaft is at the zero degree position. Not all transducers produce an INDEX signal.

The XVME-203/293 is designed to operate with as many as four quadrature transducers. When a channel on the module is to be used as a quadrature position detector the transducer must be connected as follows:

The EVEN-numbered CLOCK input (0 or 2) of a particular channel is connected to the SIN output of the transducer.

The ODD-numbered CLOCK input 1 (or 3) is connected to the COS output of the transducer.

The INDEX signal (if generated) must be connected to one of the GATE inputs (O-3).

CLOCK inputs O/l and 2/3 thus form two SIN/COS pairs of signals that are routed to the each of the STC's. Each STC is capable of handling two sets of quadrature signals.

When the transducer is rotated in the clockwise direction a pulse will appear on the CW output of the logic array. If the transducer rotates in the counter-clockwise direction a pulse will appear on the CCW output of the logic array. The width of the pulse generated is equal to the amount of time it takes for the delayed SIN or COS to follow the SIN or COS signal (100-200 ns).

3.4 PROGRAMMING EXAMPLES

The following three sections contain examples of programming the Am9513A on the XVME-203/293 for operating the chip's frequency measurement, "Mode E" and "Mode D" features.

3.4.1 Example One: Frequency Measurement

```
ASMID   68000
LIST    CON,ME,PAGE(62),SYM,XREF
NOLIST  CND,DBG
GEN.L


FREQ
        rate generator MODE D

ORG     800000H

CNTMOD  EQU     0F90000H        ;XVME-203 BASE ADDRESS
DIO     EQU     0F90400H        ;XVME-200 BASE ADDRESS
STCAD   EQU     0F9000lH        ;STC 'A' DATA REGISTER
STCAC   EQU     0F90003H        ;STC 'A' CONTROL REGISTER
STCBD   EQU     0F90005H        ;STC 'B' DATA REGISTER
STCBC   EQU     0F90007H        ;STC 'B' CONTROL REGISTER
ICTRD   EQU     0F90009H        ;INTERRUPT CONTROLLER DATA
                                ;REGISTER
ICTRC   EQU     0F9000BH        ;INTERRUPT CONTROLLER CONTROL
                                ;REG.


9513A
INITIALIZATION

        NOP
        NOP
        M0VE.B  #OFFH,STCAC     ;Reset cntr 1
        M0VE.B  #OE7H,STCAC     ;Cntr 1, 8 bit bus mode

        M0VE.B  #SFH,STCAC      ;Load the reset counters
        M0VE.B  #OEEH,STCAC     ;Turn gate off
        M0VE.B  #17H,STCAC      ;Set data ptr to Master mode register
        M0VE.B  #OOH,STCAD      ;Disable auto incr. LSB
        M0VE.B  #40H,STCAD      ;MSB

                                ;Set data pointer to
        M0VE.B  #01H,STCAC      ;Cntr 1 Mode register
        M0VE.B  #21H,STCAD      ;Set cntr 1 mode reg.
        M0VE.B  #OBH,STCAD      ;Mode D rate gen no gating
```

```
                                    ;Set data pointer to
M0VE.B    #09H,STCAC                ;Cntr 1 load register
M0VE.B    #08H,STCAD                ;Set cntr 1 load reg. LSB
M0VE.B    #OOH,STCAD                ;MSB

M0VE.B    #6 1 H,STCAC              ;Load and Arm cntr 1

TRAP      #15                       ;End
WORD      0000H
END
```

3.4.2 Example Two: External Gating

```
        ASMID 68000
        LIST  CON,ME,PAGE(62),SYM,XREF
        NOLIST CND,DBG
        GEN.L



    extgate PROGRAM


MON.START   EQU   0000H     ;RETURN T O 68OMON
CR          EQU   0DH       ;CARRIAGE RETURN
LF          EQU   0AH       ;LINE FEED
CNTMOD      EQU   0F90000H  ;XVME-203 BASE ADDRESS
DI01        EQU   0F90400H  ;PITl BASE ADDRESS
D102        EQU   0F90440H  ;PIT2 BASE ADDRESS
DI01TCR     EQU   0F90421H  ;PITl TIMR CNTRL REG
DI02TCR     EQU   0F90461H  ;PIT2 TIMR CNTRL REG
DIOlCPRH    EQU   0F90427H  ;PITl COUNT PRELOAD REG HIGH
DIOlCPRM    EQU   0F90429H  ;PITl COUNT PRELOAD REG MID
DIOlCPRL    EQU   0F9042BH  ;PITl COUNT PRELOAD REG LOW
DI02CPRH    EQU   0F90467H  ;PIT2 COUNT PRELOAD REG HIGH
DI02CPRM    EQU   0F90469H  ;PIT2 COUNT PRELOAD REG MID
DI02CPRL    EQU   0F9046BH  ;PIT2 COUNT PRELOAD REG LOW
STCAD       EQU   0F90001H  ;STC 'A' DATA REGISTER
STCAC       EQU   0F90003H  ;STC 'A' CONTROL REGISTER
STCBD       EQU   0F90005H  ;STC 'B' DATA REGISTER
STCBC       EQU   0F90007H  ;STC 'B' CONTROL REGISTER
UICD        EQU   0F90009H  ;INTERRUPT CONTROLLER DATA
                            ;REGISTER
UICC        EQU   0F9000BH  ;INTERRUPT CONTROLLER CONTROL
                            ;REG.
LEl         EQU   0F90085H  ;QUAD LATCH #l CHIP SELECT
LE2         EQU   0F90089H  ;QUAD LATCH #2 CHIP SELECT
MDL         EQU   21H       ;MODE LSB
MDH         EQU   0AIH      ;MODE MSB
VL          EQU   02H       ;COUNT VALUE LSB
VH          EQU   00H       ;COUNT VALUE MSB
```

```
        ORG  $00000H


INITIALIZATION


    9513A
INITIALIZATION


        ,
        M0VE.B   #OFFH,STCAC      ;Reset cntr A
        M0VE.B   #0E7H,STCAC      ;Cntr A, 8 bit bus mode
        M0VE.B   #5FH,STCAC       ;Load and clear TC outputs

                                  ;Set data pointer to
        M0VE.B   #17H,STCAC       ;Select master mode register
        M0VE.B   #OOH,STCAD       ;
        MOVE.B   #OOH,STCAD       ;enable auto incr.
        '
        M0VE.B   #0 1 H,STCAC     ;Select cntr 1 mode register
        M0VE.B   #MDL,STCAD       ;Load 1st byte of mode
        M0VE.B   #MDH,STCAD       ;Load 2nd byte of mode
        M0VE.B   #VL,STCAD        ;Load 1st byte of load reg
        M0VE.B   #VH,STCAD        ;Load 2nd byte of load reg
        ,
        MOVE.B   #02H,STCAC       ;Select cntr 2 mode register
        M0VE.B   #MDL,STCAD       ;Load 1st byte of mode
        M0VE.B   #MDH+ 1 ,STCAD   ;Load 2nd byte of mode
        M0VE.B   #VL,STCAD        ;Load 1st byte of load reg
        M0VE.B   #VH,STCAD        ;Load 2nd byte of load reg


        MOVE.B   #03HSTCAC        ;Select cntr 3 mode register
        M0VE.B   #MDL,STCAD       ;Load 1st byte of mode
        M0VE.B   #MDH+2,STCAD      ;Load 2nd byte of mode
        M0VE.B   #VL,STCAD        ;Load 1st byte of load reg
        M0VE.B   #VH,STCAD        ;Load 2nd byte of load reg

        ,
```

```
        M0VE.B   #04H,STCAC      ;Select cntr 4 mode register
        M0VE.B   #MDL,STCAD      ;Load 1st byte of mode
        M0VE.B   #MDH+3,STCAD    ;Load 2nd byte of mode
        M0VE.B   #VL,STCAD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCAD       ;Load 2nd byte of load reg
        ;

NEXT    M0VE.B   #OFFH,STCBC     ;Reset cntr B
        M0VE.B   #0E7H,STCBC     ;Cntr B, 8 bit bus mode
        M0VE.B   #5FH,STCBC      ;Load and clear TC outputs

                                 ;Set data pointer to
        M0VE.B   #17H,STCBC      ;Master mode register
        M0VE.B   #OOH,STCBD      ;
        M0VE.B   #OOH,STCBD      ;enable auto incr.

        ;MOVE.B   #01HSTCBC       ;Select cntr 1 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH,STCBD      ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg

        MOVE.B   #02H,STCBC      ;Select cntr 2 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+ 1 ,STCBD  ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg

        M0VE.B   #03H,STCBC      ;Select cntr 3 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+2,STCBD    ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg

        MOVE.B   #04H,STCBC      ;Select cntr 4 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+3,STCBD    ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg
        ;

        MOVE.B   #7FH,STCAC      ;LOAD AND ARM ALL COUNTERS 'A'
        M0VE.B   #7FH,STCBC      ;LOAD AND ARM ALL COUNTERS 'B'
```

```
            NOP
            NOP


      init  xvme-200


DIO         M0VE.B    #OOH,DIO 1 CPRH     ;SET DIOl COUNT PRELOAD REG HIGH
            M0VE.B    #OOH,DIO 1 CPRM     ;SET DIOl COUNT PRELOAD REG MID
            M0VE.B    #OFFH,DIOlCPRL      ;SET DIOl COUNT PRELOAD REG LOW
            NOP
            NOP
            M0VE.B    #OOH,DI02CPRH       ;SET D102 COUNT PRELOAD REG HIGH
            M0VE.B    #OOH,DI02CPRM       ;SET D102 COUNT PRELOAD REG MID
            M0VE.B    #OFFH,DI02CPRL      ;SET D102 COUNT PRELOAD REG LOW
            NOP
            NOP
            M0VE.B    #4 1 H,DIO 1 TCR    ;SET TIMR FOR SQUARE WAVE
            M0VE.W    #048H,DO
            NOP
            NOP
LOOP        SUB1.B    #IH,DO
            BNE       LOOP
            M0VE.B    #4 1H,DI02TCR       ;SET TIMR FOR SQUARE WAVE
            NOP
            NOP
TEST        MOVE.B    #3H,DIO 1+9H        ;SET PORT C DATA DIRECTION REG
            M0VE.B    #OH,DIO 1+19H       ;SET PORT C DATA REG
            MOVE.B    #30H,DIOl+lH        ;SET PORT GENERAL CONTROL REG
                                          ;MODE 0 UNI-8 BIT
            MOVE.B    #OOH,DIO 1+3H       ;SET PORT SERVICE REG
            M0VE.B    #OFFH,DIO 1+5H      ;SET PORT A DATA DIRECTION REG TO
                                          ;OUTPUT
            M0VE.B    #OOH,DIO 1 +ODH     ;SET PORT A CONTROL REGISTER
            M0VE.B    #OOH,DIOl+llH       ;START STCA CNTR #l BY ENABLING GlA


            TRAP      #15
            WORD      0000
```

3.4.3 Example Three: No Hardware Gating

```
ASMID     68000
LIST      CON,ME,PAGE(62),SYM,XREF
NOLIST    CND,DBG
GEN.L



modedext  PROGRAM



MON.START EQU   0000H     ;RETURN TO 680MON
CR        EQU   ODH       ;CARRIAGE RETURN
LF        EQU   OAH       ;LINE FEED
CNTMOD    EQU   OF90000H  ;XVME-203 BASE ADDRESS
DIOI      EQU   OF90401H  ;PITl GEN CNTRL REG ADDRESS
D102      EQU   OF90441H  ;PIT2 GEN CNTRL REG ADDRESS
DIOlTCR   EQU   OF90421H  ;PITl TIMR CNTRL REG
DI02TCR   EQU   OF90461H  ;PIT2 TIMR CNTRL REG
DIOICPRH  EQU   OF90427H  ;PITl COUNT PRELOAD REG HIGH
DIOlCPRM  EQU   OF90429H  ;PITl COUNT PRELOAD REG MID
DIOlCPRL  EQU   OF9042BH  ;PITl COUNT PRELOAD REG LOW
DI02CPRH  EQU   OF90467H  ;PIT2 COUNT PRELOAD REG HIGH
DI02CPRM  EQU   OF90469H  ;PIT2 COUNT PRELOAD REG MID
DIOIZCPRL EQU   OF9046BH  ;PIT2 COUNT PRELOAD REG LOW
STCAD     EQU   OF90001H  ;STC 'A' DATA REGISTER
STCAC     EQU   OF90003H  ;STC 'A' CONTROL REGISTER
STCBD     EQU   OF90005H  ;STC 'B' DATA REGISTER
STCBC     EQU   OF90007H  ;STC 'B' CONTROL REGISTER
UICD      EQU   OF90009H  ;INTERRUPT CONTROLLER DATA
                          ;REGISTER
UICC      EQU   OF9000BH  ;INTERRUPT CONTROLLER CONTROL
                          ;REG.
LEl       EQU   OF90085H  ;QUAD LATCH #1 CHIP SELECT
LE2       EQU   OF90089H  ;QUAD LATCH #2 CHIP SELECT
MDL       EQU   21H       ;MODE LSB
MDH       EQU   OIH       ;MODE MSB
VL        EQU   02H       ;COUNT VALUE LSB
VH        EQU   OOH       ;COUNT VALUE MSB


          ORG   800000H
```

INITIALIZATION

9513A
INITIALIZATION

```
;
;
M0VE.B    #OFFH,STCAC       ;Reset cntr A
M0VE.B    #OE7H,STCAC       ;Cntr A, 8 bit bus mode
M0VE.B    #5FH,STCAC        ;Load and clear TC outputs

                            ;Set data pointer to
MOVE.B  # 17H,STCAC         ;Select master mode register
M0VE.B    #OOH,STCAD        ;
M0VE.B    #OOH,STCAD        ;enable auto incr.

;
;
M0VE.B    #0 1 H,STCAC      ;Select cntr 1 mode register
M0VE.B    #MDL,STCAD        ;Load 1st byte of mode
M0VE.B    #MDH,STCAD        ;Load 2nd byte of mode
M0VE.B   #VL,STCAD          ;Load 1st byte of load reg
M0VE.B    #VH,STCAD         ;Load 2nd byte of load reg
,

MOVE.B    #02H,STCAC        ;Select cntr 2 mode register
M0VE.B    #MDL,STCAD        ;Load 1st byte of mode
M0VE.B    #MDH+ 1 ,STCAD    ;Load 2nd byte of mode
M0VE.B    #VL,STCAD         ;Load 1st byte of load reg
M0VE.B    #VH,STCAD         ;Load 2nd byte of load reg
;

MOVE.B    #03H  STCAC       ;Select cntr 3 mode register
M0VE.B    #MDL,STCAD        ;Load 1st byte of mode
M0VE.B    #MDH+2,STCAD      ;Load 2nd byte of mode
M0VE.B    #VL,STCAD         ;Load 1st byte of load reg
M0VE.B    #VH,STCAD         ;Load 2nd byte of load reg
,
;
```

```
        M0VE.B   #04H,STCAC      ;Select cntr 4 mode register
        M0VE.B   #MDL,STCAD      ;Load 1st byte of mode
        M0VE.B   #MDH+3,STCAD    ;Load 2nd byte of mode
        M0VE.B   #VL,STCAD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCAD       ;Load 2nd byte of load reg
        ;
        ;
NEXT    M0VE.B   #OFFH,STCBC     ;Reset cntr B
        M0VE.B   #OE7H,STCBC     ;Cntr B, 8 bit bus mode
        M0VE.B   #5FH,STCBC      ;Load and clear TC outputs
        ;
        ,
                                 ;Set data pointer to
        M0VE.B   # 17H,STCBC     ;Master mode register
        M0VE.B   #OOH,STCBD
        M0VE.B   #OOH,STCBD      ;enable auto incr.
        ,
        MOVE.B   #O 1 H,STCBC    ;Select cntr 1 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH,STCBD      ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg
        '
        MOVE.B   #02H,STCBC      ;Select cntr 2 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+ 1 ,STCBD  ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg
        ;
        ;
        M0VE.B   #03H,STCBC      ;Select cntr 3 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+2,STCBD    ;Load 2nd byte of mode
        M0VE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg
        ,
        M0VE.B   #04H,STCBC      ;Select cntr 4 mode register
        M0VE.B   #MDL,STCBD      ;Load 1st byte of mode
        M0VE.B   #MDH+3,STCBD    ;Load 2nd byte of mode
        MOVE.B   #VL,STCBD       ;Load 1st byte of load reg
        M0VE.B   #VH,STCBD       ;Load 2nd byte of load reg
        ,
        MOVE.B   #7FH,STCAC      ;LOAD AND ARM ALL COUNTERS 'A'
        M0VE.B   #7FH,STCBC      ;LOAD AND ARM ALL COUNTERS 'B'
```

```
            NOP
            NOP

      init  xvme-200

DIO         M0VE.B   #OOH,DIO 1 CPRH    ;SET DIOl COUNT PRELOAD REG HIGH
            M0VE.B   #OOH,DIOl CPRM     ;SET DIOl COUNT PRELOAD REG MID
            M0VE.B   #OFFH,DIO 1 CPRL   ;SET 0101 COUNT PRELOAD REG LOW
            NOP
            NOP
            MOVE.B   #OOH,DI02CPRH      ;SET D102 COUNT PRELOAD REG HIGH
            M0VE.B   #OOH,DI02CPRM      ;SET D102 COUNT PRELOAD REG MID
            M0VE.B   #OFFH,DI02CPRL     ;SET D102 COUNT PRELOAD REG LOW
            NOP
            NOP
            M0VE.B   #41H,DIOITCR       ;SET TIMR FOR SQUARE WAVE
            M0VE.W   #048H,DO
            NOP
            NOP
LOOP        SUB1.B   #lH,DO
            BNE      LOOP
            M0VE.B   #4 lH,DI02TCR      ;SET TIMR FOR SQUARE WAVE
            NOP
            NOP
TEST        M0VE.B   #30H,DIO 1         ;SET PORT GENERAL CONTROL REG
            M0VE.B   #OOH,DIO 1+2       ;SET PORT SERVICE REG
            M0VE.B   #OFFH,DIO 1+5      ;SET PORT A DATA DIRECTION REG
            M0VE.B   #OOH,DIO 1 +ODH    ;SET PORT A CONTROL REGISTER
            M0VE.B   #01H,DI01+11H      ;START STCA CNTR #l BY ENABLING GlA


            TRAP     #15
            WORD     0000
```

Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-203 is physically configured as a non-expanded (NEXP), single-height, VMEbus-compatible board. There is one 96-pin bus connector on the rear edge of the board, labeled Pl. The pin connections for PI contain the standard address, data and control signals necessary for the operation of NEXP modules.

Table A-l. Pl - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	lA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1 A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AMO-AM5	1A:23 lB:16,17, 18,19 lC:14	ADDRESS MODIFIER (bits O-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	lA:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A0l-A23	1A:24-30 lC:15-30	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:l	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	lB:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:ll	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BGOIN*- BG3IN*	1B:4,6, 8,l0	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BGOOUT*- BG30UT*	1B:5,7, 9,ll	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (O-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DSO*	IA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSI*	lA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D15).
DTACK*	1A:l6	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22, 31	GROUND

Table A- 1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	**1A:20**	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQl*-IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	**1B:22**	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	lA:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5v	1 A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12V	lA:31	-12 VDC POWER: Used by system logic circuits.

BACKPLANE CONNECTOR Pl

The following table lists the Pl pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DO0	BBSY*	DO8
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	DlO
4	DO3	BGOIN*	Dll
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG30UT*	BERR*
12	DSI*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	All
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5v	+5v

Appendix B

QUICK REFERENCE GUIDE

This chapter contains the following XVME-203 tables for easy reference:

- XVME-203 I/O Interface Block (Memory Map; Figure 3-1)
- Control Register Bits (Figure 3-2)
- Status Register Bits (Figure 3-3)
- Direction Indicator Bits (Table 3-2)
- Jumper Options (Table 2-l)
- Jumper List (Table 2-6)
- Base Address Jumper Options (Table 2-2)
- Input Connector JKI (Table 2-5)
- Module Base Address List (Table 2-3)
- Interrupt Controller Connections (Table 3-3)
- Quadrature Selection (Table 3-4)

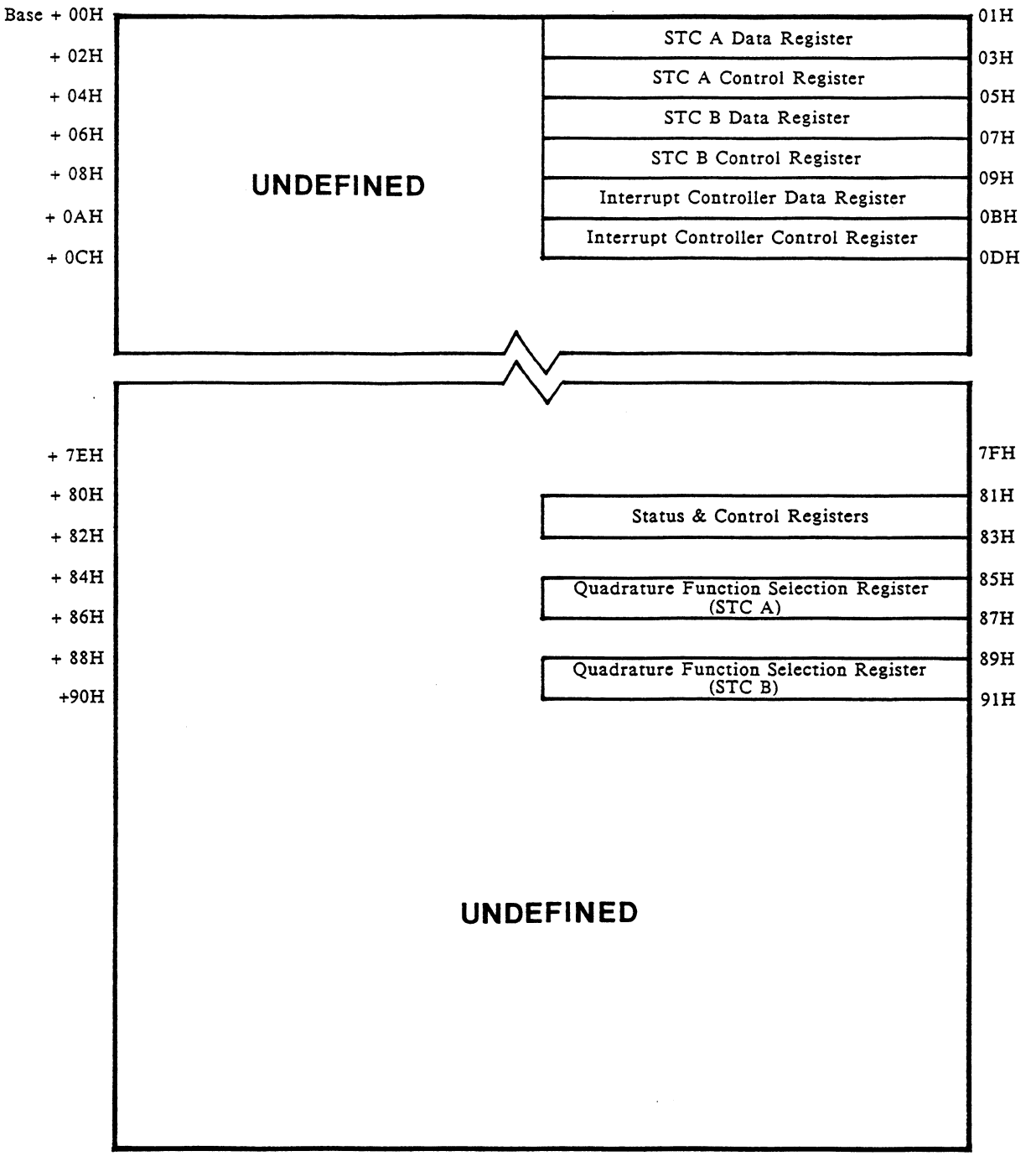


Figure B-1. XVME-203/293 Memory Map

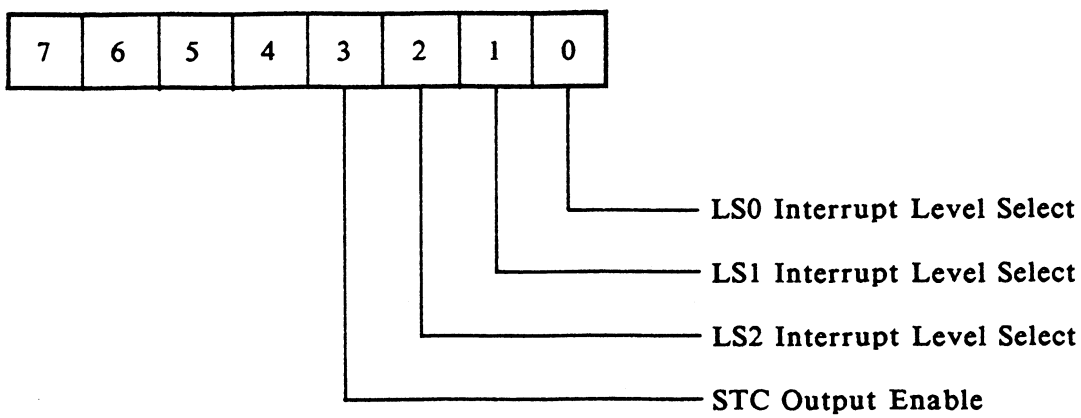


Figure B-2. Control Register (Write Only)

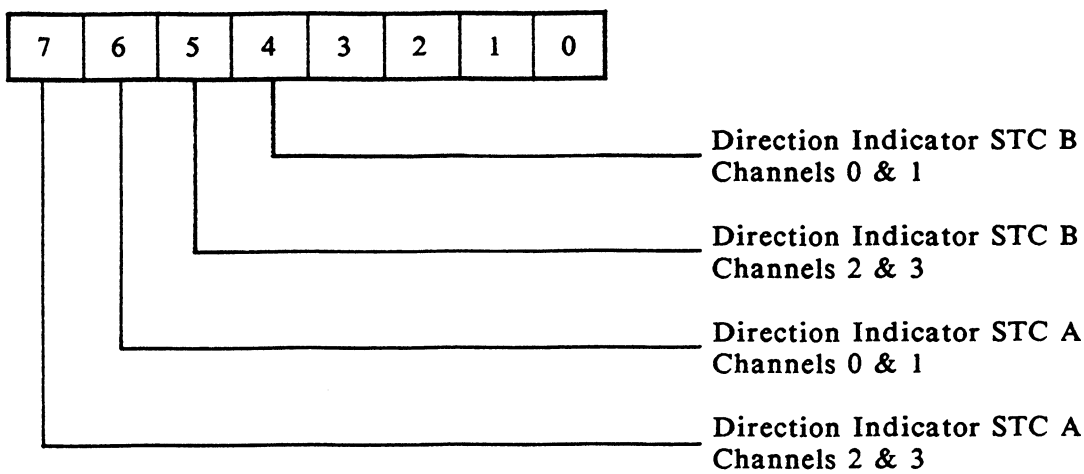


Figure B-3. Status Register (READ ONLY)

Table B-l. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY *	DOS
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	D10
4	DO3	BG0IN*	Dll
5	DO4	BGOOUT*	D12
6	DO5	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG20UT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG30UT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5V STDBY	+12v
32	+5v	+5V	+5V

Table B-2. Pin Assignment for P2 (XVME-293)

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
P2A-1	ACLOCKO	P2B-1	v c c	P2C-1	GND
P2A-2	AGATE0	P2B-2	GND	P2C-2	GND
P2A-3	ACLOCKl	P2B-3	NO CONNECT	P2C-3	GND
P2A-4	AGATE1	P2B-4	NO CONNECT	P2C-4	GND
P2A-5	ACLOCK	P2B-5	NO CONNECT	P2C-5	GND
P2A-6	AGATE2	P2B-6	NO CONNECT	P2C-6	GND
P2A-7	ACLOCK3	P2B-7	NO CONNECT	P2C-7	GND
P2A-8	AGATE3	P2B-8	NO CONNECT	P2C-8	GND
P2A-9	AOUTO	P2B-9	NO CONNECT	P2C-9	GND
P2A-10	AOUTl	P2B-10	NO CONNECT	P2C-10	GND
P2A-11	AOUT2	P2B-11	NO CONNECT	P2C-11	GND
P2A-12	AOUT3	P2B-12	GND	P2C-12	GND
P2A-13	BCLOCKO	P2B-13	v c c	P2C-13	GND
P2A-14	BGATEO	P2B-14	NO CONNECT	P2C-14	GND
P2A-15	BCLOCKl	P2B-15	NO CONNECT	P2C-15	GND
P2A-16	BGATEl	P2B-16	NO CONNECT	P2C-16	GND
P2A-17	BCLOCK2	P2B-17	NO CONNECT	P2C-17	GND
P2A-18	BGATE2	P2B-18	NO CONNECT	P2C-18	GND
P2A-19	BCLOCK3	P2B-19	NO CONNECT	P2C-19	GND
P2A-20	BGATE3	P2B-20	NO CONNECT	P2C-20	GND
P2A-21	BOUT0	P2B-21	NO CONNECT	P2C-21	GND
P2A-22	BOUT1	P2B-22	GND	P2C-22	GND
P2A-23	BOUT2	P2B-23	NO CONNECT	P2C-23	GND
P2A-24	BOUT3	P2B-24	NO CONNECT	P2C-24	GND
P2A-25	NO CONNECT	P2B-25	NO CONNECT	P2C-25	GND
P2A-26	AOUT4	P2B-26	NO CONNECT	P2C-26	GND
P2A-27	AFOUT	P2B-27	NO CONNECT	P2C-27	GND
P2A-28	BOUT4	P2B-28	NO CONNECT	P2C-28	GND
P2A-29	BFOUT	P2B-29	NO CONNECT	PC2-29	GND
P2A-30	NO CONNECT	P2B-30	NO CONNECT	P2C-30	GND
P2A-31	NO CONNECT	P2B-31	GND	P2C-31	GND
P2A-32	NO CONNECT	P2B-32	VCC	P2C-32	GND

Table B-3. Input Connector JKl

Pin Number	Signal	Pin Number	Signal
1	Ground	26	BCLOCK 0
2	ACLOCK 0	27	Ground
3	Ground	28	BGATE 0
4	AGATE 0	29	Ground
5	Ground	30	BCLOCK 1
6	ACLOCK 1	31	Ground
7	Ground	32	BGATE 1
8	AGATE 1	33	Ground
9	Ground	34	BCLOCK 2
10	ACLOCK 2	35	Ground
11	Ground	36	BGATE 2
12	AGATE 2	37	Ground
13	Ground	38	BCLOCK 3
14	ACLOCK 3	39	Ground
15	Ground	40	BGATE 3
16	AGATE 3	41	Ground
17	Ground	42	BOUT 0
18	AOUT 0	43	Ground
19	Ground	44	BOUT 1
20	AOUT 1	45	Ground
21	Ground	46	BOUT 2
22	AOUT 2	47	Ground
23	Ground	48	BOUT 3
24	AOUT 3	49	Ground
25	Ground	50	Ground

Table B-4. XVME-203/293 Jumper Options

VMEbus OPTIONS	
Jumpers	Use
JA10, JA1l, JA12, JA13, JA14, JA15	Module base address select jumpers (refer to section 2.4.2)
Jl	This jumper allows the module to respond to supervisory access only (when installed) or to both supervisory and non-privileged access (when removed; Section 2.4.3)

Table B-5. Access Options

Jumper Jl	Access Mode Selection	Address Modifier Code
Installed	Supervisory Only	2DH
Removed	Supervisory or Non-Privileged	2DH or 29H

Table B-6. Interrupt Level Options

Bits (Set in Status/Control register)			
LS2	LS1	LS0	VMEbus Interrupt Level
0	0	0	None, Interrupts Disabled
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table B-7. Base Address Jumper Options

Jumpers						VME base address in VME Short I/O Address Space
JA15	JA14	JA13	JA12	JA11	JA10	
IN	IN	IN	IN	IN	IN	0000H
IN	IN	IN	IN	IN	OUT	0400H
IN	IN	IN	IN	OUT	IN	0800H
IN	IN	IN	IN	OUT	OUT	0C00H
IN	IN	IN	OUT	IN	IN	1000H
IN	IN	IN	OUT	IN	OUT	1400H
IN	IN	IN	OUT	OUT	IN	1800H
IN	IN	IN	OUT	OUT	OUT	1C00H
IN	IN	OUT	IN	IN	IN	2000H
IN	IN	OUT	IN	IN	OUT	2400H
IN	IN	OUT	IN	OUT	IN	2800H
IN	IN	OUT	IN	OUT	OUT	2C00H
IN	IN	OUT	OUT	IN	IN	3000H
IN	IN	OUT	OUT	IN	OUT	3400H
IN	IN	OUT	OUT	OUT	IN	3800H
IN	IN	OUT	OUT	OUT	OUT	3C00H
IN	OUT	IN	IN	IN	IN	4000H
IN	OUT	IN	IN	IN	OUT	4400H
IN	OUT	IN	IN	OUT	IN	4800H
IN	OUT	IN	IN	OUT	OUT	4C00H
IN	OUT	IN	OUT	IN	IN	5000H
IN	OUT	IN	OUT	IN	OUT	5400H
IN	OUT	IN	OUT	OUT	IN	5800H
IN	OUT	IN	OUT	OUT	OUT	5C00H
IN	OUT	OUT	IN	IN	IN	6000H
IN	OUT	OUT	IN	IN	OUT	6400H
IN	OUT	OUT	IN	OUT	IN	6800H
IN	OUT	OUT	IN	OUT	OUT	6C00H
IN	OUT	OUT	OUT	IN	IN	7000H
IN	OUT	OUT	OUT	IN	OUT	7400H
IN	OUT	OUT	OUT	OUT	IN	7800H
IN	OUT	OUT	OUT	OUT	OUT	7C00H
OUT	IN	IN	IN	IN	IN	8000H
OUT	IN	IN	IN	IN	OUT	8400H
OUT	IN	IN	IN	OUT	IN	8800H
OUT	IN	IN	IN	OUT	OUT	8C00H
OUT	IN	IN	OUT	IN	IN	9000H
OUT	IN	IN	OUT	IN	OUT	9400H
OUT	IN	IN	OUT	OUT	IN	9800H
OUT	IN	IN	OUT	OUT	OUT	9C00H
OUT	IN	OUT	IN	IN	IN	A000H
OUT	IN	OUT	IN	IN	OUT	A400H
OUT	IN	OUT	IN	OUT	IN	A800H
OUT	IN	OUT	IN	OUT	OUT	AC00H
OUT	IN	OUT	OUT	IN	IN	B000H
OUT	IN	OUT	OUT	IN	OUT	B400H
OUT	IN	OUT	OUT	OUT	IN	B800H
OUT	IN	OUT	OUT	OUT	OUT	BC00H
OUT	OUT	IN	IN	IN	IN	C000H
OUT	OUT	IN	IN	IN	OUT	C400H
OUT	OUT	IN	IN	OUT	IN	C800H
OUT	OUT	IN	IN	OUT	OUT	CC00H
OUT	OUT	IN	OUT	IN	IN	D000H
OUT	OUT	IN	OUT	IN	OUT	D400H
OUT	OUT	IN	OUT	OUT	IN	D800H
OUT	OUT	IN	OUT	OUT	OUT	DC00H
OUT	OUT	OUT	IN	IN	IN	E000H
OUT	OUT	OUT	OUT	IN	IN	F000H
OUT	OUT	OUT	OUT	IN	OUT	F400H
OUT	OUT	OUT	OUT	OUT	IN	F800H
OUT	OUT	OUT	OUT	OUT	OUT	FC00H

NOTE

IN = Logic "0"
OUT = Logic "1"

Table B-8. XVME-203/293 Jumper List

Jumper	Description
Jl	IN = supervisory only; OUT = supervisory or non-privileged
JAI0	Module base-address selection jumper (A10)
JAI1	Module base-address selection jumper (A11)
JA12	Module base-address selection jumper (A12)
JAI3	Module base-address selection jumper (A13)
JA14	Module base-address selection jumper (A14)
JA15	Module base-address selection jumper (A15)

Table B-9. Interrupt Level Options

Bits (Set in Control register)			VMEbus Interrupt Level
LS2	LSI	LS0	
0	0	0	None, Interrupts Disabled
0	0	1	I
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table B-10. Direction Indicator Bits

	Channel Numbers	Bit Numbers	Clockwise Bit Setting	Counterclockwise Bit Setting
STC B	0&l	7	0	1
	2&3	6	0	1
STC A	0&l	5	0	1
	2&3	4	0	1

Table B-l 1. Interrupt Controller Connections

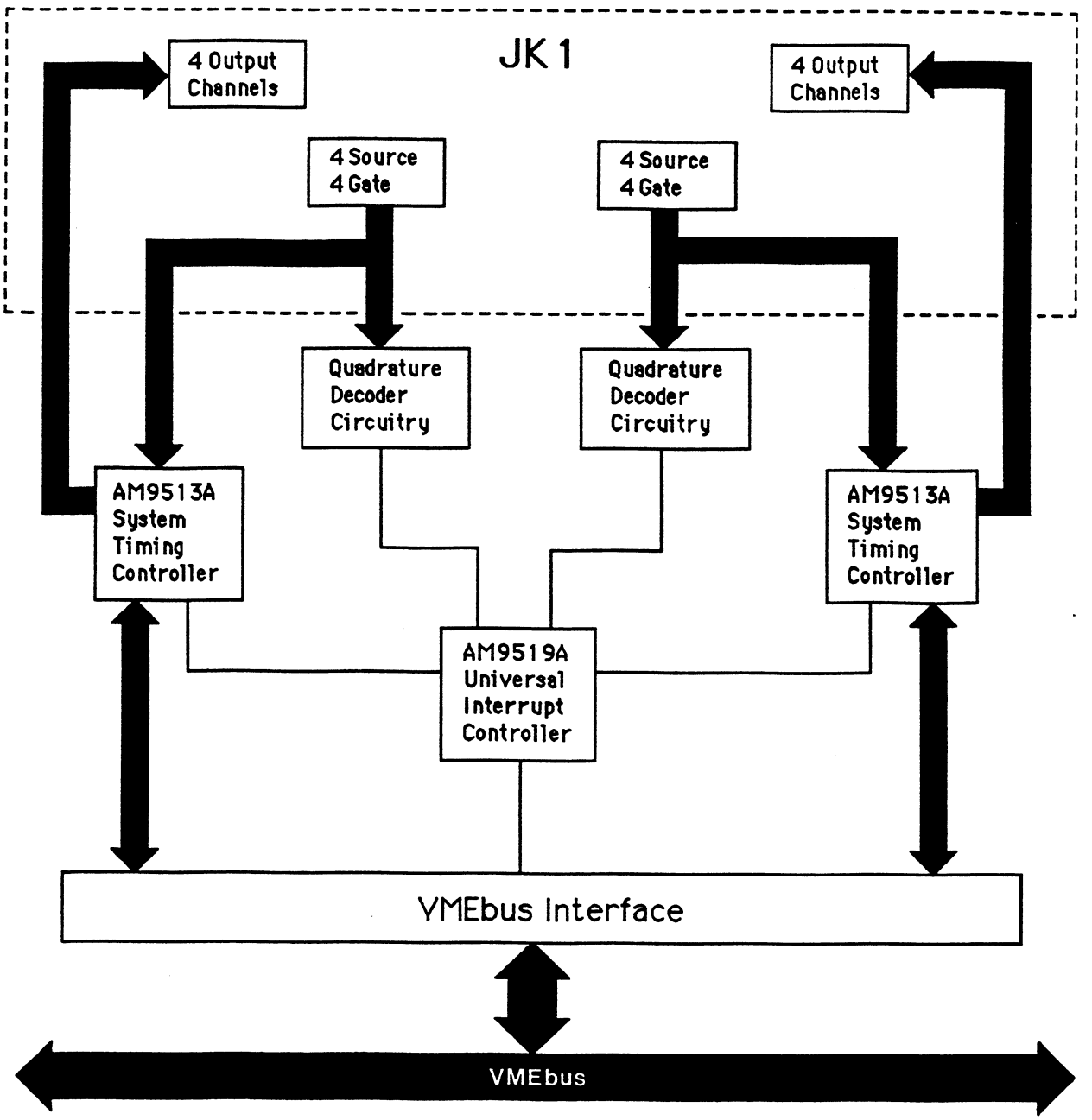
STC A outputs	STC B outputs	Interrupt Controller Inputs
AOUTO	---	IREQO
AOUTI	---	IREQI
AOUT2	---	IREQ2
AOUT3	---	IREQ3
---	BOUT0	IREQ4
---	BOUT1	IREQ5
---	BOUT2	IREQ6
---	BOUT3	IREQ7

Table B-12. Quadrature Selection

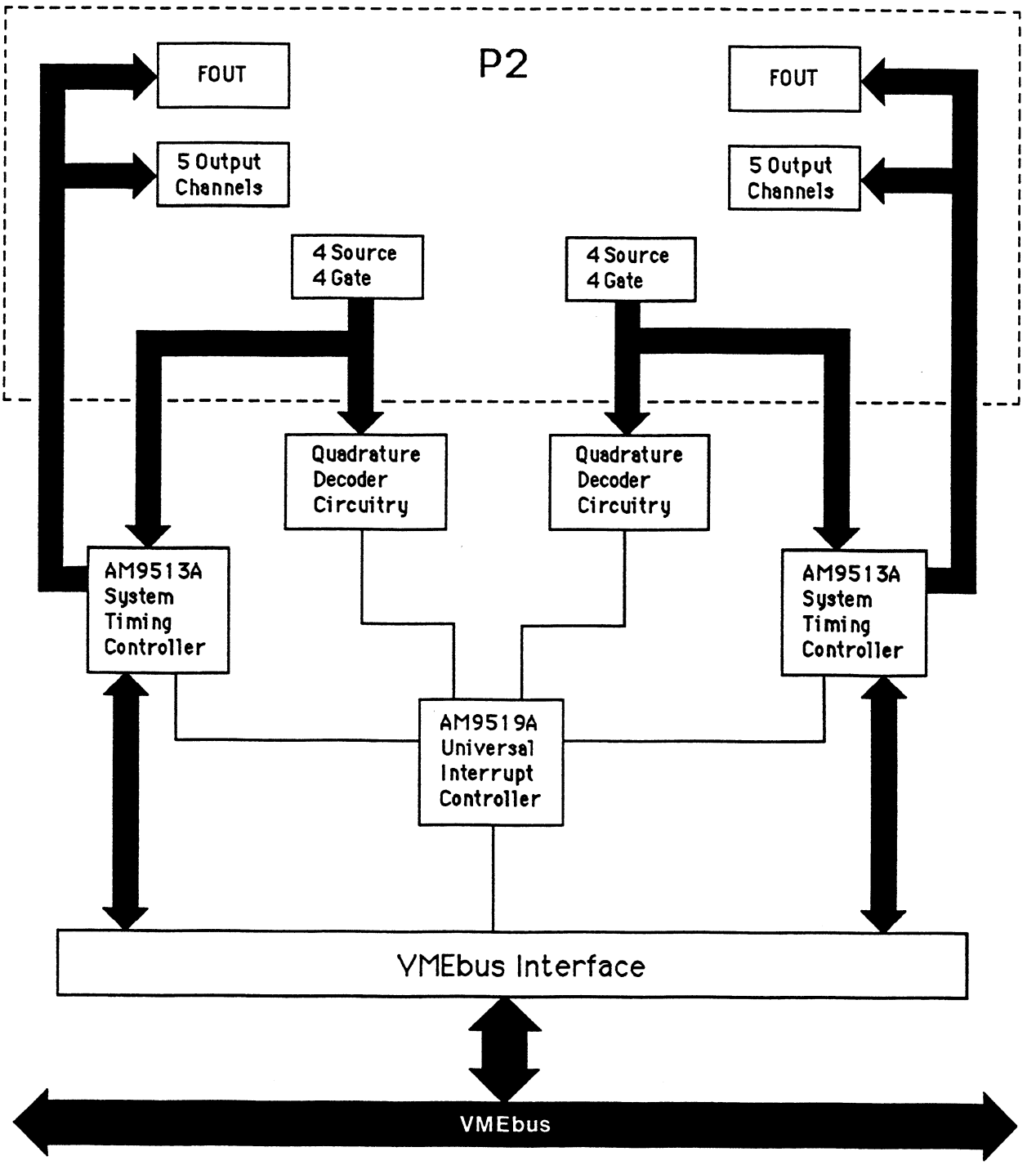
	Signal name	
STC INPUT	Quadrature selected	Quadrature not selected
SRCl	CLOCK 0	CLOCK 0
SRC2	CLOCK 1	CLOCK 1
SRC3	CW 1	CLOCK 2
SRC4	CCW 1	CLOCK 3
SRC5	CW 0	CW 0
GATE1	GATE 0	GATE 0
GATE2	GATE 1	GATE 1
GATE3	GATE 2	GATE 2
GATE4	GATE 3	GATE 3
GATE5	CCW 0	CCW 0

Appendix C

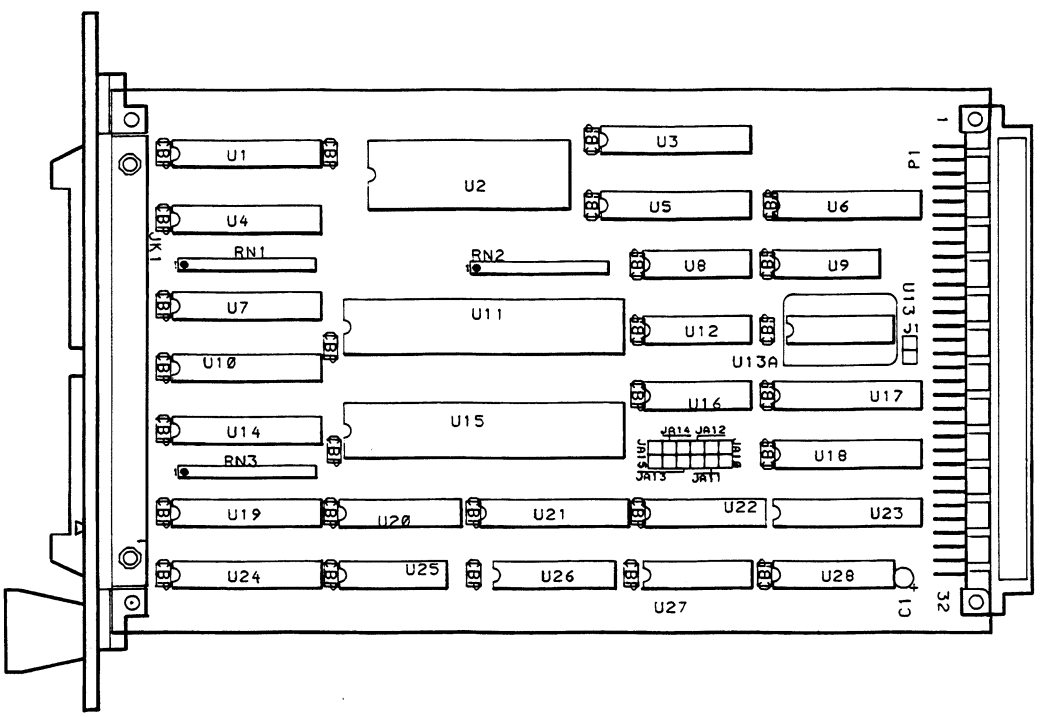
BLOCK DIAGRAM, ASSEMBLY DRAWINGS & SCHEMATICS



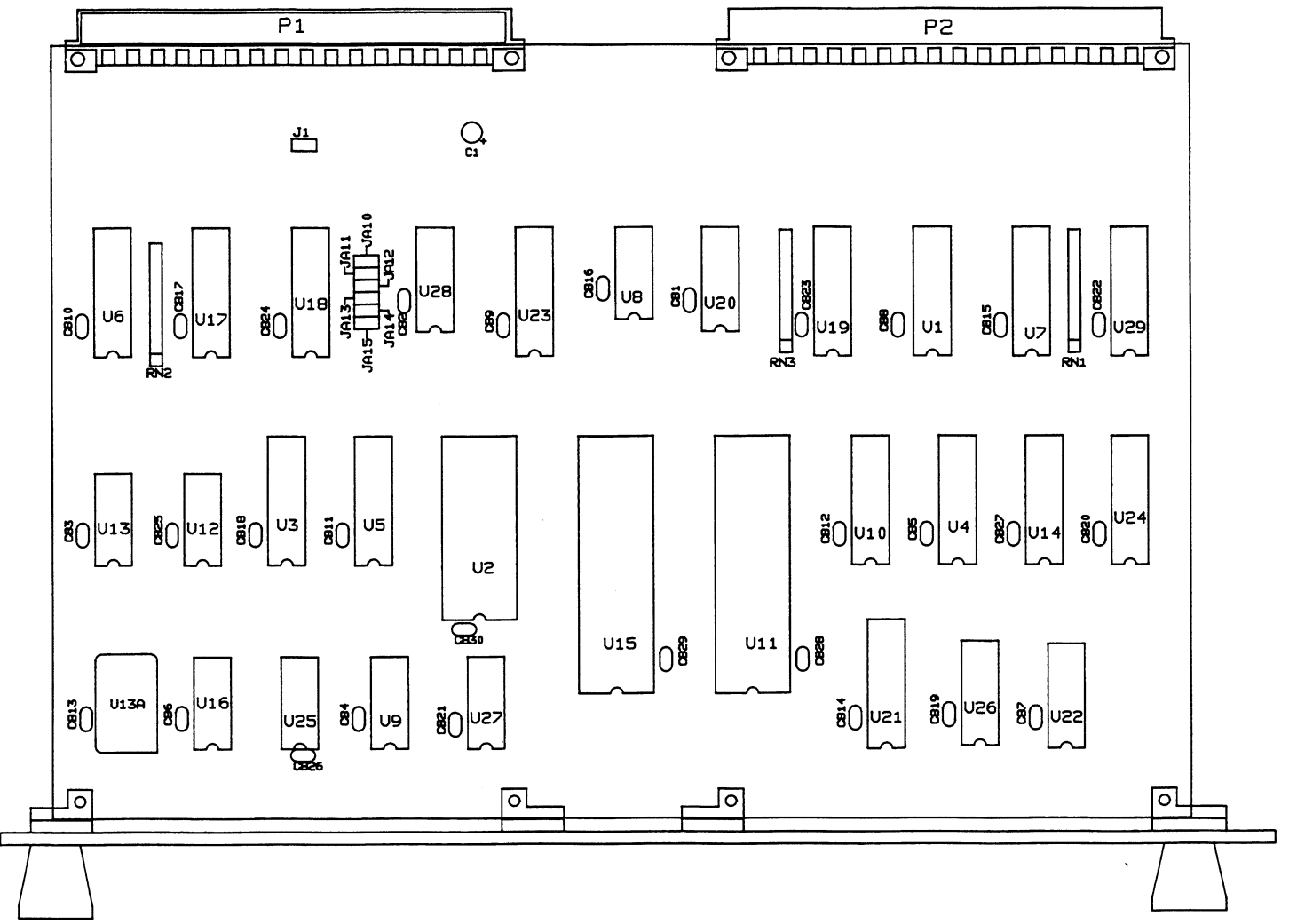
XVME-203 Block Diagram



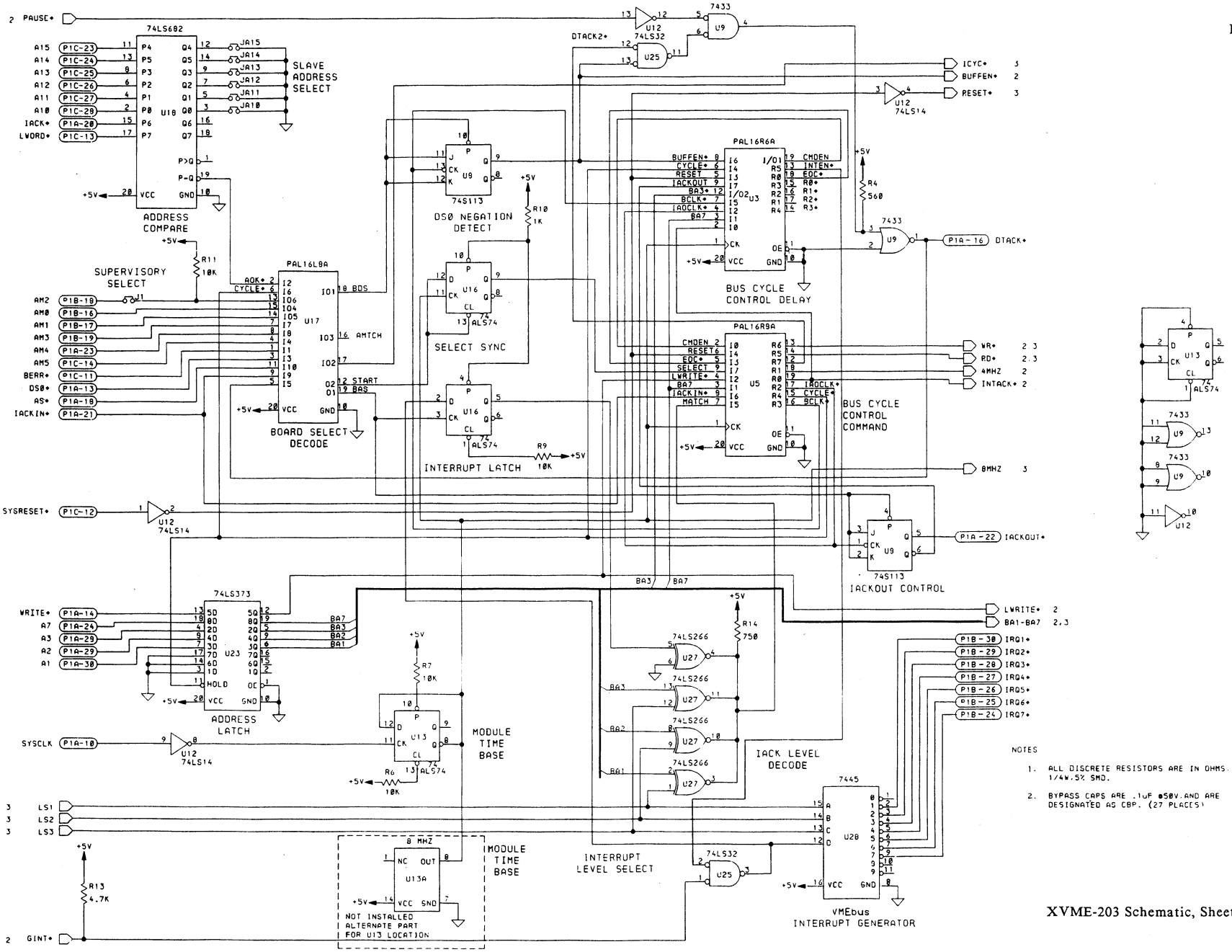
XVME-293 Block Diagram



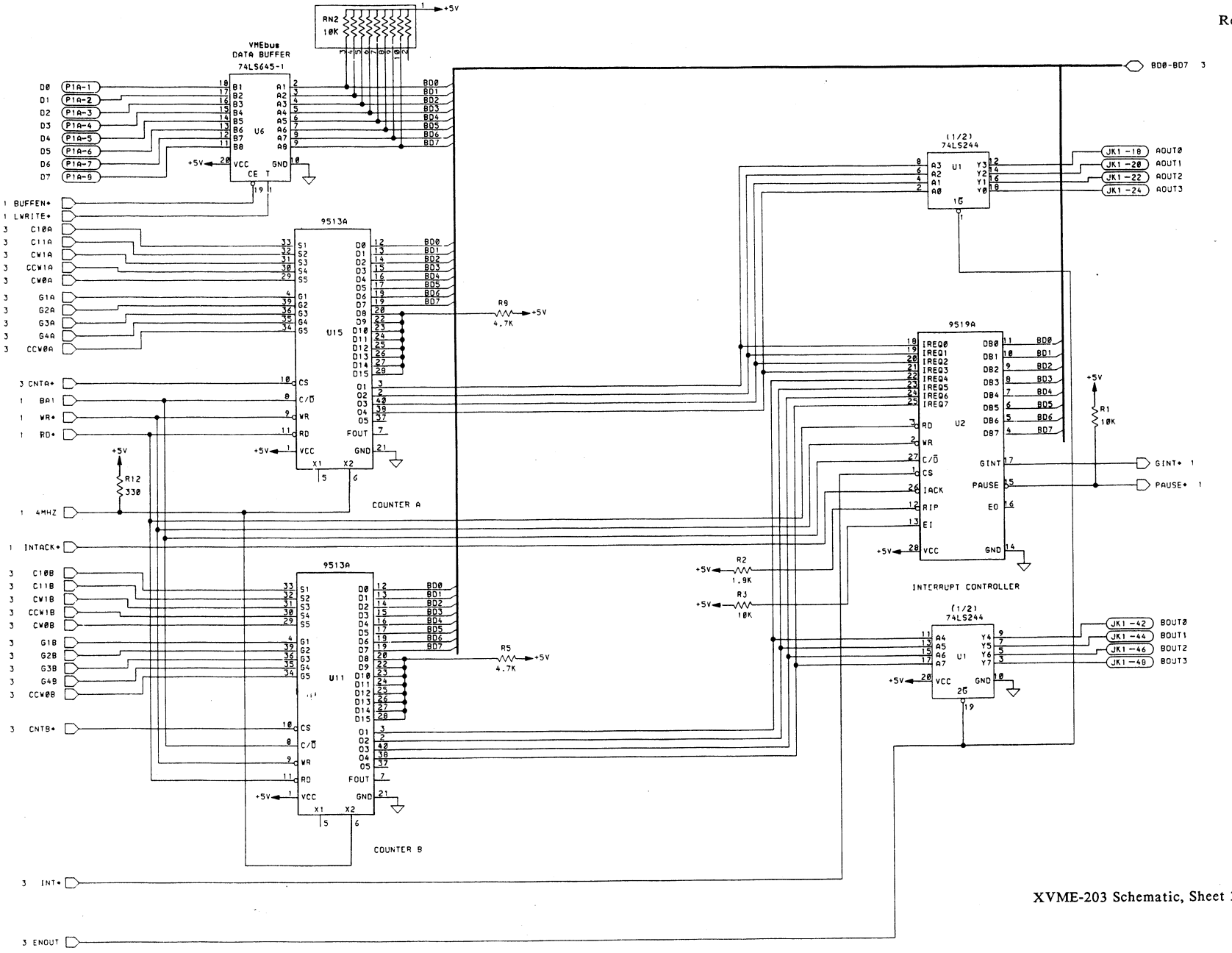
XVME-203 Assembly Drawing



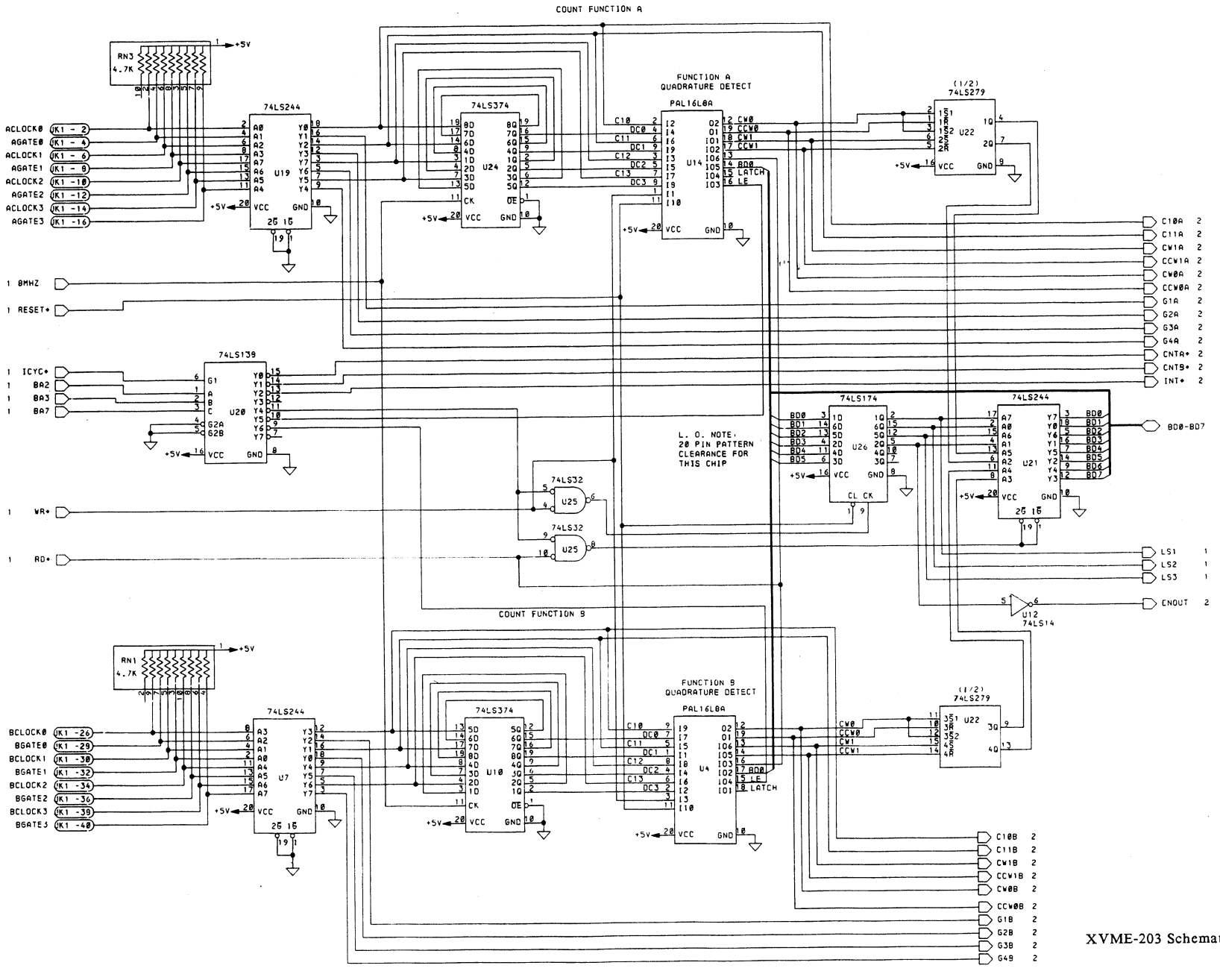
XVME-293 Assembly Drawing

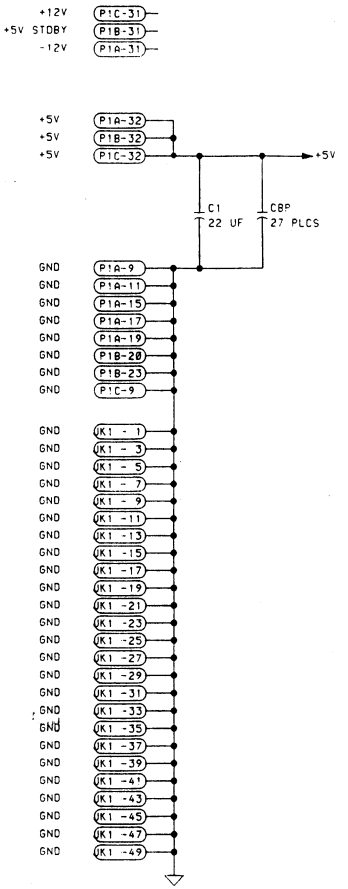


XVME-203 Schematic, Sheet 1 of 4

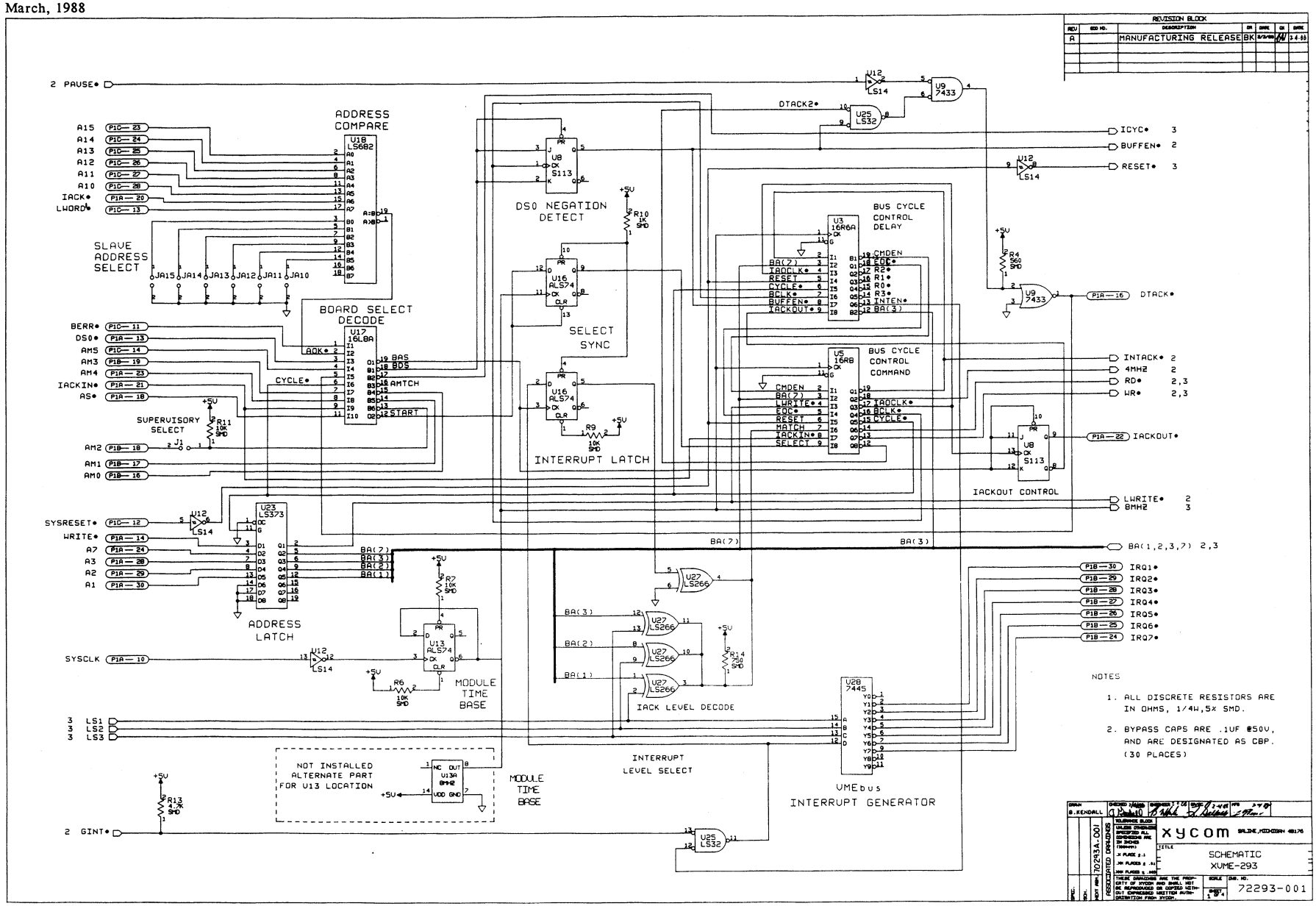


XVME-203 Schematic, Sheet 2 of 4


COUNT FUNCTION A
RN3
4.7K
+5V
74LS244
U19
ACLOCK0 (K1 - 2)
AGATE0 (K1 - 4)
ACLOCK1 (K1 - 6)
AGATE1 (K1 - 8)
ACLOCK2 (K1 -10)
AGATE2 (K1 -12)
ACLOCK3 (K1 -14)
AGATE3 (K1 -16)
74LS374
U24
FUNCTION A
QUADRATURE DETECT
PAL16L8A
U14
C10
C11
C12
C13
DC0
DC1
DC2
DC3
CW0
CCW0
CW1
CCW1
BD0
LATCH
LE
(1/2)
74LS279
U22
1 8MHZ
1 RESET*
74LS139
U20
1 ICYC*
1 BA2
1 BA3
1 BA7
74LS174
U26
74LS244
U21
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD0-BD7
L. O. NOTE:
20 PIN PATTERN
CLEARANCE FOR
THIS CHIP
CL CK
74LS32
U25
1 WR*
1 RD*
C10A 2
C11A 2
CW1A 2
CCW1A 2
CW0A 2
CCW0A 2
G1A 2
G2A 2
G3A 2
G4A 2
CNTA* 2
CNTB* 2
INT* 2
LS1 1
LS2 1
LS3 1
ENOUT 2
U12
74LS14
COUNT FUNCTION B
RN1
4.7K
74LS244
U7
BCLOCK0 (K1 -26)
BGATE0 (K1 -29)
BCLOCK1 (K1 -30)
BGATE1 (K1 -32)
BCLOCK2 (K1 -34)
BGATE2 (K1 -36)
BCLOCK3 (K1 -39)
BGATE3 (K1 -40)
74LS374
U10
FUNCTION B
QUADRATURE DETECT
PAL16L8A
U4
(1/2)
74LS279
U22
C10B 2
C11B 2
CW1B 2
CCW1B 2
CW0B 2
CCW0B 2
G1B 2
G2B 2
G3B 2
G4B 2



XVME-203 Schematic, Sheet 4 of 4


REVISION BLOCK
A MANUFACTURING RELEASE BK
2 PAUSE•
ADDRESS COMPARE
U18 LS682
A15 A14 A13 A12 A11 A10 IACK• LWORD•
SLAVE ADDRESS SELECT
JA15 JA14 JA13 JA12 JA11 JA10
BOARD SELECT DECODE
U17 16L8A
BERR• DS0• AM5 AM3 AM4 IACKIN• AS•
CYCLE•
BAS BDS AMTCH RESTART
SUPERVISORY SELECT
R11 10K SMD
AM2 AM1 AM0
DS0 NEGATION DETECT
U8 S113
R10 1K SMD
SELECT SYNC
U16 ALS74
INTERRUPT LATCH
R9 10K SMD
DTACK2•
U12 LS14
U9 7433
U25 LS32
ICYC• BUFFEN• RESET•
BUS CYCLE CONTROL DELAY
U3 16R6A
BA(2) IACLK• RESET CYCLE• BCLK• BUFFEN• IACKOUT•
CMDEN EOC• R2• R1• R0• R3• INTEN• BA(3)
R4 560 SMD
DTACK•
BUS CYCLE CONTROL COMMAND
U5 16R8
CMDEN BA(2) LWRITE• EOC• RESET MATCH IACKIN• SELECT
IACLK• BCLK• CYCLE•
INTACK• 4MH2 RD• WR•
IACKOUT CONTROL
IACKOUT•
LWRITE• 8MH2
SYSRESET• WRITE• A7 A3 A2 A1
U23 LS373
ADDRESS LATCH
BA(7) BA(3) BA(2) BA(1)
BA(1,2,3,7) 2,3
SYSCLK
U13 ALS74
R7 10K SMD
R6 10K SMD
MODULE TIME BASE
U27 LS266
IACK LEVEL DECODE
IRQ1• IRQ2• IRQ3• IRQ4• IRQ5• IRQ6• IRQ7•
U28 7445
VMEbus INTERRUPT GENERATOR
INTERRUPT LEVEL SELECT
3 LS1 3 LS2 3 LS3
NOT INSTALLED ALTERNATE PART FOR U13 LOCATION
U13A 8MHZ
R13 4.7K SMD
2 GINT•
U25 LS32
NOTES
1. ALL DISCRETE RESISTORS ARE IN OHMS, 1/4W,5% SMD.
2. BYPASS CAPS ARE .1UF @50V, AND ARE DESIGNATED AS CBP. (30 PLACES)
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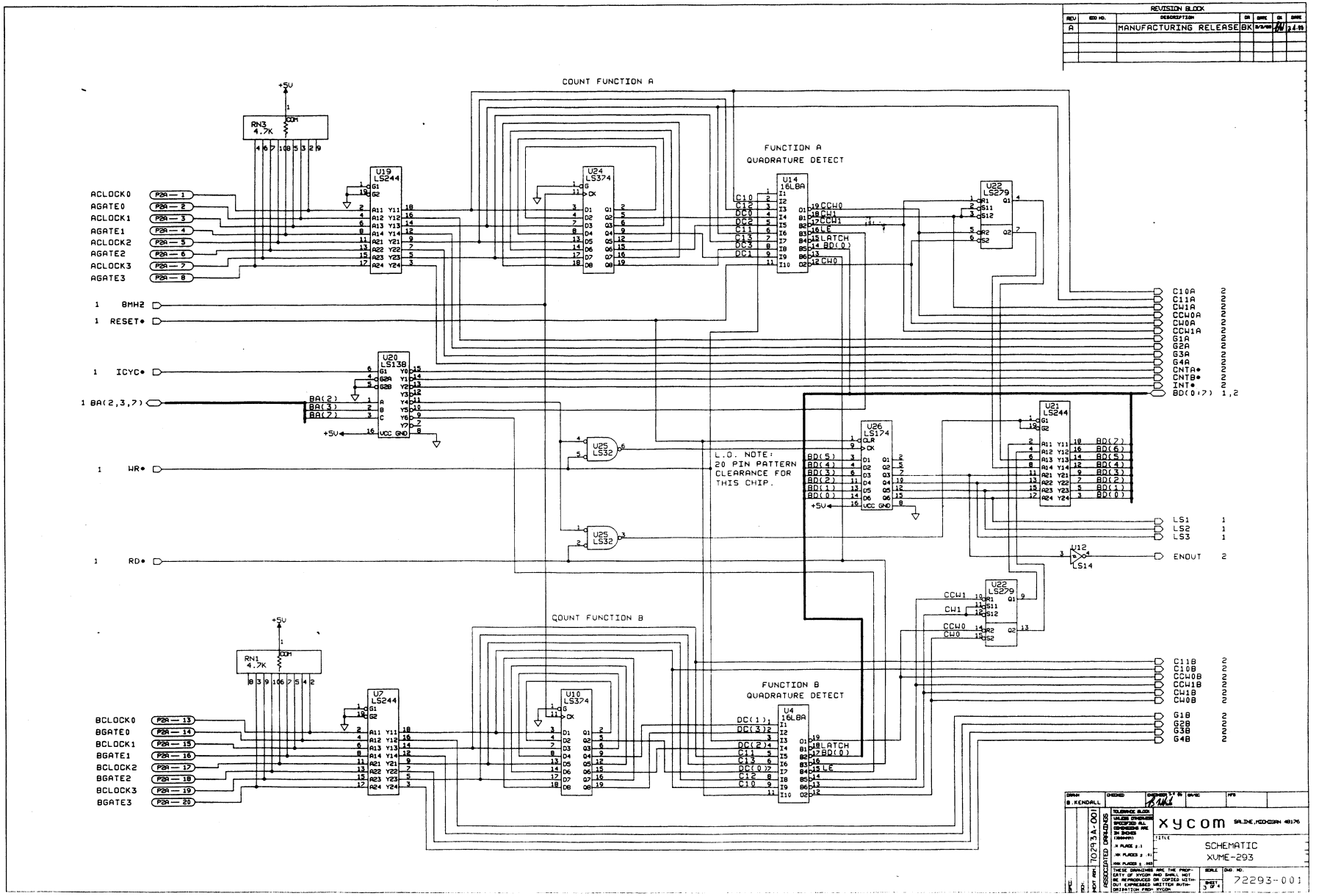
ASSOCIATED DRAWINGS 70293A-001
xycom SCHEMATIC XVME-293
72293-001


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
BK
2-4-88
COUNT FUNCTION A
FUNCTION A
QUADRATURE DETECT
+5V
RN3
4.7K
U19
LS244
U24
LS374
U14
16L8A
U22
LS279
ACLOCK0
AGATE0
ACLOCK1
AGATE1
ACLOCK2
AGATE2
ACLOCK3
AGATE3
8MHZ
RESET*
ICYC*
BA(2,3,7)
WR*
RD*
U20
LS138
BA(2)
BA(3)
BA(7)
U25
LS32
U26
LS174
L.O. NOTE:
20 PIN PATTERN
CLEARANCE FOR
THIS CHIP.
U21
LS244
U12
LS14
C10A
C11A
CW1A
CCW0A
CW0A
CCW1A
G1A
G2A
G3A
G4A
CNTA*
CNTB*
INT*
BD(0:7)
LS1
LS2
LS3
ENOUT
COUNT FUNCTION B
FUNCTION B
QUADRATURE DETECT
RN1
4.7K
U7
LS244
U10
LS374
U4
16L8A
U22
LS279
BCLOCK0
BGATE0
BCLOCK1
BGATE1
BCLOCK2
BGATE2
BCLOCK3
BGATE3
C11B
C10B
CCW0B
CCW1B
CW1B
CW0B
G1B
G2B
G3B
G4B
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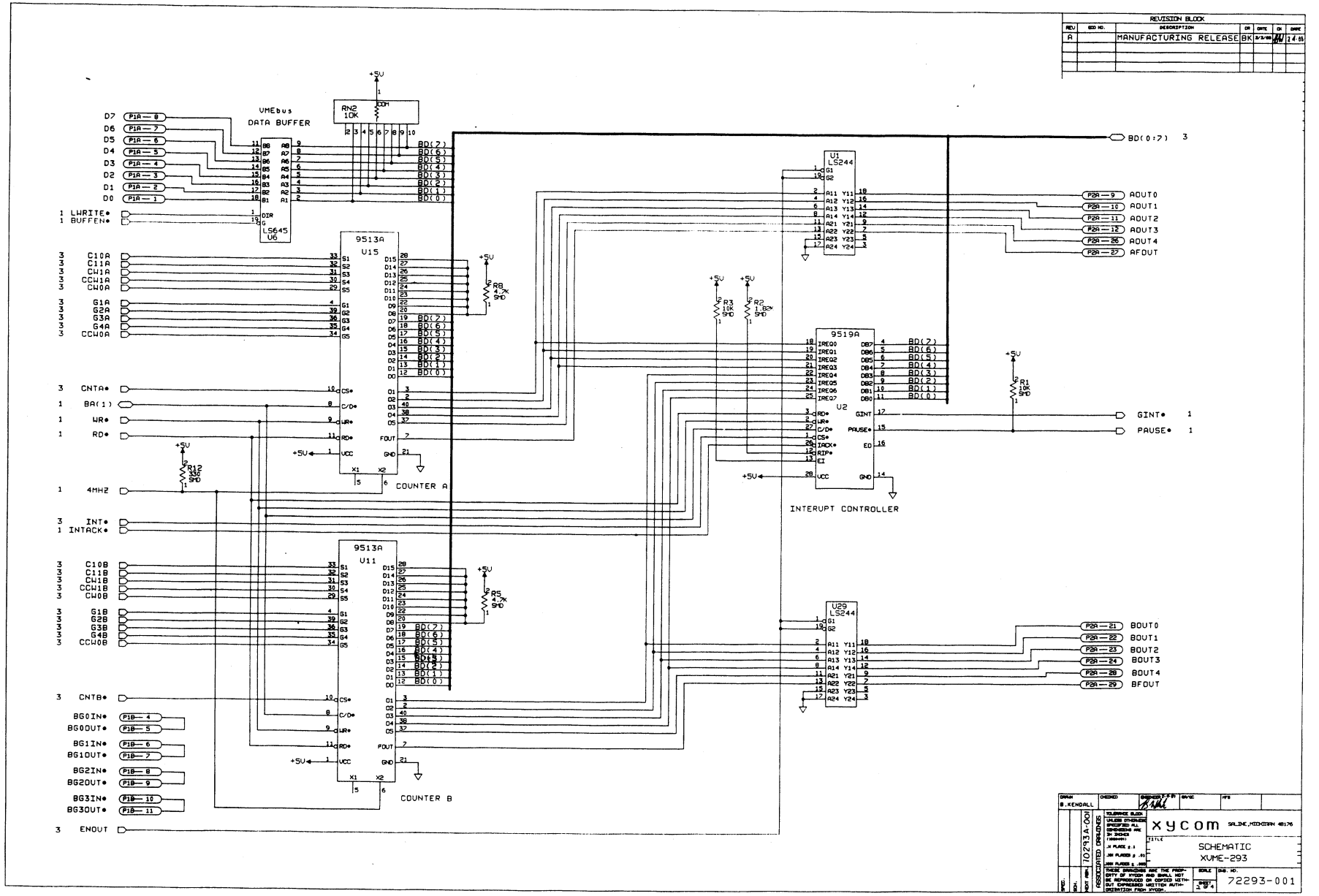
SCHEMATIC
XVME-293
72293-001
72293A-001


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
BK
VMEbus
DATA BUFFER
U6
LS645
RN2
10K
U1
LS244
U29
LS244
U15
9513A
COUNTER A
U11
9513A
COUNTER B
U2
9519A
INTERUPT CONTROLLER
BD(0:7)
AOUT0
AOUT1
AOUT2
AOUT3
AOUT4
AFOUT
BOUT0
BOUT1
BOUT2
BOUT3
BOUT4
BFOUT
GINT*
PAUSE*
4MHZ
LWRITE*
BUFFEN*
INT*
INTACK*
ENOUT
BG0IN*
BG0OUT*
BG1IN*
BG1OUT*
BG2IN*
BG2OUT*
BG3IN*
BG3OUT*
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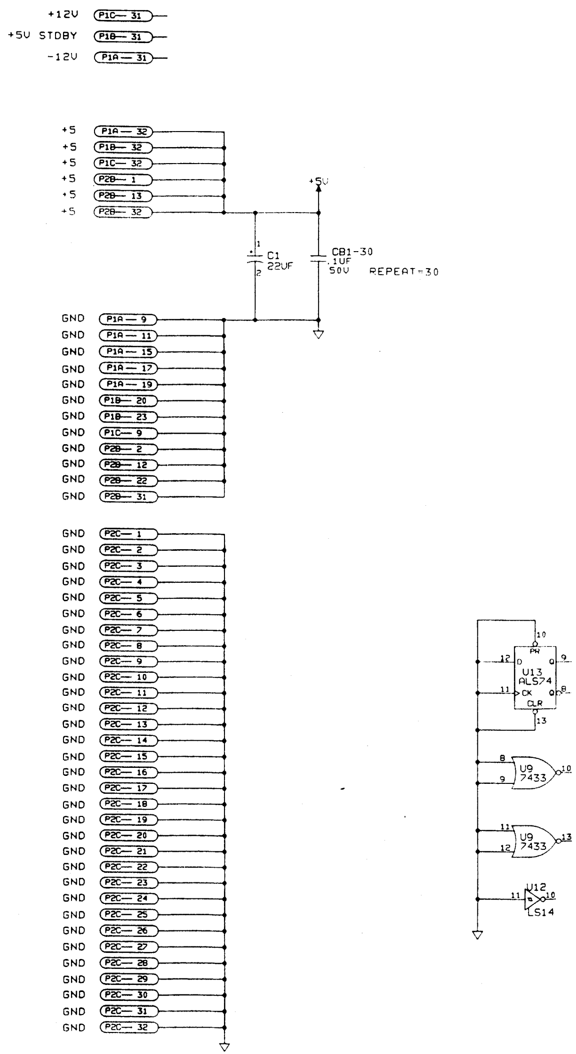
SCHEMATIC
XVME-293
72293-001

REVISION BLOCK

REV	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
A		MANUFACTURING RELEASE	BK			



REFERENCE DESIGNATOR	DEVICE	VCC	GND
U1,7,19,21	74LS244	20	10
U3	16R6A	20	10
U4,14,17	16L8A	20	10
U5	16R8	20	10
U6	74LS645	20	10
U8	74S113	14	7
U9	7433	14	7
U10,24	74LS374	20	10
U12	74LS14	14	7
U13,16	74ALS74	14	7
U18	74LS682	20	10
U20	74LS138	16	8
U22	74LS279	16	8
U23	74LS373	20	10
U25	74LS32	14	7
U26	74LS174	16	8
U27	74LS266	14	7
U28	7445	16	8
U29	74LS244	20	10

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