ACD Retriggering Study

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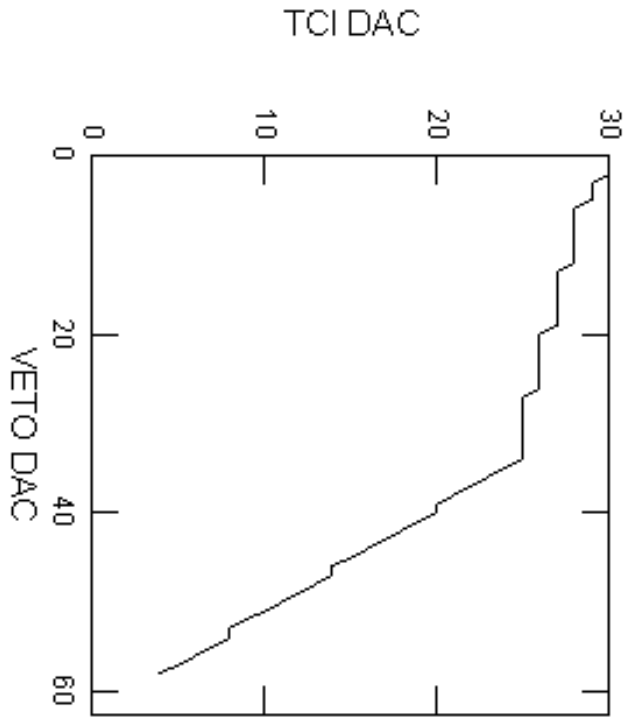
Introduction

- There was evidence of veto retriggering with charge injection at high DAC settings.
- Mike asked me to write a script that does the following:
  - Scan through the entire CI DAC range
  - At each setting
    1. Issue a calstrobe
    2. Read out the tile and CNO LRS counters to record how many times the veto fired
    3. Issue a TACK
    4. Read out the tile and CNO LRS counters.
  - There are long pauses (1 ms) between the individual steps to ensure the counter readings record what actually happened at exactly this step.
- The test was run on the mini-LAT which has one GARC attached.

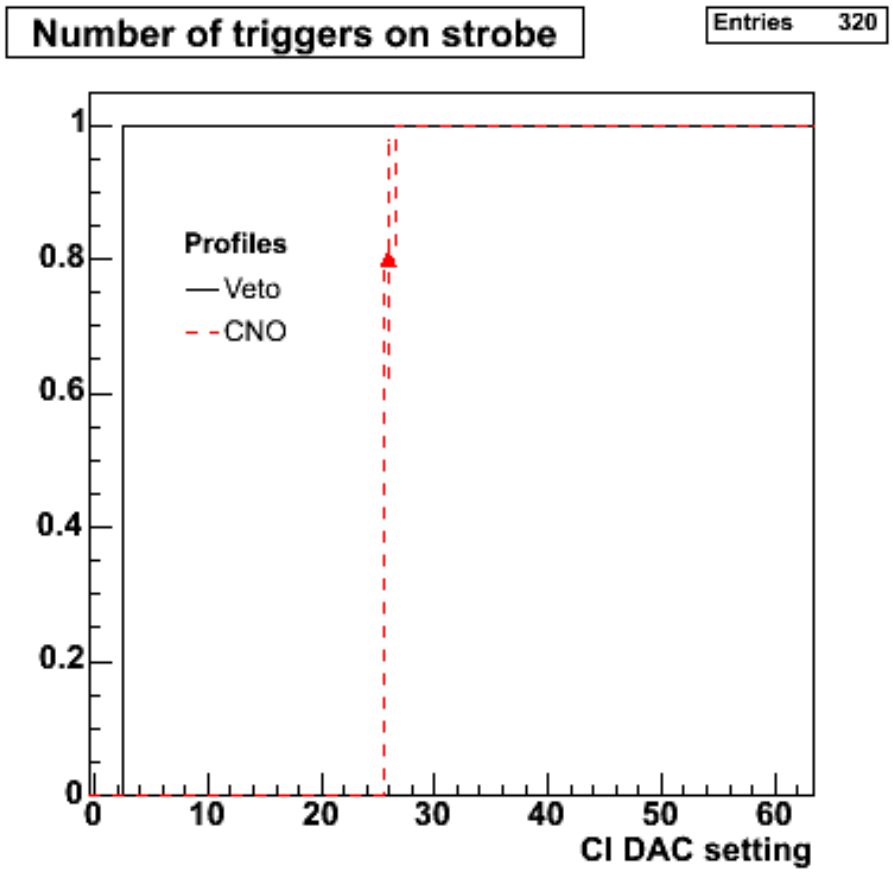
ACD Charge Injection

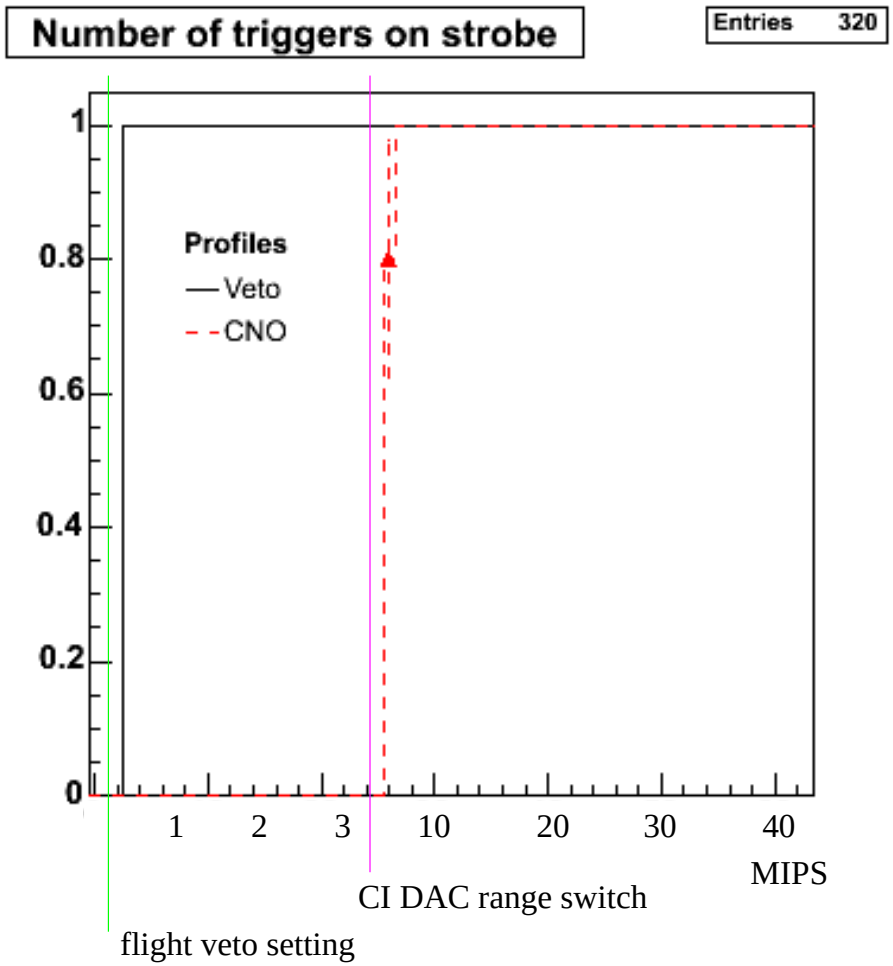
- Charge injection is done through a 6 bit DAC (0 - 63).
- There are two subranges: 0 - 23 and 24 - 63.
- The upper range gain is about 6 times higher.
- The two ranges meet at 24.



Scan results

LRS counters after calstrobe:



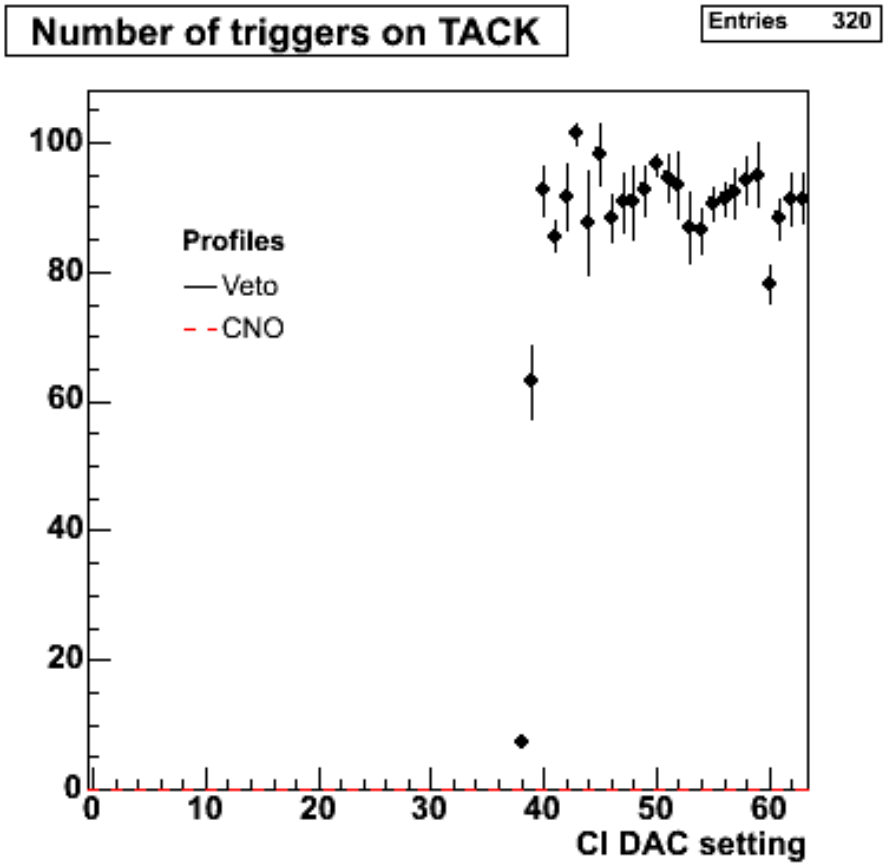


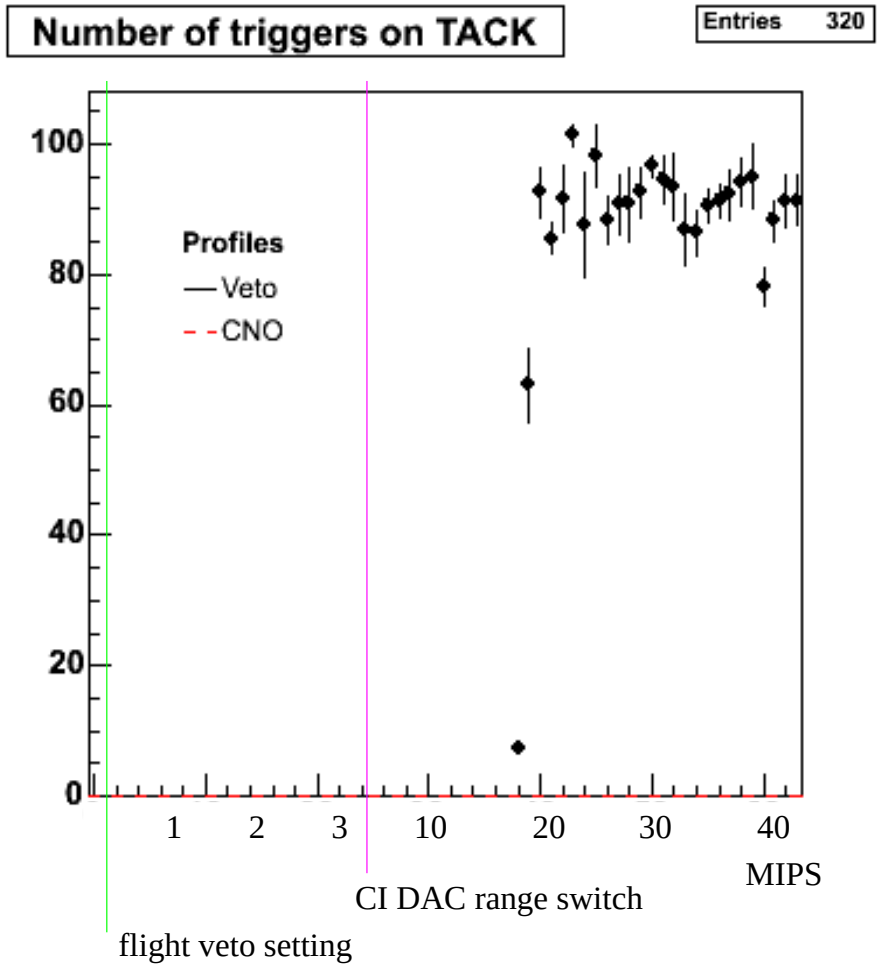
Left plot: vs. CI DAC

Right plot: vs. MIPS (approx.)

Scan results

LRS counters after TACK:



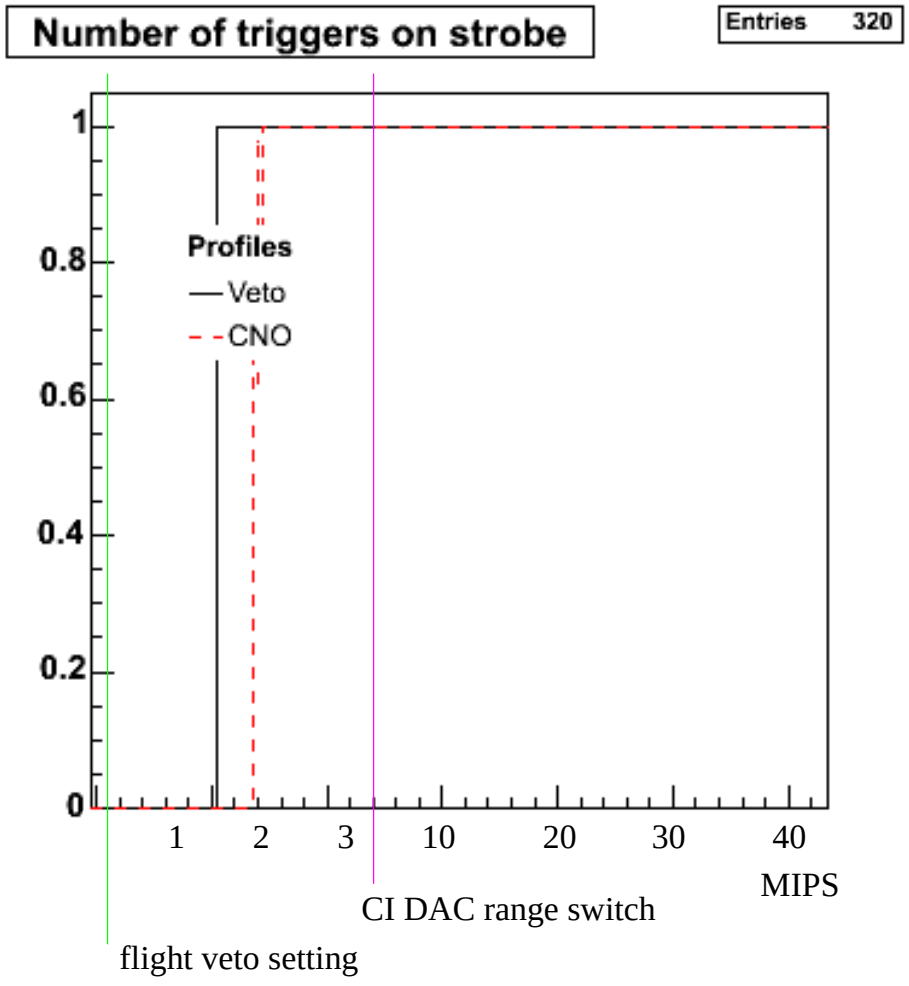


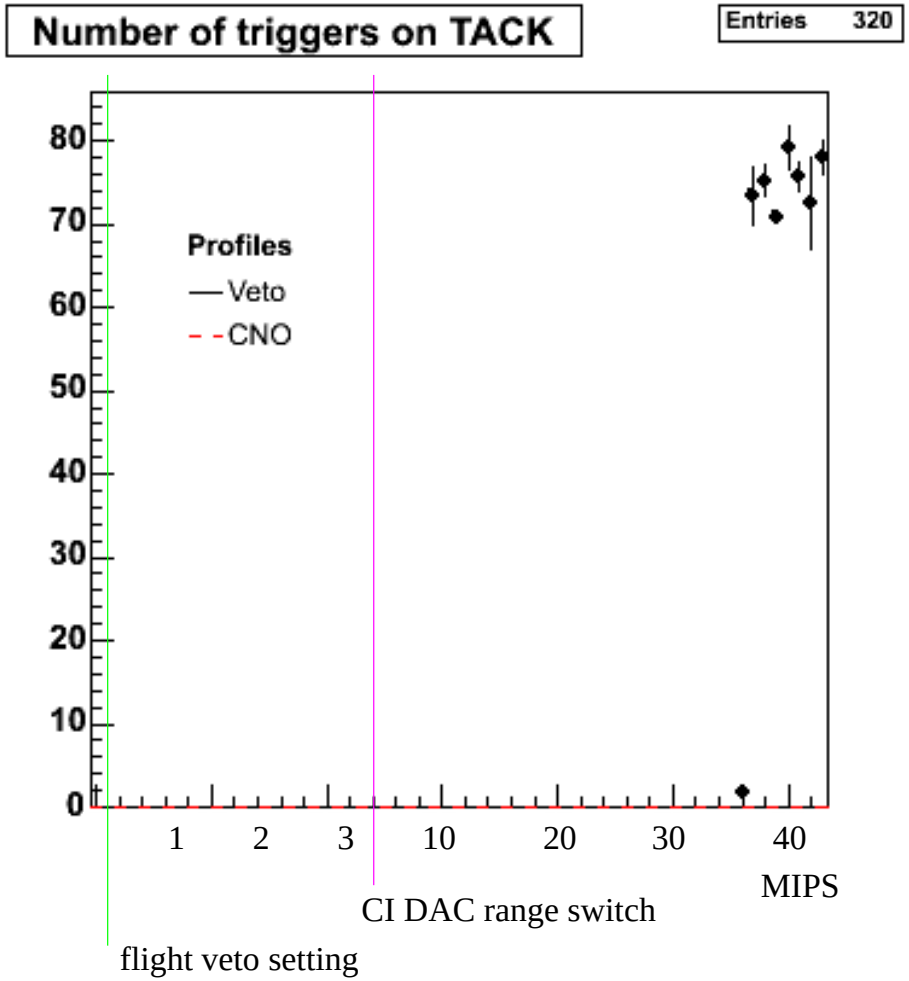
Left plot: vs. CI DAC

Right plot: vs. MIPS (approx.)

Scan results

At higher veto threshold:





Left plot: After calstrobe

Right plot: After TACK

Summary

Summary of findings:

- Retriggering occurs on readout.
- There is no retriggering during the original pulse after a calstrobe.
- The retriggering threshold changes with the veto DAC setting.
- There is no channel cross-talk.
- There is no retriggering when doing TACK without calstrobe.

Mike and Gunther analyzed the situation and concluded that the retriggering is caused by the reset of the charge injection which happens on the readout that follows a calstrobe.

$\Longrightarrow$ No problem for data taking.