3DX: A micro-machined silicon crystallographic X-ray detector

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ABSTRACT

We are developing pixel detectors for macromolecular crystallography, in which diffracted X-rays are directly absorbed by high-resistivity, crystalline silicon that has been micro-machined by inductively-coupled plasma etching. Arrays of 64 x 64 holes at 150µm pitch are first formed by etching through the entire silicon bulk, then backfilled with polysilicon that is doped to create conducting p and n type columnar electrodes. When reverse biased, these electrodes generate electric fields that define the individual pixels. By forming conducting polysilicon on the sides of the sensors, which are cut-out of the silicon wafer by plasma etching, the entire surface of the detector may be made active. CMOS readout integrated circuits are conductively bump bonded behind each 3D detector, providing a direct connection to every pixel. A large array will be assembled with no insensitive bands along the edges by overlapping these sensors, each of area 0.96cm². This detector will measure X-ray signal intensities of up to 10⁵ events/pixel/sec without any pile-up loss, by using an integration method that retains the benefits of discrete photon counting. The detector sensitivity will be highly uniform, it will not exhibit any dark signal or spurious noise, and no geometric distortion will occur within each sensor.

Keywords: Silicon, plasma etching, pixel detector, X-ray, crystallography, diffraction

1. INTRODUCTION

For the study of large unit-cell crystals that diffract over several hundred orders, detectors with input apertures >20 x 20cm² square and with spatial resolution <200µm are required. The present detectors of choice at synchrotron sources comprise a phosphor screen coupled to a CCD camera readout. The optical image formed by X-rays striking the phosphor screen is relayed by an array of coherent fiber-optic bundles to multiple CCDs [1], or by a fast lens (N.A. 0.16) imaging onto a single, large format CCD [2]. Although some incremental improvements in speed of readout and noise can be anticipated for these systems, they can never reply to the ideal requirements of crystallography, in particular

- single X-ray photon sensitivity together with a signal dynamic range >10⁵. A few intense spots in a diffraction pattern suffice to spoil the usable dynamic range of a CCD which in any case never exceeds ~16 bits, defined by its electronic read noise and pixel charge handling capacity.
- continuous accumulation of data. In protein crystallography, sample crystals decay rapidly in the intense X-ray beams of 3rd generation synchrotrons, so data must be accumulated rapidly and efficiently. CCD systems operate in repeated ‘integrate then readout’ cycles, synchronized to the opening of an X-ray shutter that is needed to avoid image smear upon CCD frame transfer. This cyclic operation also requires that a mechanical spindle, which turns the diffracting crystal, be ‘rewound’ after each CCD frame integration. The entire readout process requires a second or more, whereas for strongly diffracting crystals the CCD may reach its signal saturation limit in 0.1sec.
- a narrow point spread function, devoid of the long tails associated with the spatial response of the granular phosphor screen. Precise determination of the signal intensity in sharp diffraction peaks that are often closely grouped is severely limited by this phenomenon.

A promising replacement for the phosphor screen-CCD combination is the pixel detector array. Each element of this array is a sandwich of:

- a layer of semiconductor material, for the absorption and direct conversion of the incident X-rays to electrical charge. This layer is electrically segmented into pixels of size 100 to 200µm square. Apart from the effect of lateral
charge diffusion from X-rays that convert within a few microns of the pixel borders, the response of the detector is confined to the single pixel in which the X-ray is absorbed.

An integrated circuit for readout that is bump bonded to connect individually with all the pixels. This circuit usually includes a preamplifier, discriminator and counter under every pixel, and operates in a ‘photon counting’ mode.

Hundreds of these sandwich elements must be assembled, as close packed or overlapping tiles, to create a final detector array comprising several million pixels. Several groups have now tested such detectors, either as single elements or as prototype, small assemblies [3,4,5,6,7]. The manufacture of a full-scale detector array presents formidable problems of mechanical alignment, stability, connectivity, and heat dissipation [8].

We present a scheme for such a pixel detector that differs from those reported to date in two essential aspects:

1. it uses high resistivity (>3kΩ cm) silicon as the X-ray absorbing material, in which columnar electrodes, penetrating the entire silicon bulk, are spaced at regular intervals to define the internal charge collecting fields. Compared to conventional, planar processed silicon, the strong drift fields of this ‘3D’ architecture that point away from the pixel boundaries, rather than along them for much of the silicon thickness, minimize the deleterious effects of charge sharing between adjacent pixels. As mentioned earlier, 3D processing also permits each silicon detector element to be made sensitive to within a few microns of its physical edges.

2. it uses a readout architecture with sub-millisecond, cyclical sampling of the charge accumulated in every pixel element. This is followed by sparsified readout of only those pixels having accumulated significant signal charge, permitting the subsequent data acquisition electronics to digitally integrate signals over longer time periods. The short integration cycles result in near zero X-ray count expectancy for each pixel, and this permits correction of the residual effect of charge sharing between pixels.

2. 3D MICRO-MACHINED DETECTORS

2.1 Principal of operation

With micro-machining methods, “3D” electrode arrays can be made which solve many problems associated with conventional solid-state sensors used as particle or X-ray detectors [9]. Instead of creating planar electrodes on both surfaces, we have fabricated an array of closely spaced (100 - 200µm pitch) electrodes, passing completely through the sensor (figure 1a). The electrodes consist of alternate p-type and n-type polysilicon, back-filled into holes of nominal diameter 20µm that have been micro machined through the high resistivity p type silicon wafer. When reverse-biased, these electrodes generate electric fields that are parallel to the silicon wafer surface. With this architecture, the wafer can be made arbitrarily thick without increasing the voltage needed to deplete the p bulk. For a silicon resistivity 10kΩ cm, the detector is fully depleted with <10V of bias [10].

The 3D architecture permits fast readout speed even at low voltage operation because the electrodes are close together: at a 10V bias, charge created by ionizing radiation drifts and is collected by the electrodes in ~10ns or less. As the front and backside voltages are identical at corresponding points, we do not confront the problem of preventing large, top-to-bottom surface current leakage at the cut edges of the silicon. We propose that a conducting polycrystalline silicon electrode may be processed on the very edges of the detector so that the entire surface becomes an active sensor (figure 1b). This should be compared with conventional planar sensors, which must have an insensitive region at their edges, which is occupied by a multi guard ring structure, needed to define and control the peripheral electric fields. It is impossible to tile such conventional planar detectors into larger arrays without creating a mesh pattern of insensitive regions, amounting to 5% or more of the surface area for silicon sensors of thickness 500µm [3, 11].
2.2 Fabrication

Holes were made in supported silicon wafers using inductively coupled plasma etching with an instrument made by Surface Technology Systems [12]. This uses the ‘Bosch’ process [13], in which fluorine ions from dissociated SF₆ vertically bombard regions of the silicon wafer not protected by a patterned photoresist. The exposed silicon reacts to form SiF₄ gas. To prevent fluorine that does not react at the bottom of the hole from laterally etching sides of the hole, the SF₆ is pumped out after a few seconds and replaced by C₄F₈ gas which decomposes in the plasma, creating CF₂ radicals that combine to deposit a polymerized fluorocarbon coating on all surfaces, including the hole walls. The C₄F₈ is rapidly replaced once again with SF₆, and the etching is re-initiated. The fluorocarbon is rapidly etched away at the bottom of the hole, but the sidewall resists the new etching phase. This procedure cycles automatically. With careful adjustment of the process parameters, a highly directional vertical etching of the silicon at a rate of 1 - 5µm/minute is obtained.

Figure 2: Test ‘C’ hole structures in silicon, fabricated at the Stanford Nanofabrication Facility using the Bosch process plasma etching.

The holes are filled with polysilicon, which is then doped to make n (or p) type electrodes. Polysilicon is created by low-pressure chemical vapor deposition, which involves the capture and surface decomposition of silane. This creates a conformal coating because the silane mean free path is large compared to the hole dimensions and its reactivity is low, so the probability of attaching on any one collision is very low. After several microns of polysilicon have been deposited, a dopant gas is introduced to deposit boron from B₂O₃ (for the n type electrodes), followed by an annealing in which the dopant is diffused into the surrounding single crystal silicon. The dopant makes the polysilicon and the crystalline silicon bulk immediately surrounding it into a highly conductive electrode, with the diode junction inside the single crystal silicon, which is essential to keeping leakage current low when the device is biased. After protecting the n electrodes at the surface with an oxide deposition, the hole filling process is repeated to create the p type electrodes, using phosphorus deposition from P₂O₅. Finally the p and n electrodes are electrically connected as needed by a patterned aluminum deposit. The process steps are summarized in Figure 3.

Figure 3: Simplified process steps for fabrication of 3D detectors.

Figure 4 shows a fabricated 23µm diameter polysilicon filled hole in a 300µm thick wafer. This wafer cracked during the processing, and reveals the polycrystalline texture of the material (the use of a support wafer, oxide bonded to the sensor wafer at the start of processing, now prevents such cracking). Note that the column of polysilicon is not significantly tapered in the upper part where the plane of fracture has fortuitously included the axis of the hole. We have now made dozens of such detectors, creating thousands of electrodes in well-controlled, repeatable process steps: essentially all the devices that have been fabricated to date have electrodes that are physically intact and electrically functional.

In addition to making possible efficient collection from thick detectors, the 3D process can be used to fabricate detectors that are sensitive all the way out to the physical edges of the wafer. Up to now, we have cut individual detectors from the wafer using conventional saw...
cutting. To produce electrically active edges, the individual detectors will be segmented by plasma-etching linear trenches through the silicon: these ‘cuts’ are smooth and do not introduce the micro-cracking at the crystal edges inevitably found with saw cuts. Like the column holes, these trenches will have been back-filled with conducting polysilicon, and the dopant diffused a micron or so into the crystalline silicon, so that after being separated from the supporting wafer by a final etch step, the detector edge can be electrically contacted to act as a field defining, boundary electrode. This ‘active edge’ capability is central to our project, as we plan to cover a large area with individual detectors of dimension only 0.96 cm square. This small sensor size has been chosen to ensure a high yield, and as it permits a highly parallel system to be assembled with a correspondingly fast readout.

2.3 Test results
The 3D detectors are fully depleted with a bias voltage as low as ~10V for a 200µm pitch column array. This was verified by measurements that showed saturated charge collection at the p column electrodes when the detectors were stimulated by a 915nm pulsed light-emitting diode. Room temperature leakage currents measured on several of these fully depleted detectors were in the range 0.3 to 1.3 nA/mm³ [10]. The capacitance of a p electrode was measured indirectly, by connecting it to a low capacity probe (0.1pF//1MO), pulsing the light emitting diode, and measuring the characteristic RC decay time. After correction for the probe contribution, a value of 0.19pF was obtained for a 121µm thick detector with 200µm p column pitch [14]. Note that unlike conventional planar detectors, this capacitance will scale in proportion to the detector thickness.

True active edges on 3D detectors have not yet been fabricated, but we have simulated these by fabricating detectors with 11µm wide trench electrodes placed midway between rows of column electrodes as shown in figure 5a. Figure 5b shows the signal amplitude from the column electrodes facing the trench electrodes as the bias voltage was increased (an infra-red, light emitting diode was used to generate signal charge inside the detector). A clear plateau is seen above 15V, indicating full depletion and charge collection. Spatial scans of these detectors were also made, by focusing an 820nm infrared light emitting diode with a microscope objective. The current signal (measured from an isolated, single p type column electrode) vs. position plot had a full width at half max of 287µm, consistent with the trench-to-trench center spacing of 320µm and the infra-red beam width of ~30µm diameter [15]. These results are encouraging but not conclusive, as they were complicated by the surface reflectivity of the aluminum traces. Scanning measurements are now being made with a 12keV X-ray micro beam <10µm diameter at a synchrotron source.

Spectra of X-ray and gamma sources have been made using sensors in which 16 groups of 14 column electrodes each were connected with aluminum traces. The detectors were glue mounted on a printed circuit board, and wire bonded to a 16-channel integrated circuit charge preamplifier-shaper. Figures 6a,b,c show the pulse height spectra from a detector that was flood-illuminated by ⁵⁵Fe and ²⁴¹Am radioactive sources [16]. They illustrate the excellent energy resolution of the detector, where the peak widths are dominated by the preamplifier electronic noise. The photopeaks are symmetrical and as shown in figure 6b, well fitted by a Gaussian profile. The ⁵⁵Fe measurement was recently repeated on sensors that had been stored with no particular precautions for more than a year, and gave qualitatively identical spectra to that shown in figure 6c. The remarkably little, low energy tailing in the ⁵⁵Fe spectrum is a sensitive test of the absence of significant surface charge trapping or recombination. Any signal charge sharing to adjacent rows of columns would also have produced a low energy tail in the spectra. The partial loss of signal charge within the columnar electrodes themselves is unlikely, as there is no field to drive out the charge carriers and the capture lifetime is very short (a few nsecs) in the polysilicon. However, by this same argument, the column electrodes, which amount to ~1.4% of the surface area of the sensor, are considered to be X-ray insensitive. This fractional loss can to some extent be reduced by the fabrication of
narrower electrodes. We also intend to fabricate 3D detectors where the etched holes are backfilled with doped silicon that is grown epitaxially. If this epitaxy can be grown with sufficient charge recombination lifetime, charge created by X-rays absorbed within the electrodes will diffuse out, and the dead area represented by these electrodes will be made active.

3. DETECTOR FOR X-RAY CRYSTALLOGRAPHY

3.1 Detector Geometry

We have proposed a protein crystallography detector of cylindrical symmetry made up of columns of overlapping 3D sensors, each column 0.96cm wide. The sensors are shingled in both directions, and tilted so that X-rays scattered from the sample crystal are incident on the individual sensor elements at near perpendicular angles (figure 7a,c). This arrangement avoids a parallax effect, whereby off-perpendicular X-rays are absorbed exponentially at different depths in the silicon and appear smeared across two or more pixels, spoiling the detector’s spatial response. Consider a 30x30cm$^2$ array, placed 15cm from the crystal sample. For X-rays of energy 12.65keV (the Selenium edge energy, of great importance in protein crystallography), the Bragg 2q diffraction angle at the detector edge will be 45°, corresponding to
crystallographic data of 1.3Å resolution, a very satisfactory figure. As each sensor is at the optimal orientation with respect to the diffracting crystal sample, the maximum off-perpendicular angle for X-rays striking the sensor will be only 2.6°. The 3D sensors of 500µm thickness that will be used (of total X-ray absorption efficiency 87%) will have 150µm square pixels defined by the p column electrode pitch. Incident X-rays must deviate >16° to deposit energy over more than two pixels due to parallax, but this angle is never approached if the array to sample distance is kept reasonably close to its design value.

3.2 Electronic Readout

For silicon pixel detectors, the sub-picofarad input capacities permit the fabrication of a charge preamplifier and shaper with an electronic noise of ~300e-. This should be compared to the charge resulting from photoelectric absorption of a 12.6keV X-ray, which produces 3480e-. Thus, it is easy to set a discriminator level that ensures efficient ‘single photon’ counting with virtually no background counts arising from spurious electronic noise. Considering just a single pixel, this apparently permits the construction of a detector with a practical dynamic range limited only by the signal counting statistics. Pixel detectors currently under development for crystallography by other groups have adopted this approach, i.e. a complete chain of charge preamplifier-shaper, discriminator, and counter are placed under each X-ray sensing pixel. This counter-per-pixel approach suffers from a drawback however, namely the ‘splitting’ of events that must inevitably occur for incident X-rays absorbed at, or near, the boundaries between each pixel. In any semiconductor X-ray detector, there is a finite distance over which the charge created by the photoelectric effect must drift before its collection at some sensing electrode. During this drift, the charge diffuses spatially in three dimensions, hence a single X-ray event may deposit charge in two neighboring pixel elements. According to the level at which the electronic discrimination level has been set, and the fraction of charge collected in each pixel, a single X-ray will be subsequently recorded as a single count, two counts (if the threshold has been set too low), or not detected at all (if the threshold has been set too high). This ‘lost count’ problem is worse still when approaching the corner of a pixel, where charge is split up to four ways [17]. While this may be acceptable in semi-quantitative imaging applications, it will cause significant errors in the measurement of peak intensities in crystallography where the width of the diffraction peak incident on the detector is comparable to the pixel width.

We have adopted a different readout scheme. Figure 8 is a schematic of the readout integrated circuits that will be bonded to the 3D sensors at each p electrode location, using indium bumps or some other commercially available flip-chip process. This 'under pixel' circuitry, is being fabricated with 0.25µm CMOS technology, and will easily be kept within a cell dimension ~145µm, i.e. slightly smaller than the 3D pixel pitch. The mismatch between the detector active pixel size, and that of the readout circuit cell size, will enable us to saw cut the integrated circuit with a width smaller than that of the precisely dimensioned, plasma etch cut 3D sensor that will be mounted above it.

Referring to figure 8, a charge integrating preamplifier and column bus driver is contained under each pixel, as well as current offset trimming circuitry (not shown). The preamplifier has a reset transistor across its integrator, and in addition, a ‘hold’ capacitor connected to the output of the integrator. The other end of this hold capacitor is grounded during and immediately after reset, then switched to link the integrator with the output amplifier that drives the column bus during readout. This correlated double sampling (CDS) procedure subtracts out the

Figure 8: Simplified schematic of the electronic readout of the 3D integrated circuit. The cross-hatched areas depict two pixels of the 3D sensor that will be bump bonded above. The integrated circuit will extend by ~5mm beyond the edge of 0.96cm square 3D sensor side.
transistor thermal noise voltage that is present across the turned-on reset transistor channel and which is imposed on the integration capacitor during its reset (the so-called kTC noise). Running in the column direction up one side of the array is a shift register in which clock pulses from the readout logic sequencer drive a row select bit. Via its column driver, the signal output of each pixel integrator in a row is connected to the sample and hold circuit of its respective column ADC. All pixels in a given row start and end their charge integration and readout in synchronism, cyclically at a fixed period. At the end of the transfer of data to the column ADC sample and hold buffers, the entire row is reset and restarts its signal integration.

Wilkinson type ADCs are used to digitize the integrated charge values. We are using a proven design now employed in the Atlas collaboration SVX4 silicon strip readout chip [18]. In this, the signal on the ADC’s sample and hold buffer is applied to one side of a comparator that is present for every column, and a common ramp voltage is applied to the other input of all these comparators. When the common ramp voltage exceeds the signal voltage at the input of a particular comparator, the current value of the clock count, i.e. the measure of the signal value, is stored in a register for that column. After the data for the current pixel row N has been encoded and latched, the ramp voltage and clock counter are reset, integration in the next pixel row N+1 is stopped, and the process described above repeated for the next row. When the last row is has been encoded, the readout cycles back to the first row.

We will use a significantly modified version of the SVX4 readout sequencer that is capable of cycling through the readout of the 64 pixel rows of the 3D sensor. As the SVX4 geometry was designed for the readout of a row of 128 channels at 75µm pitch (i.e. it contains 128 ADC circuits), we will read-out double rows of 2 x 64 channels per cycle. Using a 40MHz clock, and allowing time for a minimal 6-bit ADC encoding, the time taken to completely readout the entire 3D sensor of 64 x 64 pixels will be 64µs. This entire sensor readout cycle time assumes, however, a process of sparsification of the data before it is output to subsequent data acquisition electronics. We will use the sparsification scheme of the SVX4 integrated circuit, configured in our application to identify and read-out any 5 pixels that are ‘hit’ in a double row group of 128 pixels. As explained below, only a few pixels will have hits, even at the highest global and local X-ray intensities that we anticipate.

With the scheme described, all rows are integrating signal almost all of the time, including the time while ADC encoding and subsequent digital electronics and computer readout is being carried out. The downstream data acquisition electronics and control computer will keep a running total of the charge sums for each pixel over multiple readout cycles of 64µs until the acquisition is stopped. The computer will not only be able to store a simple, total charge sum for each pixel, but also an ‘X ray quantum count’ like a true photon counting system. This will be possible as

1. The sensor readout cycle is fast enough so that at most only a few X rays will hit the busiest pixels during a 64µs cycle. In any particular readout cycle most pixels are not hit at all, as shown below.
2. Only mono-energetic X rays will be detected in our application, and the detector has sufficient energy resolution to clearly distinguish an X ray pulse from the preamplifier and Fano (i.e. charge statistics) noise contributions.

The computer will distinguish between the charge signal from N and N ± 1 X rays, where N is the number of hits during a particular readout cycle. The simplest algorithm to find the number N is just to divide the output ADC value by its calibrated average value for one X ray, then round the result to the nearest integer. By using more complex algorithms based on analog summation over neighboring pixels, charge sharing effects can also be minimized. A feature of 3D sensors that greatly simplifies this process is that the column electrodes that define the corners of each pixel repel charge, so that no significant amount of signal charge is shared with the four neighbor pixels that only touch at their corners. Note that for most of the time, the computer has only to distinguish between zero and one X-ray hit in a pixel.

Consider a mean count rate of 2x10^4 hits/mm²/second over the entire detector surface: this corresponds to only 0.03 events per 64µs readout cycle hitting each pixel. For the busiest pixels in the brightest diffraction spots, we expect to collect ~10^5 X rays/pixel/second, i.e. an average ~6 hits per 64µs readout cycle. The pixel preamplifier will be the dominant source of noise at 2 - 3keV (FWHM). The 3D detector room-temperature leakage current is ~1nA/mm², which for a 150µm square pixel will generate an offset corresponding to the charge integral over the 64µs readout cycle of ~4500e-. This is a worst case estimate as it is based on simple scaling-up of the current leakage measured on 121µm detectors to correspond to the final 500µm thickness, while we do not expect the contribution from surface leakage to increase with detector thickness. This integral has a statistical fluctuation of ~70e rms, corresponding to a noise of
0.6keV FWHM. This, and the detector Fano noise contribution of 0.17keV FWHM (for one 12.65keV X-ray) are both negligible when added in quadrature to the preamplifier noise. The stability over time of the offsets resulting from the individual pixel leakage currents is of more concern, so the leakage current for each pixel preamplifier will be individually compensated as part of a calibration procedure. With 6-bit ADC resolution, we shall be able to discriminate between N = 5, 6 or 7 hits with little error.

3.3 Practical Considerations

The spectra of Figure 6a,b,c were taken with an obsolete 5V, 1.2µm CMOS technology preamplifier that used a 50µm wide input transistor with a bias current of 0.3mA. For these measurements, sixteen of the 3D detector’s p electrodes were electrically ganged together and wire bonded to the charge preamplifier input, thus increasing input capacity and noise figure. For a bump-bonded array detector, using 0.25µm technology we can produce a charge preamplifier with an acceptable noise <300e− that will dissipate <0.25mW per channel. For the complete 64 x 64 pixel integrated circuit, including readout and other logic functions, we expect a maximum of 2W of power dissipation per sensor. This is tolerable but requires efficient heat transfer from the sensor modules to the mechanical support structure, which in turn will require temperature stabilization by water-cooling.

Radiation damage to either the 3D sensor or the CMOS readout circuitry must be considered. At current 3rd generation synchrotron undulator beamlines, typical protein crystallography diffraction measurements result in ~10⁹ X-ray photons in a single image frame, i.e. ~10²³ photons/mm² for a 30cm square detector. The central part of this detector will receive a higher signal intensity, which as a worst case we estimate as 10³ photons/mm². During a day, a beamline in constant operation may acquire up to 40 000 frames of data. Let us require that the detector must tolerate 10 years of service, at an expected maximum utilization of 250days/year. The extreme accumulated lifetime dose will then be ~10¹⁴ X-ray photons/mm². Taking an X-ray energy of 12.6keV, which has an absorption length of 260µm in silicon, this exposure corresponds to a silicon surface dose of ~350kGy.

Silicon itself is extremely resistant to damage from X-rays of energy <250keV, the threshold energy needed for displacement damage of the silicon lattice by photons [19]. Extensive practical studies over many years by the high-energy particle physics community have shown silicon to be highly tolerant, to beyond 1MGy, to X rays and electrons at energies <100keV [20]. The 3D sensors already produced have been themselves subjected to severe irradiation tests with an integrated proton flux up to 10¹⁵ protons/cm² (55MeV protons). Such high-energy protons disrupt the silicon crystalline lattice, creating charge-trapping defects, and are far more damaging than X-rays. However, the irradiated devices subsequently worked acceptably at room temperature over a 45V-wide plateau (bias voltages 105V to 150V). We conclude that the high-resistivity, silicon material of the 3D sensors will not be damaged by the expected radiation exposure.

Absorption of X-rays in the sensor’s surface field oxide will however generate trapped charge. Electrons preferentially escape the oxide if driven out by an applied electric field, while some of the positive charge holes are trapped. This increasing positive oxide charge forms an electron accumulation layer beneath the oxide which, unless precautions are taken, may result in large surface leakage currents in conventional, planar processed detectors. While the amount of trapped charge in a working 3D sensor might differ from that generated in our radiation tests made with unbiased sensors, it will not have a significant effect on hole collection, since an electron cloud attracted to the positive field oxide will be repelled from the negatively charged electrodes that collect holes. Surface implants, i.e. the creation of diode structures, and field plates [21] are possible means of controlling the effects of oxide charge build-up on the sensor.

Our principal concern is the radiation tolerance of the CMOS electronics used in the in the readout integrated circuit, which is susceptible to malfunction from trapped oxide charges. The amount of charge liberated by a single X-ray is not large, and much of it occurs in low or zero field conductive regions where it recombines, with the remainder quickly absorbed by the circuit with no noticeable long term effect (i.e. destructive ‘latch up’ is not a problem). However in the oxide layer, particularly those regions with high fields, hole charges move more slowly, mostly as hydrogen ions, and when they appear at the oxide-silicon borders they have a high trapping probability. There, they shift threshold voltages and increase the rate of capture and release of charges in the underlying conducting channel, increasing the noise in the analog circuitry. Fortunately, recent MOS integrated circuits that are fabricated with deep sub-micron features have correspondingly thin gate oxides. These circuits are inherently more radiation tolerant than their predecessors, as for a
given irradiation, they absorb less total energy so that less charge is created and trapped, and there is now a process of ‘self annealing’ whereby the trapped holes leak from the oxide. These circuits can also be designed with proven transistor guard structures that block radiation-induced leakage currents flowing under the field oxides. The circuits can also be astutely designed to anticipate radiation ageing effects, for example, large internal signals can be used, which are less affected by noise and threshold shifts.

At 12.6keV, only 13% of incident X-rays will pass through the 500µm thick 3D sensor to strike the CMOS readout chip behind it. Using the previous estimates of radiation exposure, and considering the absorption within silicon oxide, we obtain an extreme lifetime dose of ~60kGy. Standard 0.25µm CMOS process integrated circuits of similar complexity and function to those we require have already been made by other groups and shown to tolerate over 300kGy of 10keV X rays [22]. Indeed, in these experiments, no significant deterioration of these components was observed after this level of irradiation.

4. CONCLUSION

We have developed a reliable method for the production of silicon radiation sensors that employs 3-dimensional processing of the silicon bulk. This method presents advantages over conventional planar diode structures, and the processing of active edge electrode should permit the assembly of large area, tiled detectors without insensitive gaps. 3D detectors have been proven as excellent detectors of X-rays at the energies required for synchrotron crystallography experiments. We have presented a scheme for building a practical pixel array detector for protein crystallography that uses a novel readout method capable of compensating for residual effects of charge sharing between individual pixels. We are confident that this detector will tolerate the lifetime radiation dose that it will receive at a 3rd generation synchrotron beamline. Work on this project and the further refinement of 3D detectors is in progress.

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6. REFERENCES

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