Status of the Sirius RF BPM Electronics
IBIC2014, Monterey

Sérgio Rodrigo Marques
(on behalf of the beam diagnostics group)
Outline

• Introduction
• Stability Requirements
• General System Requirements
• FOFB Strategy
• Hardware Overview
• Performance Tests: Laboratory Bench
• Performance Tests: SPEAR3 Beam (SLAC/SSRL)
• Final Remarks
Introduction

LNLS UVX storage ring
1.37 GeV 2nd generation light source
Operating since 1997

Campinas, State of São Paulo, Brazil

Sirius
3 GeV light Source
First beam: mid-2018

Brazilian Center for Research in Energy and Materials
Introduction

Picture – December 2013
March 2014: Earthwork finalized
October 2014: Construction companies selection

Sirius
3 GeV, 0.28 nm, 5BA
518 meter circumference

LNLS-UVX Storage Ring

Sirius commissioning has been rescheduled and should occur in the 1st semester of 2018.
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## Requirements of Sirius RF BPM electronics

Requirements of Sirius RF BPM electronics.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (RMS) @ 0.1 Hz to 1 kHz</td>
<td>&lt; 80 nm</td>
</tr>
<tr>
<td>Resolution (RMS) @ turn-by-turn full bandwidth</td>
<td>&lt; 3 µm</td>
</tr>
<tr>
<td>1 hour position stability (RMS)</td>
<td>&lt; 0.14 µm</td>
</tr>
<tr>
<td>1 week stability (RMS)</td>
<td>&lt; 5 µm</td>
</tr>
<tr>
<td>Beam current dependence (decay mode)</td>
<td>&lt; 1 µm</td>
</tr>
<tr>
<td>Beam current dependence (top-up mode)</td>
<td>&lt; 0.14 µm</td>
</tr>
<tr>
<td>Filling pattern dependence</td>
<td>&lt; 5 µm</td>
</tr>
</tbody>
</table>

### Stability Requirements

- **Energy:** 3GeV
- **Natural emittance:** 0.28 nm.rad
- **RF frequency:** ~500 MHz
- **Natural bunch length:** ~ 8.8 ps
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Electron and photon beam position monitoring from accelerator’s control system

Storage ring Fast Orbit Feedback control: stabilizes beam orbit at sub-micron level

Orbit interlock: prevents machine from damage due to mis-steered high power photon beams

Machine studies: turn-by-turn readouts provide valuable information of machine behavior

Failure diagnostics: beam loss analysis (post-mortem)

General diagnostics
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FOFB Strategy

- Orbit correction algorithm
- Network latency (FOFB → Corrector)
- Power supply
- Corrector magnet + Vacuum Chamber
- BPM electronics
- BPM digital electronics
- Position measurement noise
- Orbit disturbance
- Beam orbit

- Network latency (FOFB ↔ BPM): < 10 μs latency
- 10 ~ 30 μs latency
- Position measurement noise: < 80 nm (0.1 Hz - 1 kHz)
- 10 kHz bandwidth
- ~ 110 kHz Update rate
- PS current noise
Vacuum chamber bandwidth = 14.80 kHz
BPM group delay = 3 × FOFB sampling period

Crossover frequency (Hz)

Total data distribution delay from/to FOFB controller (μs)
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Hardware Overview

RFFE v1 (block diagram and tests)


RFFE v2: (diagonal channels)

20 ns RF switches

Switching @ FOFB rate (~115 kHz)
Hardware Overview

FMC standard 130 MSP/s 16-bit ADC board

“Standard” features

- External clock input
- Adjustable oscillator’s frequency for internal clock
- FMC standard (FPGA Mezzanine Card)

Optimized for undersampling

PLL tuning for internal clock
Hardware Overview

More info online at:

6th meeting of the xTCA interest group
“A MicroTCA system for Sirius BPM”
Daniel Tavares (LNLS)
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Performance Tests: Bench

Block diagram of the setup used for the BPM electronics test

ADC clock / RF signals freq.:
- UVX: 476 / 113 MHz
- Sirius: 500/ 117 MHz

BPM geometric factor: $K = 10$ mm
Performance Tests: Bench

Beam Current Dependence – long range

The temperature dependence was kept below 140 nm under a 8°C degrees temperature variation.

Beam Current Dependence – short range

~2 days test
RMS X, Y < 140 nm
Data rate: ~10 Hz
Bandwidth: ~2 Hz
Diagonal switching scheme virtually eliminates electronic noise originated in the RF chain downstream of the switches up to a certain frequency...

Switching off

Switching on

Integrated RMS noise [nm]

Frequency [Hz]

Test setup

RF generator > RFFE v2 > 130 MSP/s ADC > FPGA kit

Compare
Red vs Brown and/or
Blue vs Black

Switching frequency
~ 110 kHz (complete cycle)

-10 dBm ~ 500 mA
-20 dBm ~ 160 mA
Performance Tests: Bench

The switching scheme introduces coherence between the diagonal channel pairs (A-C and B-D) from DC to approximately 40 kHz.

\[
C_{xy}(f) = \frac{|P_{xy}(f)|^2}{P_{xx}(f)P_{yy}(f)}
\]

**Low frequency range:**
High coherence (DC-100 Hz)

**Medium frequency range:**
Decreasing coherence (100 Hz - 40 kHz)

**High frequency range:**
No coherence (40 kHz - few GHz)

Switching @ ~ 110 kHz

![Test setup](image)
Performance Tests: Bench

Wrong FPGA calibration of delays between ADC clock and data paths caused the problem!

Test setup

RF generator > RFFE v1 > 130 MSP/s ADC > FPGA kit

Old result
IBIC’2013 (MOPC09)

New result

RF generator > RFFE v2 > 130 MSP/s ADC > FPGA kit
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Performance Tests: Beam

Block diagram of the setup used for the BPM electronics test

Testes performed at SPEAR3 (SLAC/SSRL)
Comparing real beam, real beam @ low alpha mode and RF generators

Low alpha bunch length ~ 4.5 ps
Users beam bunch length ~ 18 ps

Equivalent to ~40 mA
Equivalent to ~500 mA
Final Remarks

- Open Hardware repository: www.ohwr.org/projects
- Substantial integration work on the digital back-end will take place in 2015
- The performance of the Sirius BPM electronics “analog” hardware was improved
- Critical specifications are now met with exceeding performance
- BPM electronics design was performed in order to not limit the FOFB performance
- Efforts will be redirected to pre series production of RFFE and ADC boards in the 1st semester of 2015

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Thank you for your attention!