DEPFET Pixel Detectors for Particle and Astrophysics

- DEPFET Principle
- Single Pixel characteristics
- DEPFET prototypes for
  - XEUS
  - ILC Vertex detection

MPI HLL in collaboration with the Universities of Bonn and Mannheim
**DEPFET Principle**

- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand

J. Kemmer & G. Lutz, 1987
DEPFET Principle

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- internal amplification
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DEPFET Principle

- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand
Overview: Types and Applications

**X-ray imaging spectroscopy → XEUS**
- pixel size: 100µm
- r/o time per row: 2.5 µs
- Noise: ≈4 el ENC

**Particle tracking → vertex detector at ILC**
- pixel size: 25µm
- r/o time per row: 20..40ns
- Noise: ≈100 el ENC
- thin detectors: ≈50µm

**X-ray (imaging) spectroscopy**
DEPFET MacroPixel
- pixel size: 100s of µm
Source Follower vs Drain Readout

- Constant bias current $I_{\text{Bias}}$
- Change in channel conductivity translates into $\Delta V_{\text{Source}}$
- Low noise due to direct voltage amplification
- Speed depends on overall source capacitance ($\approx \mu$s)

Drain voltage kept constant
- Change in channel conductivity translates into $\Delta I_{\text{Drain}}$
- Control of all bias parameters
- Fast(!) - signal rise time limited by $R_{\text{in}}$, gate settling time... ($\approx \text{ns}$)
Internal Amplification $g_q$

Transconductance of the internal gate:

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2} (V_{GS} - V_{th})$$
**Measurement of $g_q$**

- **Drain readout setup**
- Measurement of $g_q$ in **dynamic mode** using charge integration
- Fixed clear frequency, illumination with $^{55}$Fe source
- Sampling output voltage after integration, before clear process
- Additional precharge by laser every second cycle to check linearity
- Result: **Pulse height spectrum**
Measurement of $g_q$

- Measured $g_q$ values meet expectations from simulations
- No dependence on precharge in observed range
- Charge handling capacity $O(10^5)$ electrons
1. Positive oxide charge and positively charged oxide traps have to be compensated by a more negative gate voltage: negative shift of the threshold voltage.

2. Increased density of interface traps: higher 1/f noise and reduced mobility ($g_m$).
Threshold voltage shift

GSF - National Research Center for Environment and Health, Munich

$^{60}$Co (1.17 MeV and 1.33 MeV)

No annealing during irradiation
→ ~ 3 days irradiation
Dose rate: ~ 20 krad(SiO$_2$)/h

![Graph showing threshold voltage shift vs. dose with markers for "ON" and "OFF" states.](image-url)
Transconductance and subthreshold slope

\[ N_{it} = \frac{C_{ox}}{kT} \cdot \ln(10) \cdot (s_{D2} - s_{D1}) \]

Literature:
After 1 Mrad 200 nm (SiO₂):
\[ N_{it} \approx 10^{13} \text{ cm}^{-2} \]

300 krad \( \rightarrow \) \( N_{it} \approx 2 \cdot 10^{11} \text{ cm}^{-2} \)
912 krad \( \rightarrow \) \( N_{it} \approx 7 \cdot 10^{11} \text{ cm}^{-2} \)
55Fe Spectrum (single pixel)

- **non-irradiated**
  - $V_{\text{thresh}} \approx -0.2 \text{V}$, $V_{\text{gate}} = -2 \text{V}$
  - $I_{\text{drain}} = 41 \mu\text{A}$
  - time cont. shaping $\tau = 10 \mu\text{s}$
  - Noise $\text{ENC} = 1.6 \text{ e}^- \text{ (rms)}$
  - at $T > 23 \text{ degC}$

- **912 krad $^{60}\text{Co}$**
  - $V_{\text{thresh}} \approx -4.0 \text{V}$, $V_{\text{gate}} = -6.0 \text{V}$
  - $I_{\text{drain}} = 40 \mu\text{A}$
  - time cont. shaping $\tau = 10 \mu\text{s}$
  - Noise $\text{ENC} = 3.5 \text{ e}^- \text{ (rms)}$
  - at $T > 23 \text{ degC}$
Noise vs. shaping time $\tau$

\[ ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau} \]

- Therm. noise
- $1/f$
- $I_L$
Noise vs. shaping time $\tau$

\[ ENC = \sqrt{\frac{2kT}{g_m} \frac{C_{\text{tot}}^2 A_1}{\tau} + 2\pi a_f C_{\text{tot}}^2 A_2 + qI_L A_3 \tau} \]

- Therm. noise
- $1/f$
- $I_L$
Matrix integration

Auxiliary ASICs needed:

- Switching circuitry (for rows) → "SWITCHER"
- Analog front-end circuit (for columns) → "CAMEX" or "CURO"
Matrix signal

- **Signal** sampling in row # n depends on integrated charge.
- Clear process: pixel returns to empty level = reference level.
- **Baseline** sampling in row # n: "empty" level pixel row # n - 1.
- **Baseline** sampling in row # n + 1: "empty" level pixel row # n - 1.

- Offset shift in time when switching to row # n + 1.
- Signal step for settling process in pixel row # n.
- Measure incomplete clear introduces additional noise.

- V_Source or I_Drain are used for switching processes.
- Study mini matrix devices in laser setup
- Scan wide parameter space of Clear Gate and Clear Voltage
- Study various designs, geometries (length of clear gate) and operating conditions (static or clocked clear gate)

Complete clear achieved with static clear gate!
Required voltages are small (5-7V) - very important for future SWITCHER!
Fast Clearing

- Study clear efficiency for short clear pulses

Device with common clear gate

Complete clear in only 10-20 ns @ $\Delta V_{\text{clear}} = 11-7 \text{ V}$
The XEUS mission

Status:
Mission under assessment

- Payload definition completed
- PDD (strawman payload)
- Feasibility study
- Decision: end 2006 / beg. 2007

Mission concept:
- Increased focal length (35m - 50 m)
- X-ray telescope consisting of two satellites
- Energy range: 0.1 - 40 keV
- Mirror area 2m² at 6keV and 5m² at 1keV

Launch ~ 2015+
Baseline instrumentation

Core payload complement:

1: Wide Field Imager: DEPFET APS

2: Narrow Field Imager
   - option 1: superconducting tunnel junctions at 250 mK
   - option 2: micro calorimeter at 50 mK
**XEUS prototype**

- **DEPFET XEUS Prototype**
  - 75x75 $\mu m^2$ pixel
  - 64x64 pixel matrix
XEUS prototype - Spectroscopy

Energy resolution: 126 eV FWHM @ Mn-Kα Line corresponding to 4.9 e⁻ ENC

Conditions

- Nitrogen atmosphere
- Temperature: -50°C
- Frame rate 300 Hz
- Pixel current 30 μA
- Line processing time 25 μs
- "frontside" illumination
Imaging with $^{55}$Fe

- Illumination from backside
- Baffle: 300 $\mu$m thick silicon
- Minimal structure size: 150 $\mu$m
- Exposure ca. 100000 frames

- Contour plot from ADU maps

- Hitmap with 100 ADU threshold
Generic Layout of the ILC Vertex Detector

- $\sigma_d \leq 5 \mu m \oplus 10 \mu m/(p \cdot \sin^{3/2}\Theta)$
- pixel size: 20-30 $\mu m$
- low mass: 0.1 %Xo per layer
- fast(!): 20 - 40 ns/row

1st layer module: 100x13 mm$^2$, 2nd-5th layer: 125x22 mm$^2 \Rightarrow \Sigma 120$ modules
Compact linear DEPFETs

smallest pixel cell 22.5 x 36 µm²
limited by technology: smallest feature size ≈ 2µm

Double pixel cells:
reduces the required read out speed by 2 → doubles the number of readout channels
Module Concept: "all-silicon module"

- Cavities in frame can save material
- Chips are thinned to 50 µm, connection via bump bonding
- Thinned sensor (50 µm) in active area
- Thick support frame (~300 µm)

Material budget (1st layer, incl. steering chips and frame) \( \approx 0.11 \% X_0 \)
ILC Prototype System

- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8µm AMS HV technology
- Radhard version in progress

See Poster 231, Marcel Trimpl: "A DEPFET Pixel System for the ILC Vertex Detector"
Testbeam at DESY, Jan. ’06

- DESY test beam with 1-6 GeV e-
- Bonn ATLAS telescope system: double sided strip detectors, 300µm pitch 50 µm (no intermediate strips)

- bias scans (→cluster size)
- energy scans (→resolution)
- different readout modes...

5 Hybrids with different matrices under test all 450 µm thick

<table>
<thead>
<tr>
<th>Name</th>
<th>Wafer</th>
<th>Type</th>
<th>Pixelsize (µm)</th>
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<tr>
<td>Hyb1B</td>
<td>W09 003</td>
<td>CCG nonHE rec small</td>
<td>33×23.75</td>
</tr>
<tr>
<td>Hyb1A</td>
<td>W11 J12</td>
<td>CCG HE rec small</td>
<td>33×23.75</td>
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<td>Hyb2A</td>
<td>W11 B03</td>
<td>CCG HE rec small A</td>
<td>36×22</td>
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<tr>
<td>HybMun1</td>
<td></td>
<td>CCG nonHE rec small</td>
<td>33×23.75</td>
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<tr>
<td>HybGCG</td>
<td></td>
<td>GCG nonHE</td>
<td>36×28.5</td>
</tr>
</tbody>
</table>

Some results →
• **Testbeam at DESY, Jan. ’06**

- **S/N ≈ 114** (for 450 µm sensor!)
- **Noise** about 250 - 300 e- ENC
  - Usual suspects: system x-talk
  - CURO, external I2V converter...
  - There is still room for improvement

- **Clock 50 Mhz ... but ...**
- **Read all channels** (no zero suppression)
- ~ 800 µs/frame (64 rows) \(\rightarrow\) ~ 12 µs/row
- **Sample-clear-sample:** ~ 240 ns
- **Clear duration 20ns**
Efficiency & Position resolution

Efficiency = \frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}

Purity = \frac{\text{Number of clusters with track}}{\text{Total number of clusters}}

For 5 \sigma seed cut
- Efficiency \approx 99.8\%
- Purity \approx 99.6 \%

After corrections for MS (6GeV electrons!!)
Position resolution about 3 - 5 \mu m
(for 33x23.75 \mu m^2 pixels)
In Summary....

..... there is so much more to be say and to present but I have to stop here.

The new generation of DEPFETs developed for

- space based X-spectroscopy and imaging
- vertexing at future collider experiments

is ready to go for the next round, i.e. the production of larger matrices in 2006
Backup slides
Processing thin detectors

a) oxidation and back side implant of top wafer

Handle <100> Wafer

Top Wafer

b) wafer bonding and grinding/polishing of top wafer

c) process → passivation

open backside passivation

d) anisotropic deep etching opens "windows" in handle wafer

50 µm, 4 diodes, 10 mm²

reverse current (pA)

700..850 pA/cm²
Energy resolution: best value

“Frontside” illumination:
Source illuminates electronic side

Energy resolution:
126 eV FWHM @ Mn-Kα Line
corresponding to 4.9 e- ENC

“Backside” illumination:
Source on top of entrance window

Energy resolution:
132 eV FWHM @ Mn-Kα Line
corresponding to 6.6 e- ENC
WFI requirements

Device dimensions
- Device active area 10.4 x 10.4 cm²
- Monolithic sensor integrated onto a single wafer
- Device thickness 450 µm
- Pixel size 100 x 100 µm²
- Total 1024 x 1024 pixel cells

Quantum efficiency
- Thin homogeneous entrance window
- Fill factor = 1
- QE @ C-Kα (282 eV) 90 %
- QE @ Si-Kα (1740 eV) 100 %
- QE @ Cu-Kα (8050 eV) 100 %
- QE @ 10 keV 96 %
- QE @ 20 keV 45 %

Spectroscopy
- Energy resolution @ Mn-Kα 125 eV
- Energy resolution @ C-Kα 50 eV
- System noise 3-5 e⁻ ENC

Readout timing
- Total readout time / frame 1 - 2 ms
- Processing time per detector row 2.5 - 4 µs
- Total raw data rate 2 GByte / s
Measurement of clear efficiency

- Drain readout setup
- Clear pulse lengths > 150 ns feasible with setup
- Clear process by diffusion & drift
- Charge injection by laser in one cycle
- Number of dark cycles follow
- Observation of dc levels at pixel output
- Sampling before and after the laser signal and after the first clear

Case of incomplete clear:

- Pixel in dynamic equilibrium
- Different dc levels after each clear
- No saturation of dc levels

Result: Pulse height spectrum
Leakage current and $g_q$

**Non-irradiated:**
Leakage current into the internal gate:

$I_{\text{Leak}} = 5 \text{ fA} \ldots 22 \text{ fA}$

*Internal amplification*

$g_q = 350 \text{ pA/e-}$

**912 krad $^{60}$Co:**
Leakage current into the internal gate:

$I_{\text{Leak}} = 156 \text{ fA}$

*Internal amplification*

$g_q = 335 \text{ pA/e-}$
Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 µm pixel)

DEPFET matrix only:
- 1st layer: 2 rows active, 30 µA · 5V · 650 · 2 · 8 = 1.6 W
- 2nd..5th layer: 1 row active, 30 µA · 5V · 1100 · 1 · 112 = 18.5 W

Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel
- 1st layer: [(4998 · 0.15 mW)+(2 · 300mW)] · 8 = 10.8 W
- 2nd..5th layer: [(6249 · 0.15 mW)+(1 · 300mW)] · 112 = 138.6 W

Σ active region ≈ 170 W
% duty cycle ILC 1/200 → ≈ 0.9 W

r/o chips (current version): 2.8 mW/chn.
for the whole vtx-d: ≈ 2 W
Clear Gate after irradiation ($^{60}$Co)