Status of a DEPFET pixel system for the ILC vertex detector

M. Trimpl, M. Koch, R. Kohrs, H. Krüger, P. Lodomez, L. Reuen, C. Sandow, E. v. Törne, J.J. Velthuis, N. Wermes

Physikalisches Institut, University of Bonn, Nussallee 12, D-53115 Bonn, Germany

L. Andricek, H.G. Moser, R.H. Richter, G.Lutz

Max-Planck-Institut für Physik, Föhringer Ring 6, D-80805 München, Germany

F. Giesen, P. Fischer, I. Peric

Institut für Technische Informatik, B 6, 26, D-68131 Mannheim, Germany

We have developed a prototype system for the ILC vertex detector based on DEPFET pixels. The system operates a 128×64 matrix (with $\sim 35 \times 25\,\mu m^2$ large pixels) and uses two dedicated microchips, the SWITCHER II chip for matrix steering and the CURO II chip for readout. The system development has been driven by the final ILC requirements which above all demand a detector thinned to $50\,\mu m$ and a row wise read out with line rates of $20\,MHz$ and more. The targeted noise performance for the DEPFET technology is in the range of ENC=$100\,e^-$. The functionality of the system has been demonstrated using different radioactive sources in an energy range from 6 to $40\,keV$. In recent test beam experiments using $6\,GeV$ electrons, a signal-to-noise ratio of S/N ~ 120 has been achieved with present sensors being $450\,\mu m$ thick. For improved DEPFET systems using $50\,\mu m$ thin sensors in future, a signal-to-noise of 40 is expected.

1. Introduction

The future International Linear Collider (ILC) will enter a new era of vertex detection. With the aimed impact parameter resolution of $\sigma\,(d_0) = (3.9 \oplus 7.8/p \cdot \sin^{\frac{3}{2}}\theta)\,\mu m$ precision physics will become possible which complements the discovery potential of the LHC machine. To achieve such outstanding performance, the ILC vertex detector requires a row wise operation where all sensor periphery is placed outside the sensitive area and detector layers that are thinned to $50\,\mu m$ or even below. Furthermore, the emerging background rates due to the high luminosity beam necessitate the readout of the whole detector in $50\,\mu s$ which translates into line rates of $20\,MHz$ and more.

2. DEPFET technology for the ILC

One technological option presently discussed for the ILC vertex detector is the DEPFET concept. The basic principle of operation of the DEPFET is illustrated in figure 1. The DEPFET (abbreviated **DEP**leted **F**ield **E**ffect **T**ransistor) [1] combines in-pixel amplification and particle detection by embedding a FET in high-ohmic silicon material. The sensor is fully depleted due to sidewards depletion from the backside contact and from the transistor channel jointly. The sidewards depletion and additional implantations close to the detector front side form a laterally confined potential valley underneath the transistor channel. This potential valley is called internal gate, derived from the external gate of the transistor. Electrons generated by impinging radiation drift to the internal gate where they are collected. The potential of the internal gate changes due to the collected
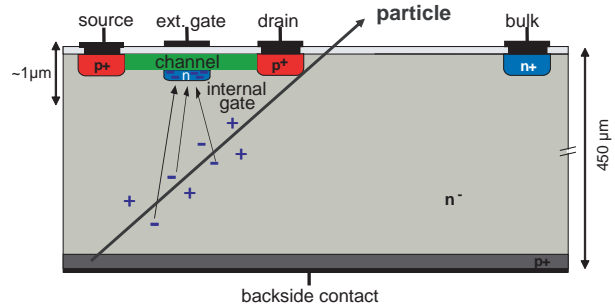

Figure 1: Cross section of a DEPFET pixel illustrating the basic principle of operation.

charge Δq and the transistor current is modulated according to $\Delta I_D = g_q \cdot \Delta q$, where g_q is called the internal gain of the DEPFET transistor, equivalent to the transconductance of the external gate g_m. Finally, the signal charge collected in the internal gate can be determined by measuring the device current. Since the readout of the device current does not affect the charge in the internal gate, it has to be removed from time to time. This is know as the clear of the device and is realized by an additional contact at the pixel fringe (not shown in figure 1). The main advantages of the DEPFET technology are the fully depleted bulk that is used for signal generation and the fact that charge collection is induced by an electric field.

Since the DEPFET concept relies on a backside contact to provide the fully depletion, new thinning concepts apart from the standard ones used in microchip industry need to be explored to fabricate thin DEPFETs. The present approach for thinning DEPFET modules is based on wafer bonding technology and anisotropic etching. The principle has been demonstrated by producing thin diode structures [2] and will be combined with a large scale DEPFET pixel
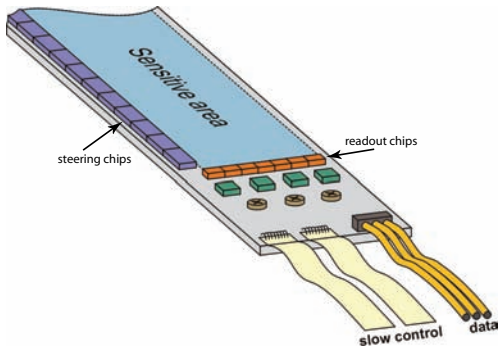
Figure 2: Sketch of one end of an ILC vertex detector laddder with thinned sensitive area, supported by a silicon frame that carries steering and readout chips.

production in future. The radiation tolerance of the sensor against ionizing radiation has been shown up to a dose of 1 MRad using X-rays from a ^{60}Co source [3].

A principle sketch of one ladder end proposed for a DEPFET ILC vertex detector is shown in figure 2. The sensitive area is thinned to $50\,\mu$m keeping a thicker frame ($\sim 300\,\mu$m) for mechanical stability and stiffening of the 100 mm long and 13 mm wide ladder. The steering chips for row selection and clearing strobes are situated at the longer side so that the detector is read out row wise to the ladder ends. There, readout chips are placed that process all matrix columns in parallel.

Concerning the readout of such a DEPFET ladder, new concepts have been explored as well [4]. Since the device signal of the DEPFET is a current, the most natural way is to adapt the signal processing queue to the current operation of the device. Therefore, current memory cells are used in the readout chip for temporal storage and processing of the signal current. The basic principle of operation of such a memory cell [5] is shown in figure 3. The cell operates as a dynamic current mirror, where transistor M1 works as
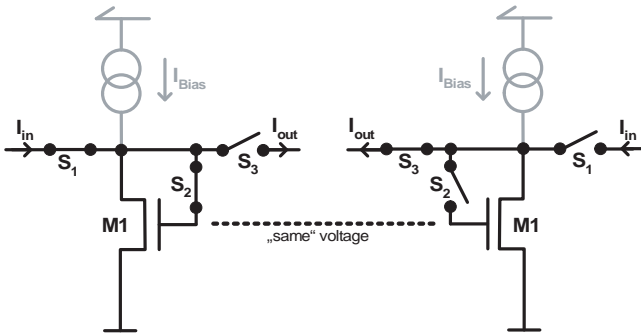

Figure 3: Basic principle of a current memory cell [5] used for signal processing in the readout chip. The circuit configuration is shown in the sampling mode (left) and in the hold mode (right).
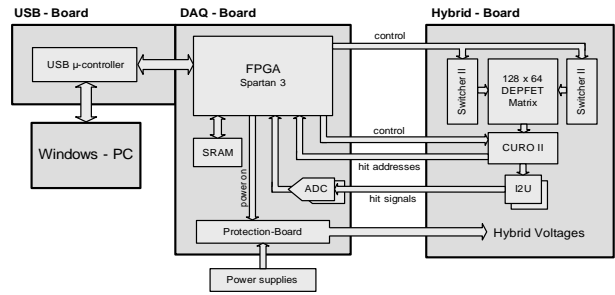

Figure 4: Schematic overview of the ILC DEPFET pixel system.

the input and output stage depending on the setting of the different switches S1-S3. Apart from the fact that a direct signal processing without any current to voltage conversion is smart, additional advantages of operating in the current domain exist, upon the most important ones are:

- The voltage sampled at the gate of the transistor M1 in figure 3 is not directly proportional to the signal current. Hence, a higher dynamic range compared to a voltage sample and hold can be achieved. This is particularly important for emerging process technologies with reduced supply voltage.

- The subtraction of two values, as needed for pedestal subtraction, can be done very accurate and easily with currents.

3. The DEPFET pixel system

As an intermediate step towards a full scale ILC detector ladder, a prototype system using a 128×64 DEPFET pixel matrix has been developed. A schematic overview of the system is given in figure 4. It consists of three major parts: a USB-Board, a DAQ-Board and a Hybrid-Board. The USB-Board is based on USB 2.0 standard and provides the communication between the system and a PC. The Hybrid-Board hosts the DEPFET pixel matrix, the steering chips SWITCHER II, the readout chip CURO II and a pair of transimpedance amplifiers (I2U) that convert the current outputs of the CURO chip to voltage signals. The DAQ-Board carries two 14 bit ADCs for digitization and a SRAM for data storage. Integral part of the DAQ-Board is a SPARTAN 3 FPGA which provides the configuration of all chips in the system and manages the synchronization between the components during data acquisition. An external Protection-Board can be inserted to safeguard the power supply voltages. A photograph of the DEPFET system is shown in figure 5.

Figure 6 shows a close-up view of the chip assembly on the Hybrid-Board. The 128×64 pixel
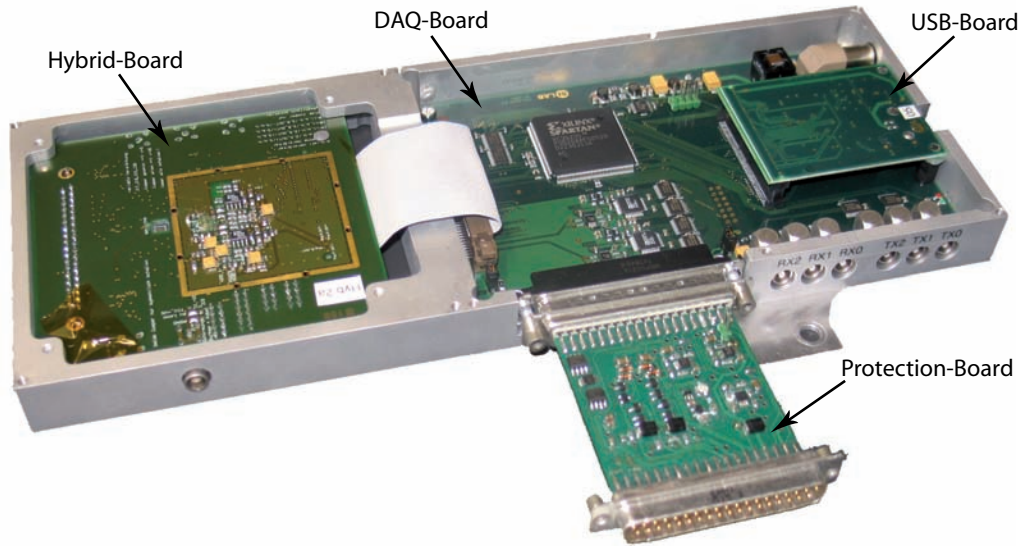
Figure 5: Photograph of the ILC DEPFET pixel system consisting of USB-Board, DAQ-Board and Hybrid-Board. The optional Protection-Board is attached at the bottom of the system.
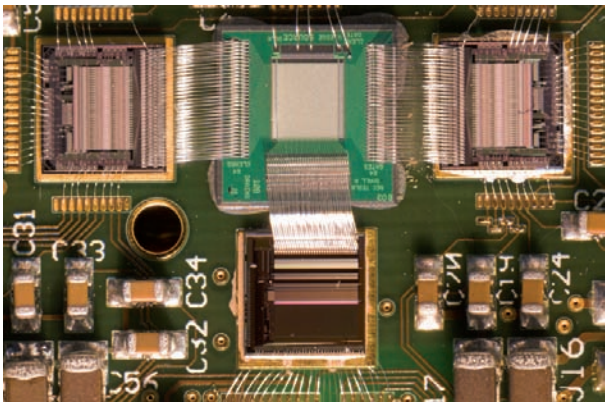

Figure 6: Chip assembly on the Hybrid-Board showing the DEPFET matrix in the middle, the two steering chips SWITCHER II at both sides and the readout chip CURO II at the bottom (area shown $\sim 23 \times 15 \, \mathrm{mm}^2$).

DEPFET matrix is situated in the center. The steering strobes for the matrix are provided by two SWITCHER II chips [6] located at both matrix sides. The SWITCHER II has been fabricated in an AMS high voltage process to provide a voltage range of up to 25 V, needed to operate some matrix designs. The present hybrid uses two steering chips to be very versatile in operating different matrix types. Recent measurements [7] show that for some matrix designs only one steering chip is sufficient to take care of matrix steering and clearing.

At the bottom of the matrix the 128 channel readout chip CURO II [8] is placed. This chip is fabricated in a $0.25 \, \mu\mathrm{m}$ TSMC process. In addition, most of the design already uses radiation tolerant layout rules [9].

It is therefore very likely that the readout chip sustains the radiation dose of 200 kRad expected after 5 years operation of the ILC. Whether the present chip already shows a suitable radiation tolerance or if the layout has to be improved further on will be studied in irradiation test.

One of the main features of the readout chip are on-chip pedestal subtraction and zero suppression. The zero suppression is performed by a scanner which scans the binary hit pattern in parallel. Standalone tests with the present CURO II chip show that the scanner finds up to two hits in a 128 channel hit pattern with rates of more than 100 MHz. This is much faster than needed to cope with the expected rates at the ILC.

4. Lab Measurements

The system has been used in the lab for X-ray detection in an energy range from 5.9 up to 44.23 keV. The capability of spatial detection of X-rays has been demonstrated using a $75 \, \mu\mathrm{m}$ thick tungsten test chart with an engraved logo and several line structures having a pitch of 100, 75, 50 and $25 \, \mu\mathrm{m}$ (from left to right, respectively). The radiogram of the $\sim 2 \times 3 \, \mathrm{mm}^2$ large test chart is shown in figure 7. The test chart has been placed on the backside of the detector and the system has been irradiated with a ^{55}Fe source. The radiogram has been obtained by summing the pulse heights for pixels that contain a signal higher than five times their noise. Although no spatial reconstruction techniques have been applied to improve the spatial resolution, the $50 \, \mu\mathrm{m}$ lines in the radiogram are clearly visible.

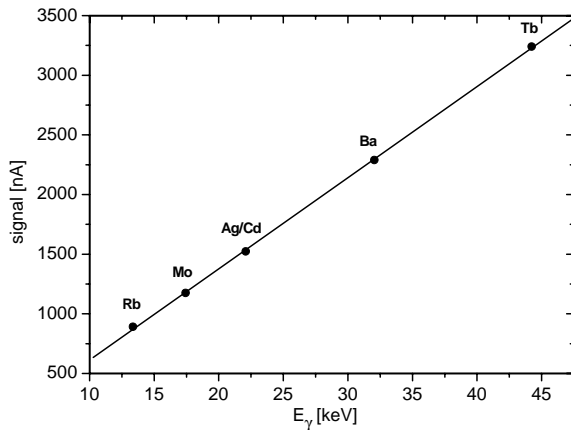Figure 7: Radiogram of a $2 \times 3\,\mathrm{mm}^2$ tungsten test chart taken with ^{55}Fe.

Figure 8: Gain measurement of the DEPFET pixel system. The sensor response is plotted for different radioactive sources.

Figure 9: Signal distribution for clusters with up to 3×3 pixels.

To determine the internal gain of the DEPFET device and to measure the linearity of the system, energy spectra have been taken for Rubidium (Rb), Molybdenum (Mo), Silver (Ag), Cadmium (Cd), Barium (Ba) and Terbium (Tb), provided by a variable X-ray source [11]. After performing a row-wise common mode correction[1], clusters are reconstructed by identifying neighboring pixels, where every pixel contains a signal higher than five times its noise. In figure 8 the mean cluster signal as a function of the characteristic X-ray energy is shown. From the slope of the system response an internal gain of the DEPFET sensor of $g_q = 282.6 \pm 3.3\,\mathrm{pA/e^-}$ is extracted. The integral-non-linearity (INL) of the system is better than $0.8\,\%$ for a dynamic range of $8500\,\mathrm{e^-}$. This range is large enough for the detection of about 2 MIPs in a $50\,\mu\mathrm{m}$ thin sensor device.

The best noise performance achieved in the lab is around ENC=$220\,\mathrm{e^-}$ at room temperature. This number is quite comparable with the calculated noise performance of ENC $\sim 190\,\mathrm{e^-}$, where thermal noise is identified as the dominant contribution [10]. However, the total noise needs to be improved by a factor of two to achieve the final aim of around $100\,\mathrm{e^-}$. This is within a realistic scope since the bandwidth of the present readout and steering chips have already been designed to cope with the final line rate of $20\,\mathrm{MHz}$. It is therefore very likely that a future generation of the system with an optimized readout chip and sensors with higher g_q can achieve a noise of $100\,\mathrm{e^-}$.

5. Beam Tests

The system has been tested for MIP detection in the $6\,\mathrm{GeV}$ electron test beam at the DESY synchrotron. The analysis of the data is done in the following way: After pedestal and common mode corrections, clusters are searched for. Seeds are identified with a threshold cut of $5\,\sigma$. The seeds are combined with neighboring pixels if their signal is two times higher than the noise.

The signal distribution for clusters containing a maximum of 3×3 pixels is shown in figure 9. The observed most probable value of about $36000\,\mathrm{e^-}$ ($1796 \pm 3\,\mathrm{ADU}$) obtained by a landau fit complies with the expected MIP signal in a $450\,\mu\mathrm{m}$ silicon sensor material. The system noise extracted from the noise peak of the raw data spectrum is found to be $15.723 \pm 0.007\,\mathrm{ADU}$. This combines to a signal-to-noise ratio of 114.2 ± 0.2. The observed noise figure in the test beam ($\sim 300\,\mathrm{e^-}$) is higher than the one achieved in the lab. It turned out that the connection node between readout chip and transimpedance amplifier is very sensitive for

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[1]Subtraction of a mean value (common mode) from the pixel pedestal. The common mode is computed using the pedestals of each pixel of a row that contain no signal.
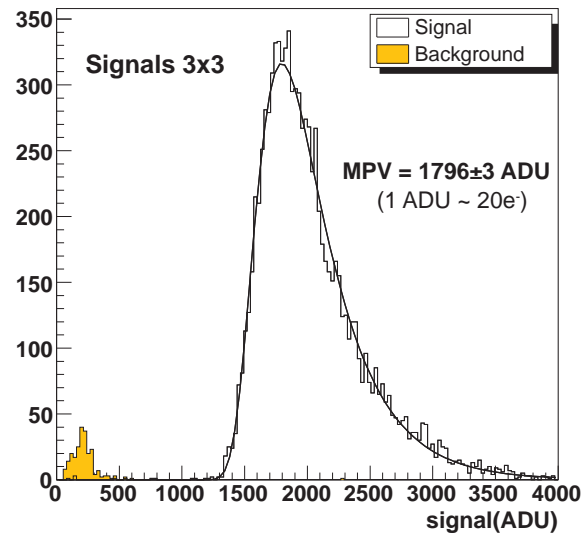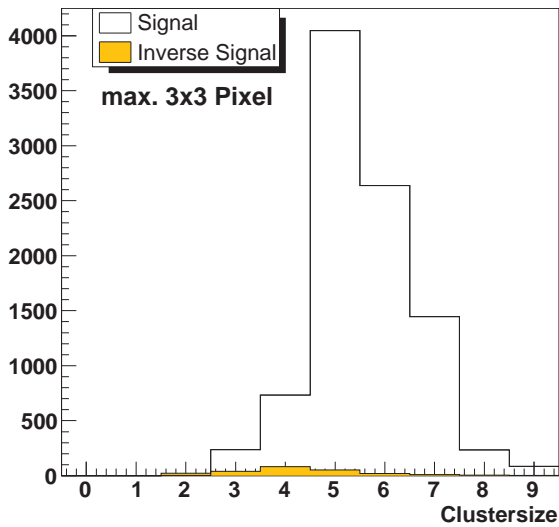
Figure 10: Cluster size distribution for a maximum of 3×3 pixels.
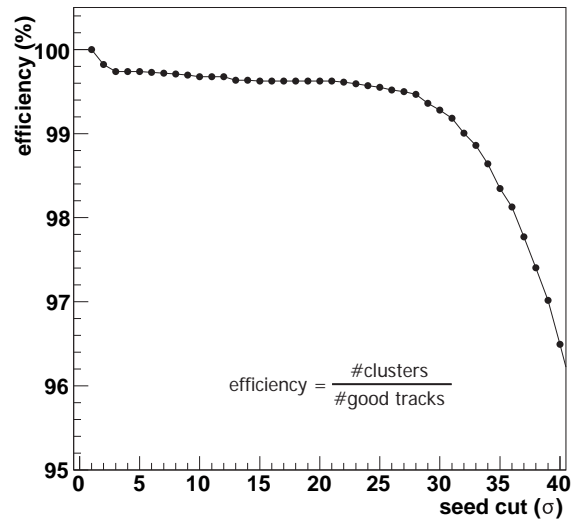

Figure 11: Efficiency to find a track as a function of the seed cut.

Figure 12: Track purity as a function of the seed cut.

pick-up. Hence, the system noise depends on different operating parameters. A future version of the readout chip implementing either a transimpedance amplifier or a current mode ADC is expected to overcome this.

Figure 10 shows the cluster size distribution. The most probable cluster contains about 5 pixels only. The relatively small clusters are due to the fact that charge collection in the DEPFET is done by an electric field and not by thermal diffusion. Also shown in figure 10 is the cluster size distribution for inverse signals. This event distribution is obtained by inverting the signals and repeating the analysis. It is very likely that the inverted signals are due to out-of-time events[2].

Furthermore, efficiency and purity for track reconstruction have been studied. A four plane telescope system is used to determine the particle tracks. Clusters are searched in the DEPFET matrix within an area of ± 2 pixels around the predicted track position. The efficiency is defined as the ratio of clusters found in the fiducial DEPFET area and the corresponding tracks identified by the telescope system. Figure 11 shows the efficiency as a function of the seed cut threshold. The observed inefficiency in the order of 0.3% is mostly due to multiple scattering effects in the low energy electron beam. (Note, that clusters are detected in a relatively small area of ± 2 pixels.) To reduce multiple scattering effects, only very stiff tracks are selected for the analysis by applying a high χ^2 probability cut of 0.9995. This enhances the efficiency to almost 100% ($> 99.99\%$).

The purity defined as the ratio of found good clusters and all clusters is shown in figure 12 as a function of the seed cut. The main result of the efficiency and purity study is that an operation at almost 100% purity and efficiency is achieved by choosing a seed cut of $5 - 7\,\sigma$. Note, that this threshold corresponds to only $\sim 5\%$ of a MIP signal.

6. Conclusion and Outlook

A prototype system for the ILC vertex detector based on DEPFET pixels has been developed. The system has been successfully used for X-ray and MIP detection. The current benchmarks of the system are:

- Noise performance of about ENC=220 e$^-$,

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[2]Events that occur between the clear of the sensor and the pedestal measurement.

- line rate of 2 MHz,

- S/N∼120 for MIPs using a 450 μm sensor.

Concerning position resolution, the present test beam data yields an upper limit of 5 μm dominated by multiple scattering effects. A more precise measurement will be performed in the high energy test beam at CERN in summer 2006.

To achieve the final ILC specifications the system still needs improvements. Most importantly, the line rate needs to be increased by a factor of 10. The single components of the systems have already been tested up to a line rate of more than 20 MHz, whereas their synchronization in the system needs further optimization. Moreover, the noise performance has to be improved by a factor of two. Based on calculations and the experience with the present system, we are very confident that this will be achieved with the next version of DEPFET sensors and readout chip.

As a next step, new generations of all system components are designed and fabricated. Large DEPFET matrices with up to 512×512 pixels are in production. The pixel size is reduced to $25 \times 25 \, \mu m^2$ and the internal gain of the sensor is optimized.

A new steering chip using a standard, low voltage process is designed. Some DEPFET designs having a so called *cleargate structure* can be cleared at much lower voltages than offered by the present steering chip. Hence, the use of a submicron process is possible here as well. This promises a much better radiation tolerance compared to the present chip using a high voltage technology.

A new generation of the readout chip is designed as well. Operating the system with a duty cycle as close as possible to the bunch timing of the accelerator (1:199) will reduce the total power consumption significantly. Hence, one of the most important conceptual extension of the readout chip will be a power down feature.

On a longer time scale, a major step is to combine the thinning technology with a DEPFET production in order to fabricate thin DEPFET sensors. Together with the aimed noise figure of ENC=100 e^-, a signal-to-noise ratio of 40 is expected for these thin devices.

Acknowledgments

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