Monitoring of the Fabrication Process of Silicon Strip Sensors for Large Scale Productions

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The Compact Muon Solenoid (CMS) is one of the experiments at the Large Hadron Collider (LHC) currently under construction at CERN. Its inner tracking system consists of the world's largest Silicon Strip Tracker (SST) which implements around 25000 silicon sensors covering an area of 200 m^2. The CMS collaboration developed a detailed quality assurance scheme in order to ensure the functionality of all these sensors for the full LHC lifetime. After explaining the basic elements of the quality assurance program the measurements performed on the sensors and on dedicated test structures will be presented. During the production several severe problems were identified and eventually solved in cooperation with the manufacturing companies. Results from these measurements will be shown.

1. CMS TRACKER OVERVIEW

The CMS experiment is one of the four large detectors for the Large Hadron Collider (LHC), which is currently under construction at CERN and will become operational in 2007. One of the most important features of CMS will be the reconstruction of charged particle tracks with high resolution and the determination of its momentum and impact parameters [1, 2]. To achieve this goal CMS is equipped with a sophisticated tracking system consisting of a pixel detector very close to the intersection point and a large Silicon Strip Tracker (SST) around it. The SST populates a cylindrical volume of 5.4 m length and 2.4 m diameter and consists of four inner barrel (TIB) and six outer barrel (TOB) detector layers. In the forward region three planes of silicon sensors are forming the inner disks (TID) and seven rings of two times nine disks are called the two endcaps (TEC). This layout is shown in figure 1. With this geometry a pseudorapidity up to $|\eta| \leq 2.5$ is covered.

1.1. Silicon Sensors Design

The SST can be divided into two regions, the inner and the outer part. TIB, TID and four innermost rings of the TEC are forming the inner region while TOB and the three outermost rings of TEC are part of the outer region. For the inner region the detector modules are built with silicon sensors of 320 μm thickness, while the detector modules of the outer region are designed to house sensors of 500 μm thickness. All of the inner detectors will be fabricated using wafers of 1.25-3.25 kΩ cm resistivity whereas the outer unit silicon sensors will be made of wafers with higher resistivity (3.5-7.5 kΩ cm) [3]. By using low-resistivity silicon wafers for the inner region, the type inversion caused by irradiation for those sensors is delayed which results in a lower depletion voltage after the planned 10 years of LHC operation.

Each detection unit in the inner region is composed of a single microstrip sensor, while the detector modules in the outer region are built by two daisy-chained sensors. The first two layers of TIB and TOB, the first two rings of TID and rings 1, 2 and 5 of TEC are instrumented with double-sided modules. These are made with two independent single-sided detection units, mounted back-to-back, with the second one being rotated by 100 mrad with respect to the first.

The silicon sensors are fabricated by two companies, Hamamatsu Photonics KK (Japan) and ST Microeletronics (Catania, Italy). The japanese company is called *HPK* and the italian vendor *STM* from now on.

The silicon detectors chosen for the CMS tracker are single-sided silicon strip sensors with either 512 or 768 implanted p^+ strips with a pitch between 80 and 205 μm without any intermediate strips in the n-type bulk material [4]. The width of the implant depends on the strip pitch where a constant width/pitch ratio of 0.25 is used. A dielectric sandwich layer composed of silicon oxide (SiO_2) and silicon nitride (Si_3N_4) between p^+ implant and metallization allows an AC coupled readout. A metal overhang above the p^+ strips improves the field configuration to ensure a stable detector behaviour with respect to the high bias voltage up to 450 V. This bias voltage is applied between the metallized backplane of the sensor and the bias ring. A guard ring around the bias ring also helps to reach the HV stability by a very large metal overhang on the outer side which acts like a multi-guard structure. The p^+ strips are connected to the bias ring via polysilicon resistors of $1.5 \pm 0.5 M\Omega$ each. At both sides of the sensor each strip has large contact pads with opens in the passivation to allow wire bonding and probe connections for testing (AC-pads). Additionally, there

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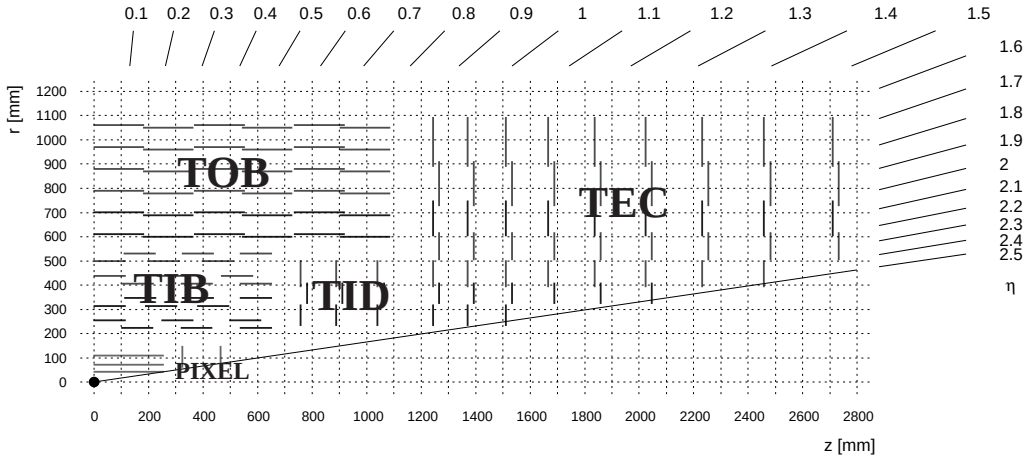

Figure 1: Longitudinal view of one quarter of the CMS Silicon Tracker.

is one DC pad per strip at one side of the detector which allows a direct connection to the p^+ implant underneath the aluminum. The cross-section of such a device can be seen in figure 2 and figure 3 shows a picture of the sensor corner, where the bias and the guard ring, the strips with its corresponding AC (aluminum) and DC (implant) pads and the polysilicon resistor can be seen.

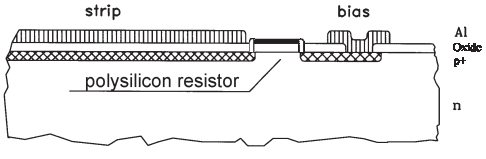

Figure 2: Sensor Profile. The strips are made of p^+-implants in n-type bulk material connected with polysilicon resistors to the bias ring. The implant is covered by dielectric insulation where the metallized strips are placed above.

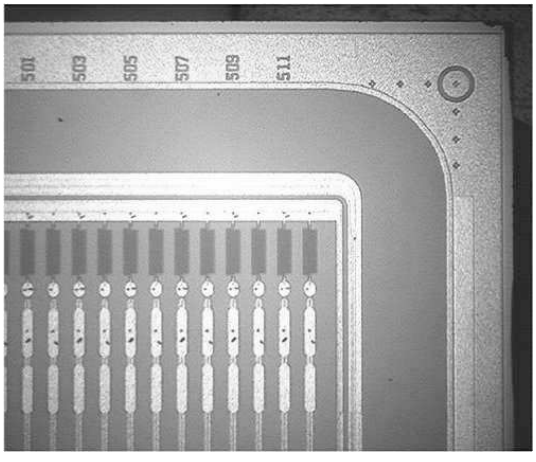

Figure 3: Picture of the corner of a typical sensor. The metal strips with large AC pads, the small DC-pad and the polysilicon resistors can be seen, surrounded by the bias and guard ring. The outermost Al-ring with the strip numbering and alignment markers is also visible.

1.2. Quality Assurance Scheme

The CMS tracker with its 200 m^2 of silicon consists of 24,244 single silicon sensors. Due to this large number, an elaborate quality assurance scheme is necessary to have continous information about the quality of the sensors during the long production period and to ensure that the detectors meet the required specifications. Additionally, very efficent logistics is necessary to track each sensor on its way between different test setups at various institutes and its final assembly and to get as much as possible information about the quality of a batch of sensors on a sample basis. The flow of the sensors from the manufactures to the module assembly centers is described now in detail and can also be seen in figure 4.

After receiving the sensors and registering each sensor id number in the tracker construction database at CERN they are shipped in equal percentage to the five 'Quality Test Centers' (QTC), which are responsible for the overall quality. These centers are located in Pisa, Perugia, Rochester, Karlsruhe and Vienna. A certain percentage will be distributed to the 'Irradiation Qualification Centers' (IQC), to the 'Process Quality Centers' (PQC) and to bonding centers for further tests [5].

Upon arrival at the QTC centers, 100 % of the delivered sensors are visually inspected using a microscope for mechanical defects like broken edges or scratches. During the pre-production phase, 100 % of the sensors have been electrically tested. After these sensors have been qualified, it is in the responsibility of the vendors to ensure that no change of the process or the

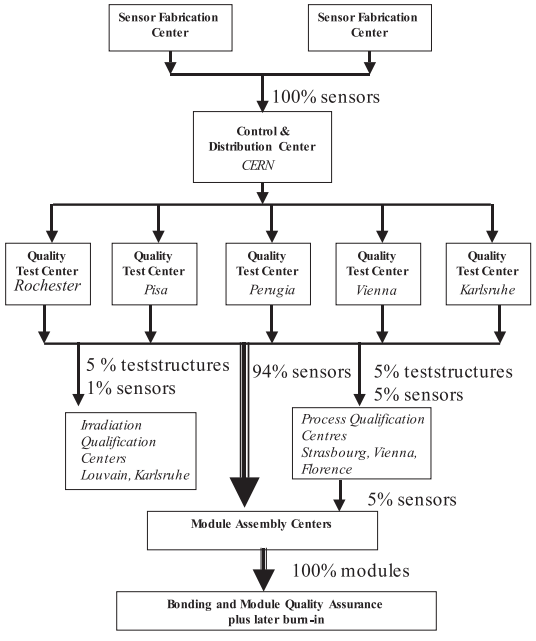

Figure 4: Logistics for the CMS Quality Assurance.

substrate properties occurs. During the full production phase, about 5 % of the sensors are electrically tested to verify the measurements done at the companies, while the manufacturing process is constantly monitored using standardized measurements on test structures in the 'Process Quality Centers' (PQC). In the following sections, the tests done at the QTC and PQC centers are described in detail.

2. QUALITY MONITORING ON SENSORS

2.1. Setup Description

The five QTC centers are equipped with different instruments and test benches. However, the measurement procedures and the output data format are identical. In this article the Vienna setup is explained in particular [6]. It consists of a vacuum support carrying the sensor, which is mounted on a XYZ-table. The micropositioner, which holds the needle for the bias ring connection, moves with the sensor support, while three further micropositioners with needles are stationary. This configuration allows a strip scan over all strips of the sensors with the possibility to contact an AC and two adjacent DC pads. The test bench ist controlled by a computer using the Labview measurement program and communicates with the instruments over the IEEE488 (GPIB) interface bus.

The electrical circuit of the probestation setup is designed for voltages up to 1000 V and currents in the range of few pA. Therefore, a good shielding and insulation of all components is essential. The test setup consists of a source measure unit (SMU) which is used to apply the reverse bias voltage to deplete the sensor. This is done in steps of 5 V up to 550 V. During the voltage ramp the IV curve is measured. Simultaneously the CV curve up to a voltage of 350 V is measured using a LCR meter. Typical diagrams for the CV and IV curves can be seen in figure 5. After

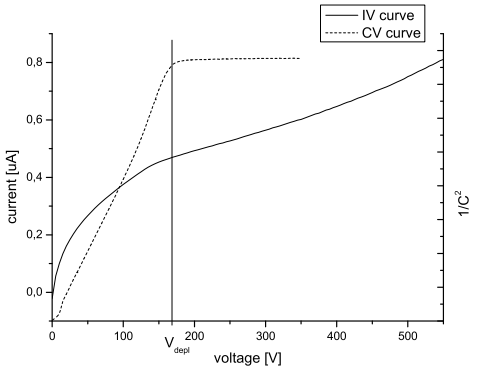

Figure 5: Typical IV (solid line) and $1/CV^2$ (dashed line) behavior of a silicon detector. The depletion voltage is around 170 V.

the bias voltage reached 550 V, the voltage is ramped to 400 V. At this voltage, the strip scan is performed. For that purpose the crosspoint switching matrix is reconfigured. Four parameters are measured for every strip: the single strip current (I_{strip}), coupling capacitance (C_{ac}) and dielectric current (I_{diel}) between AC and DC pad and the polysilicon resistor (R_{poly}). An example of a strip scan can be found in figure 6. After the strip scan is finished, the bias voltage is ramped down and an XML file with the results is uploaded into the tracker construction database.

2.2. Results

The acceptance criteria which must be fulfilled by each sensor are divided in three parts. First, the total number of bad strips (I_{strip} plus R_{poly} plus C_{AC} plus I_{diel}) must not exceed 1 %, which results in a cut of five bad strips for a sensor with 512 strips and seven bad strips for 768 strips, respectively. A strip is considered as bad if either the single strip leakage current I_{strip} exceeds 100 nA or the polysilicon resistor is below or above the limit of $1.0 < R_{poly} < 2.2\,\mathrm{M}\Omega$ or a pinhole is detected by either the coupling capacitance C_{AC} or the I_{diel} measurement.

For the overall performance of CMS it is necessary to keep the total number of bad strips at a low level to have a good spatial resolution in all regions of the tracker volume. The measurements done at QTC have been constantly compared to the measurement data provided by the companies. Since there is a very good

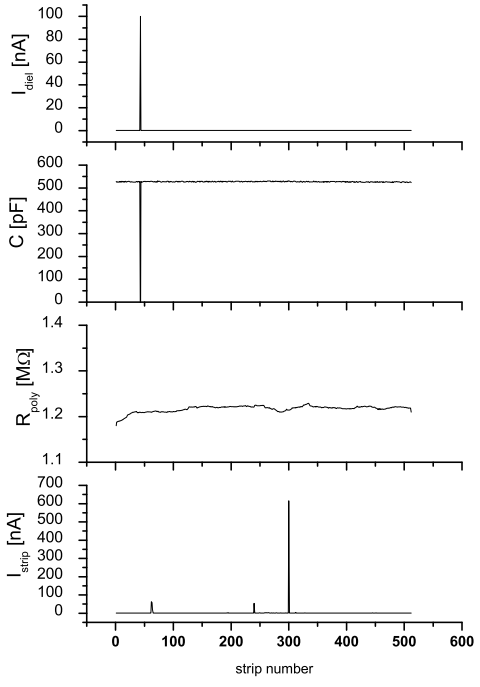

Figure 6: Example of a strip scan on a sensor with 512 strips. One pinhole at strip number 43 and one strip with high leakage current at strip number 300 can be seen.

agreement between HPK and our data for pinhole measurements, we treat both measurements equally. However, the total number of bad strips is more than the companies indicate. This is caused by the fact that the companies do not measure the single strip current and thus such strips are only identified at QTC level. In total, 17,778 HPK sensors have been accepted, by using both QTC and HPK data. For these sensors the average number of bad strips per sensors is 0.1 which is 0.018 % of the total number of strips. For STM, 2681 sensors have been tested by QTC, where we observed 1.91 bad strips per sensor which corresponds to 0.305 % failure rate. The distribution of the total number of bad strips per sensor can be seen in the figures 7 and 8 for HPK and STM sensors respectively.

The second criteria is the resistivity, which can be calculated using the depletion voltage. The thickness of wafers, the pitch and the ratio of width/pitch for the different types leads to a depletion voltage in the range from 100 to 300 V. Almost all of the tested sensors satisfy our requirements.

The third criteria is the dark current which must not exceed 5 μA at 300 V and 10 μA at 450 V. The average dark current at 450 V is 0.58 μA for HPK and 1.86 μA for STM sensors. Histograms of the distribution of the dark currents at 450 V can be found in figure 9 and 10 for both sensor types.

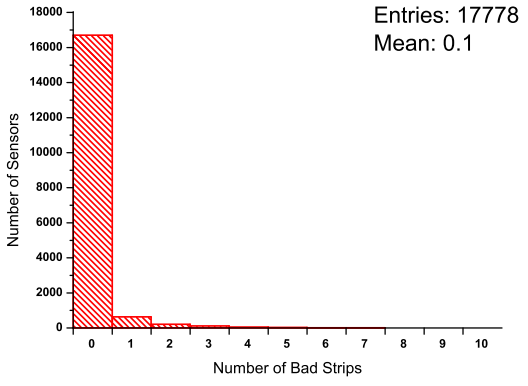

Figure 7: Distribution of the number of bad strips per HPK sensor.

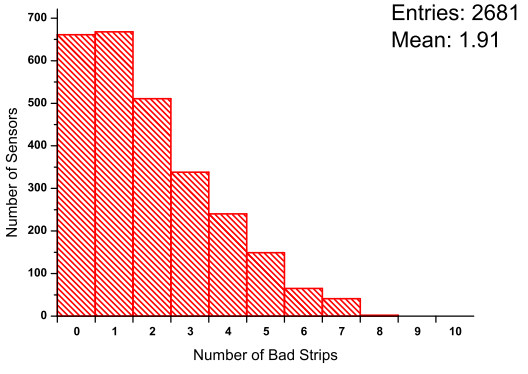

Figure 8: Distribution of the number of bad strips per STM sensor.

3. PROCESS MONITORING ON TESTSTRUCTURES

Each silicon wafer hosts additional devices beyond the sensor. These devices are placed around the rectangular sensor and are designed to monitor the stability of the manufacturing process [7]. A standard set of nine structures (called "Standard Half Moon") is used for the measurement of 11 different electric parameters with a fully automated setup The measured parameters are [8]

- bulk depletion voltage by measuring a C(V) curve on a diode
- bulk dark current at fixed Voltage by I(V) curve on a small replica of the main sensor called *baby sensor*
- coupling capacitance by using a LCR Meter on a dedicated structure called *TS-CAP* which is an array of strips directly connected to the bias ring.

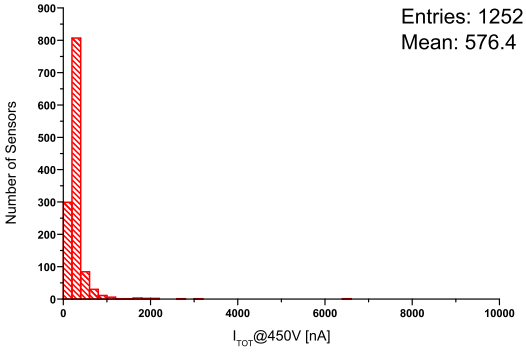

Figure 9: Histogram of the distribution dark current for HPK sensors at 450V.

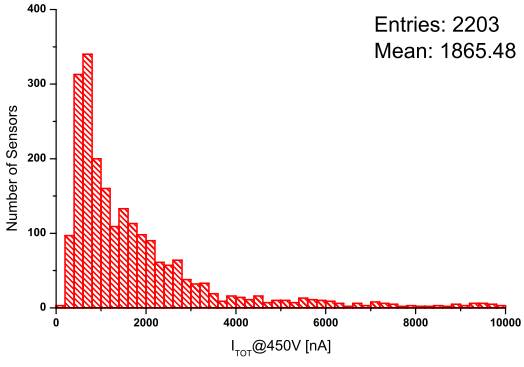

Figure 10: Histogram of the distribution dark current for STM sensors at 450V.

- breakdown voltage of dielectric layer by measuring a I(V) curve between aluminum and p^+ strips of TS-CAP structure
- interstrip resistance by I(V) curve on neighboring strips on a dedicated structure called *TS-CAP-DC*. This structure does not contain any polysilicon resistors which means that the DC strips are isolated from the bias ring.
- interstrip capacitance between central and two neighboring strips on *TS-CAP-AC* structure, which is an array of shorted strips around the three central strips which are used to measure the interstrip capacitance.
- aluminum layer resistivity by I(V) curve on a structure called *sheet* which incorporates an array of aluminum strips of different thicknesses.
- implant resistivity by I(V) curve on three p^+ strips of different thicknesses measured on the same structure.
- polysilicon resistivity by I(V) curve on three identical polysilicon resistors of sheet structure.
- flatband voltage by C(V) curve on a *MOS* (Metal-Oxide-Semiconductor) structure. This structure consists of the same dielectric layer as the thick intertrip layer of the main detector.
- surface current by I(V) curve on a gate controlled diode (*GCD* structure) which is built of comb-shaped p^+-strips intertwined with comb-shaped strips made of metal. While the p^+-strips act like a diode, the metal strips act like a MOS structure.

3.1. Setup Description

The setup is based on a probe card contacting all needed pads of the test structures with a set of 50 needles in parallel while the standard half moon is hold in place by a vacuum support in a light- tight box. The alignment procedure is done manually using a microscope and adjusting the probe card position using micrometer screws. A schematic picture of the setup can be seen in figure 11.

Each needle of the probe card is connected to an input channel of four multiplexer cards (Keithley K7154; 10 input channel each) plugged into a Keithley 7002 switching frame. The multiplexer outputs are interfaced through a 5x4 contacts matrix card (Keithley 7153) to the following instruments:

HV source measure unit (Keithley 237): Very precise source measure unit.

V source (Keithley 595 or Keithley 2410): Additional voltage source required for some of the measurements.

LCR meter (Agilent HP4285A): Capacitance measurement instrument using high frequency between 75 kHz and 30 MHz. In our measurements, we use a signal level of 100 mV. This instrument has an upstream decoupling box to allow a DC bias voltage beyond the instrument's limit of 40 V.

After the manual alignment of the probe card a computer running Labview performs all required steps to automatically measure the IV and CV curves on all structures and extracts the interesting parameters using linear fits. The computer is connected to the instruments via GPIB bus for control and data retrieval. After this procedure is finished an XML file with the results is uploaded into the tracker construction database. With this setup a single wafer can be characterized within 30 minutes.

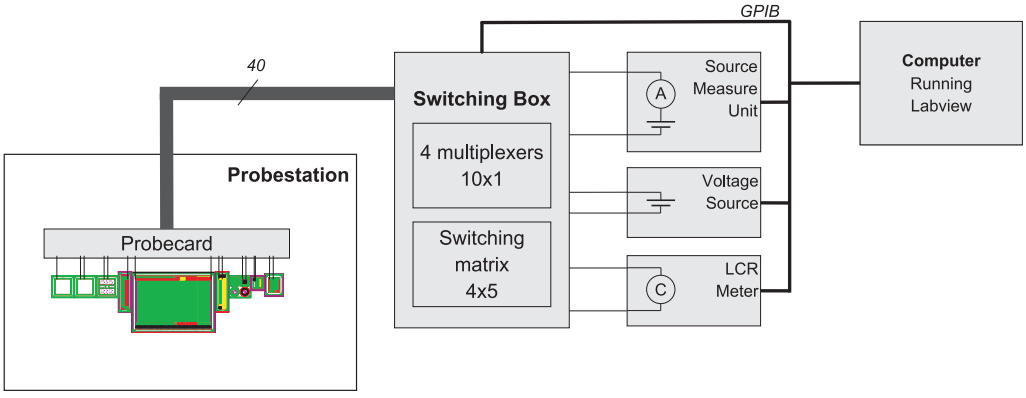

Figure 11: PQC Setup.

3.2. Measurements Examples

3.2.1. Diode

By measuring the capacitance versus voltage on a simple diode, the wafer thickness and the silicon resistivity can be determined. The silicon bulk is biased by a voltage between 0 and 300 V while the capacitance is measurement at steps of 5 V. Two linear fits are applied to the $1/C^2$ curve as a function of the applied voltage. In this view the curve rises constantly until it reaches a plateau and becomes a horizontal line. The full depletion voltage V_{depl} corresponds to the intersection of the two linear regions (see figure 12). The

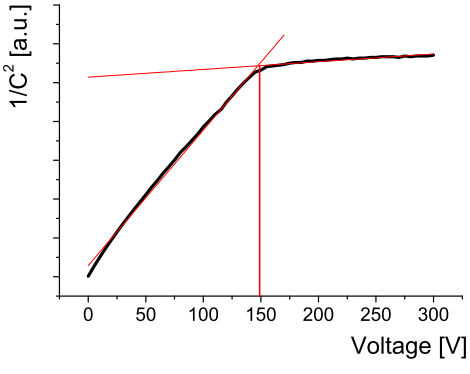

Figure 12: CV on a diode. The full depletion voltage $V_{depl} = 150\,\mathrm{V}$ is shown by a vertical line at the intersection point of the two linear regions of the curve.

bulk resistivity ρ of the silicon wafer can be calculated as

$$\rho = \frac{d^2_{\mathrm{nominal}}}{2\,\varepsilon_0\,\varepsilon_r\,\mu_e\,V_{depl}} \quad . \qquad (1)$$

3.2.2. MOS

One *metal oxide semiconductor* (MOS) structure is used to measure the flatband voltage V_{fb} through a CV plot. This MOS structure consists of the same oxide layer as the thick interstrip layer. This measurement shows how the interface mobility charge underneath the gate reacts to an applied voltage.

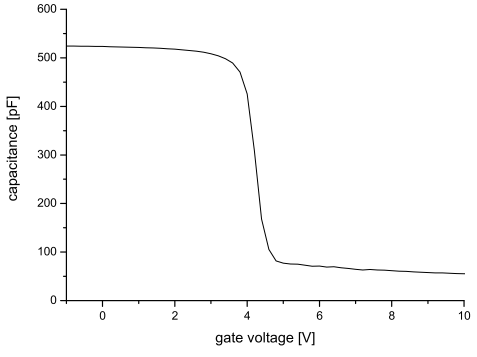

Figure 13: CV on MOS. The flatband voltage V_{fb} corresponds to the sharp drop of capacitance. In this example, this happens at $V_{fb} = 4.2\,\mathrm{V}$, while $C_{ox} = 524\,\mathrm{pF}$

Looking at the measured curve (see figure 13), we can identify three regions :

accumulation ($V_{gate} < V_{fb}$): free electrons are accumulated beneath the gate. The measured capacitance is the oxide capacitance C_{ox} only. Therefore, the oxide thickness can easily be extracted from this value.

depletion ($V_{gate} \approx V_{fb}$): increasing the voltage, the Si region underneath the gate depletes of free electrons. The capacitance decreases until the complete absence of charges in the silicon bulk. In a theoretical situation, this happens at 0 V. The shift of the flatband voltage measures the trapped positive charge in the oxide. This is the main parameter we are interested in.

inversion ($V_{gate} >> V_{fb}$): holes accumulate beneath the metal gate.

From the CV curve, two parameters are extracted by linear fits: V_{fb} and C_{ox}. With these values, we can calculate the oxide charge:

$$N_{ox} = \frac{C_{ox}}{q\ A_{gate}} \left(-0.5\,\mathrm{V} + V_{fb\_\mathrm{measured}}\right) \qquad (2)$$

3.3. Results

In total, 4500 standard half moons have been qualified at three different setups. Since the aim of these measurements is to monitor the stability of the manufacturing process, the results are usually plotted as the parameter versus the date of the measurement. Since we are always testing sensors which were produced very recently, we are able to quickly see any changes and can efficiently intervene at the producers.

In the plots below two parameters are presented in this way as examples for all the others. In the first (figure 14) the interstrip resistance is shown. There

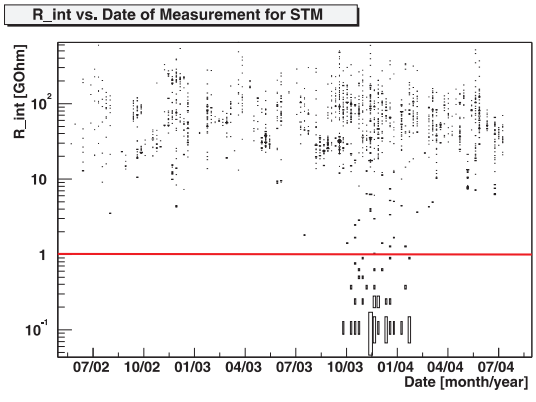

Figure 14: R_{int} vs. time. The lower limit of 1 GΩ is represented by the horizontal red line.

is a lower limit of 1 GΩ which is represented by the horizontal red line. One can see clearly that many sensors in a very narrow time period are below this limit. This issue was reported to STM as a possible passivation problem and was addressed by the company for later deliveries. However, around one thousand sensors which suffer from this problem have been rejected.

The second plot (figure 15) shows the flatband voltage as described in the last section versus time. The upper limit of 7 V is again marked with a horizontal red line. We observed constantly some batches between good ones where the results exceeded this value. These production batches have been rejected and this issue has been reported to the company, which admitted that some contamination of the production line occurred. This happened again and again up to the date where we observed the issue with the very low interstrip resistance. After that date the values were well below the limit. However, the measurements helped to avoid to use sensors for CMS which would not have survived the harsh radiation environment.

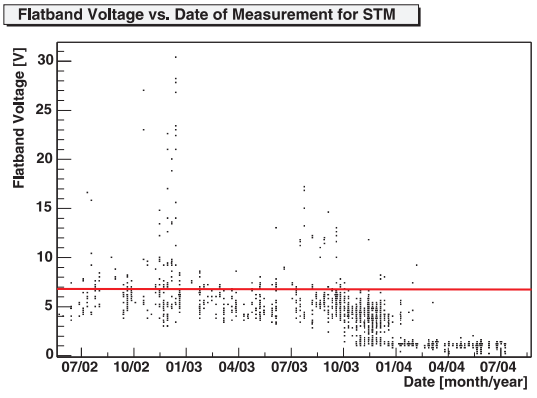

Figure 15: $V_{flatband}$ vs. time. The upper limit of 7 V is represented by the horizontal red line.

4. SUMMARY

The huge amount of silicon sensors needed for the CMS tracker has shown different problems which were not present in the past when experiments used very small tracker volumes and the silicon sensors covered only very small areas. Nowadays, the production of silicon sensors is in mass production at the manufacturers and an elaborate quality assurance at both the manufacturers and the involved scientific community is mandatory. Since it is not possible anymore to test every single strip on 100 % of the sensors it is necessary to trust the data of the companies. For the CMS silicon sensor quality it was very helpful to constantly monitor the production process of the companies using dedicated devices apart from the main detector. Without that, many sensors would have been accepted and used for the CMS tracker which would not survive the planned 10 years of operation. When even larger experiments than CMS will be built in the future the effort, costs and complexity of the quality assurance of the silicon sensors must not be underestimated.

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