CMOS MAPS with Fully Integrated, Hybrid-pixel-like Analog Front-end Electronics

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This paper discusses the criteria underlying the design of an innovative type of monolithic active pixel sensor (MAPS) in CMOS technology. The device was conceived to incorporate the potential for thin detector fabrication typical of MAPS devices and the flexibility and high functional density featured by hybrid pixel sensors. The detector layout takes advantage of the large miniaturization scale of deep submicron CMOS technologies and of the triple-well structure they offer. A proof-of-principle test chip, named Apsel0, has been thoroughly characterized, with promising results. Based on the outcomes of this first step, a second prototype was designed, paying particular attention to the noise performances of the front-end electronics. In this work, the experimental characterization of the Apsel0 chip, including data from radioactive source (^{90}Sr, ^{55}Fe) tests, will be presented. Also preliminary results from the just started measurement campaign on the second prototype, Apsel1, will be shown and discussed.

1. INTRODUCTION

In recent years, the attention of several groups in the particle physics community has been drawn to monolithic active pixel sensors (MAPS) in CMOS technology as promising candidates for charged particle tracking at the future high luminosity colliders. The success of MAPS, which were developed chiefly for imaging applications, is built on the flexibility and on the "system-on-chip" features provided by CMOS processes [1]. Their working principle, based on the diffusion of minority carriers in a lightly doped, thin epitaxial layer, might be exploited in the fabrication of highly granular, light detectors possibly satisfying the resolution constraints set by next generation experiments at the International Linear Collider and at the Super B-Factory. In such applications, CMOS MAPS could also benefit from the high degree of radiation hardness featured by deep submicron technology nodes, at least as far as the analog processing circuits are concerned [2, 3]. The extremely simple three N-type transistor (3T) scheme and the sequential readout techniques which are generally used for signal processing in imaging MAPS devices could hardly be considered suitable for treating the fast data rates foreseen at the mentioned high luminosity colliders, nor are they compatible with high speed readout of large area detectors. Several solutions have been proposed to adapt such a scheme to the specifications of the future particle accelerator experiments [4–7]. A more complex, hybrid-pixel-like processor implemented at the elementary cell level might be used to perform data sparsification and provide the needed flexibility to deal with possible increases in the accelerator luminosity throughout the experiment lifespan.
In this work, the large scale of integration and the triple-well feature of deep submicron CMOS processes have been exploited to develop an integrated sensor featuring high functional density in the elementary cell and with the potential for thin detector fabrication, therefore incorporating the main characteristics of hybrid pixels and standard MAPS in a monolithic crystal. Since an N-well with a deep junction is used as the collecting electrode, the proposed device will be called deep N-well monolithic active pixel sensor (DNW-MAPS). The main features of such a detector will be highlighted in the following section. Experimental results from the tests of two prototype chips implementing the deep N-well sensor concept will then be presented and discussed.

2. THE DEEP N-WELL MAPS CONCEPT

In standard CMOS MAPS, use of PMOS devices in the design of the front-end electronics is avoided as the N-well they are integrated in might subtract charge to the collecting electrode leading to potentially serious efficiency loss. The lack of complementary devices represents a significant limitation to the design

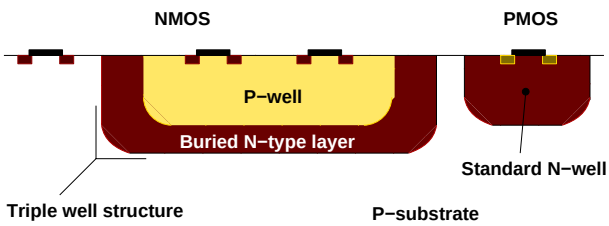

Figure 1: cross-sectional view of a CMOS process including a triple-well structure.

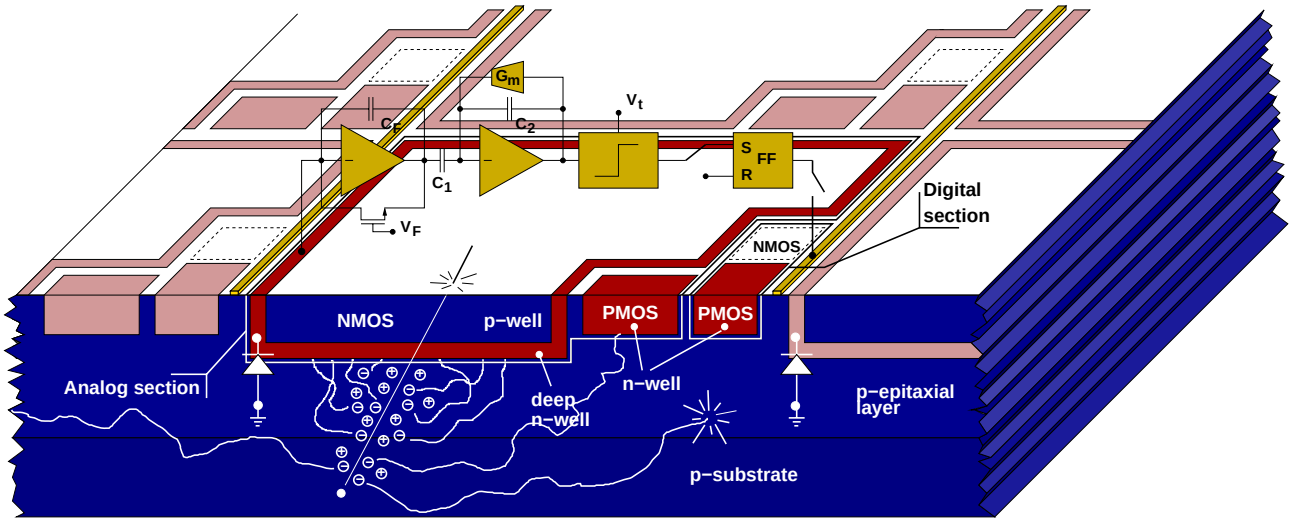

Figure 2: conceptual three dimensional view of a deep N-well MAPS in CMOS technology. The block diagram of the readout channel is also displayed.

of gain stages with satisfactory properties, thereby restricting the set of available readout solutions. In the deep N-well MAPS discussed in this paper, the problem has been circumvented by using a buried N-type layer to design a comparatively larger electrode than it is found in common CMOS sensors. Such a layer is part of a triple-well structure (sketched in Fig. 1) which has been introduced in modern CMOS technologies to shield N-type transistors performing analog functions from substrate coupled switching noise in mixed-signal circuits. If the dimensions of the collecting electrode are chosen to be sufficiently large, N-type wells can be allowed in the vicinity with no significant degradation of the collection efficiency. Therefore, P-channel MOSFETs can be included in the design of high performance amplifiers and logic blocks, implementing more sophisticated functions in the elementary cell than in the case of classical imaging MAPS. In the case of the DNW-MAPS, the choice was made to process the charge signal by means of a classical readout chain for capacitive detectors, including a charge preamplifier and a shaping filter. Binary information is provided by a threshold discriminator and then stored into a latch. As compared to standard MAPS, where the output voltage is proportional to the collected charge through the reciprocal of the sensor parasitic capacitance, employing a charge preamplifier as the front-end stage decouples the charge sensitivity from the capacitance of the sensitive element and, as a consequence, from its area. Moreover, the deep N-well structure acting as the collecting electrode may embed NMOS devices belonging to the processor analog section, therefore minimizing the impact of the front-end electronics on the pixel fill-factor, defined as the sensitive area over the total elementary cell area. Fig. 2 summarizes the layout characteristics of the deep N-well sensor, as they were described in this section. The analog and the digital sections of the readout processor are separated from each other, in order to minimize cross talk issues. The two standard N-wells where PMOS devices are integrated cover a small fraction of the total elementary cell surface. From the above considerations it is quite obvious that keeping the number and size of PMOS transistors to a minimum is supposed to improve the charge collection properties of the sensor. Fig. 2 also shows the schematic diagram of the front-end electronics monolithically integrated at the pixel level, which is described in more detail in the next paragraphs.

3. FRONT-END ELECTRONICS DESCRIPTION

As already mentioned, the processing chain of the DNW-MAPS includes a charge preamplifier, a semigaussian unipolar shaper of the first order, a discriminator and a NOR latch. In the charge preamplifier, high charge sensitivity was achieved by using, in the preamplifier feedback network, a MOS capacitor (C_F=8 fF), which made it possible to overcome the 30 fF limit set by the process design rules for MIM (metal-insulator-metal) capacitors. Continuous charge reset is performed through a subthreshold operated NMOSFET. The block following the preamplifier is a first order, semigaussian unipolar (RC-CR) shaping filter with programmable peaking time t_p, which can be selected among three different values, 0.5, 1 and 2 μs. These relatively long t_p values were chosen with the aim of avoiding ballistic deficit in the case of long collection times. The feedback network of the shaper, shown in the block diagram of Fig. 2, includes the MIM capacitances C_1 and C_2 and the

transconductor G_m. The signal at the shaper output is compared to an externally preset threshold voltage by means of a discriminator, featuring dynamical hysteresis to avoid noise induced multiple threshold crossings. A NOR latch is used to store the information bit at the comparator output and can be reset once the bit has been readout.

4. THE Apsel0 CHIP

The features discussed in section 2 were implemented for the first time in the Apsel0 prototype, whose characterization was carried out in the second quarter of 2005. The Apsel0 test chip was fabricated in a 130 nm triple-well, epitaxial CMOS process provided by STMicroelectronics. It includes six single pixel test structures, which differ from each other in the area of the deep N-well layer acting as the collecting electrode. Some of the structures were provided with a calibration capacitance at the preamplifier input, which made it possible to test the readout channel directly by charge injection. A detailed description of their features has been given in a previous paper [8]. The purpose of this first prototype was to demonstrate the feasibility of the DNW-MAPS sensor and its capability to detect ionizing radiation. The availability of single cells with different sensor area was meant to help study charge collection and signal-to-noise properties of the device. In the Apsel0 chip, the forward block of the preamplifier is a cascode stage with a cascode load. In the input NMOS element, the channel width W, 3 μm, and length L, 0.35 μm, were optimized for a detector capacitance of 100 fF and a drain current of 1 μA. Since the device is operated in moderate inversion, classical capacitive matching criteria, which apply to transistors working in the strong inversion regime, could not be used. Therefore optimal dimensions were determined through parametric circuit simulations. Finally, according to simulations, in the Apsel0 chip, the power dissipated by the analog section of the readout channel (charge preamplifier and shaper) and the threshold discriminator is about 10 μW.

4.1. Front-end electronics characterization

Among the test structures available in the Apsel0 chip, those (called ch1, ch2 and ch5) provided with a calibration capacitance (C_{inj}=30 fF) at the preamplifier input could be tested through charge injection from an external pulser. The other single cells were characterized by means of radioactive sources (the relevant results are discussed in the next section). Measurements in Fig. 3 refer to a test structure

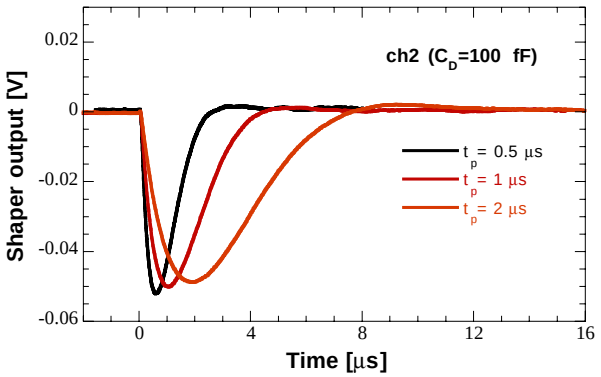

Figure 3: signal at the shaper output in the readout channel of the ch2 test structure at the three different peaking times (detector simulating capacitance C_D=100 fF, injected charge Q_{inj}=560 electrons).

(ch2) where a 100 fF MIM capacitor was connected to the preamplifier input to simulate the detector capacitance. The figure shows the shaper response to an injected charge of 560 electrons at the three different peaking times. The readout electronics, which was laid out according to the criteria discussed in section 2, was not connected to the deep N-well sensor in this case.

In table I, the charge sensitivity is displayed for all of the three channels with the calibration capacitance at the preamplifier input, again at the three available peaking times. In the ch5 pixel structure, the charge preamplifier was connected to the relevant deep N-well sensor (featuring a 270 fF capacitance) to form a DNW-MAPS. No electrical connection to the collecting electrode was laid out instead in the case of ch2, as already explained, nor in the case of ch1, which consists of the bare readout channel. Nevertheless, for both of them, the NMOS devices belonging to the analog section were integrated in a deep N-well covering the same area (830 μm^2) as in the ch5 single pixel. The significant change in the charge sensitivity featured by ch5 is to be blamed on the small loop gain in the preamplifier, which was designed to pro-

Table I : charge sensitivity [mV/fC] at the three available peaking times for the structures with integrated calibration capacitance.

	$t_p = 0.5$ μs	$t_p = 1$ μs	$t_p = 2$ μs
ch1 (C_D =0)	610	590	530
ch2 (C_D =100 fF)	580	550	520
ch5 (C_D =270 fF)	460	450	430

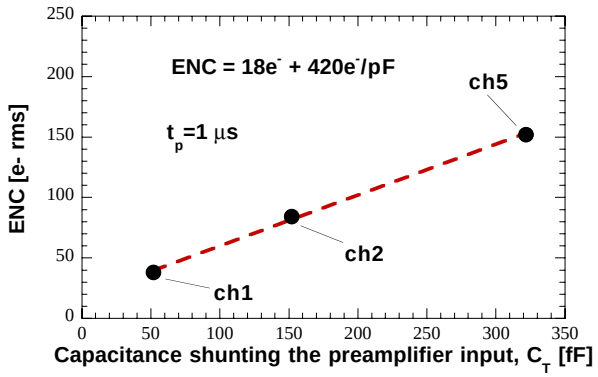

Figure 4: equivalent noise charge as a function of the total capacitance C_T shunting the charge preamplifier input.

cess signals from a 100 fF detector. The design value turned out to be about a factor of three smaller than the actual sensor parasitic capacitance, which could be measured on a set of test structures (including, among others, DNW/epitaxial-layer and DNW/P-well junctions) fabricated together with the Apsel0 chip. This flaw in the preamplifier performances could be easily reproduced in post layout simulations (PLS), once the above mentioned test structures were characterized and the deep N-well sensor capacitance was measured.

The equivalent noise charge (ENC) at a peaking time of 1 μs is shown in Fig. 4 as a function of the total capacitance C_T shunting the charge preamplifier input. C_T includes the calibration capacitance C_{inj}=30 fF, the feedback capacitance C_F=8 fF, the preamplifier input capacitance C_{in}, about 10 fF, and the detector capacitance C_D, whose value is shown in table I for each of the three considered structures. The ENC grows linearly with C_T, as predicted by the theoretical equation

$$ENC = C_T \sqrt{S_W \frac{A_1}{t_p} + A_2 A_f}. \qquad (1)$$

In (1), S_W is the power spectral density of the series noise in the preamplifier input device (virtually corresponding to its channel thermal noise) and A_f is the power coefficient of the 1/f noise, while A_1 and A_2 are shaping coefficients, with the following expressions:

$$A_1 = \frac{1}{2\pi} \int_0^{+\infty} \frac{x^2}{(1+x^2)^2} dx, \qquad (2)$$

$$A_2 = \int_0^{+\infty} \frac{x}{(1+x^2)^2} dx. \qquad (3)$$

The second term under the square root in (1) seems to dominate the equivalent noise charge, as no significant variations were detected with varying t_p. Predominance of the flicker noise term is most likely due to the small channel dimensions of the preamplifier input element and to the relatively long peaking times. In Fig. 4, the equivalent noise charge for ch5 is 150 electrons. A slightly smaller value, about 140 electrons, extracted from the interpolating straight line, should be expected if C_{inj}, which is not part of the actual readout channel, were not present. This value is nevertheless significantly larger than the noise figure obtained from circuit simulations, about 50 electrons. As in the case of the charge sensitivity issue, this discrepancy is due to the fact that the sensor parasitic capacitance was underestimated during the design phase.

4.2. Tests with radioactive sources

An ^{55}Fe source was used to calibrate noise and charge sensitivity in the pixels which were not provided with the injection capacitance, namely ch3, ch4 and ch6, with sensors respectively 1730 μm^2, 2670 μm^2 and 830 μm^2 in area. Such tests were also intended to further substantiate data from readout electronics simulation and characterization. Amplitude of the signals at the shaper output was measured by means of a digital oscilloscope.

^{55}Fe X-ray interaction with silicon is dominated by the photoelectric effect, through which the photon energy is entirely released in the detector. Fig. 5 shows the response of the ch6 DNW-MAPS at t_p=2 μs to X-rays from an ^{55}Fe source (red histogram) together with noise hit measurements (blue histogram). Note that ch6 is identical to ch5, (except for the calibration capacitance C_{inj}), which makes it possible to directly compare data from section 4.1 to the results discussed below. Photons from the ^{55}Fe 5.9 keV line generate about 1640 electron/hole pairs each. When photons

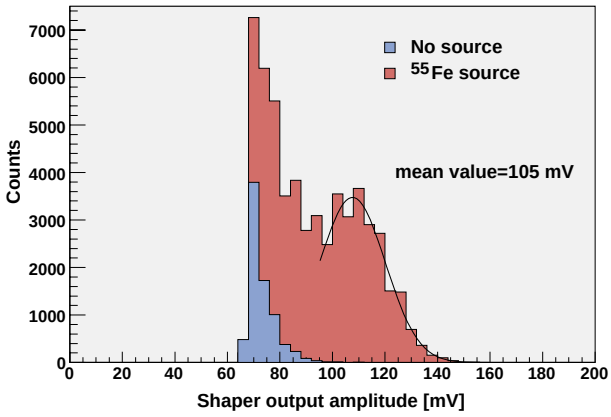

Figure 5: signal amplitude distribution for X-rays from a ^{55}Fe source (red histogram) compared to noise hit measurements (blue histogram).

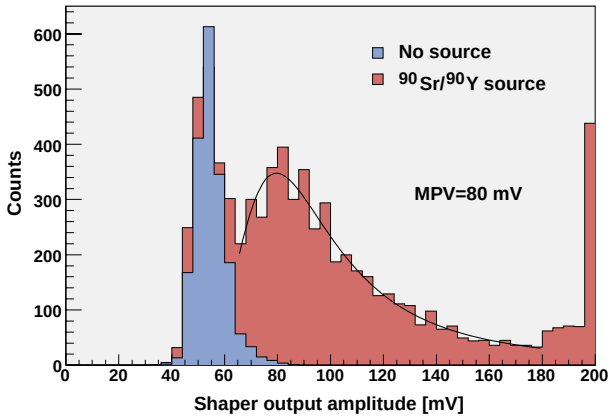

Figure 6: signal amplitude distribution for electrons from a ^{90}Sr/^{90}Y source (red histogram) compared to noise hit measurements (blue histogram).

convert nearby the collecting electrode, the released charge is virtually entirely collected, yielding the distribution emphasized, in Fig. 5, by means of the interpolating Gaussian curve (black line). The mean value, about 105 mV, corresponds to a charge sensitivity of about 400 mV/fC, within 10% of the readout electronics test and simulation results (430 mV/fC). Based on the ^{55}Fe calibration data, equivalent noise charge was found to be about 125 electrons, fairly close to ch5 ENC measurements (140 electrons). Events in significant excess of the noise counts were detected towards low shaper output amplitudes, which are likely to result from charge released far from the collecting electrode and only partially collected, therefore delivering a smaller signal. During tests, the acquisition rate was kept compatible with the oscilloscope specifications by cutting all the events producing pulses with heights below 70 mV.

The behavior of the same single pixel structure with respect to charged particles was investigated by means of a ^{90}Sr/^{90}Y source. Electrons released by such a source through beta decays ($^{90}_{38}\mathrm{Sr} \rightarrow {}^{90}_{39}\mathrm{Y} + \mathrm{e}^- + \overline{\nu}$ and $^{90}_{39}\mathrm{Y} \rightarrow {}^{90}_{40}\mathrm{Zr} + \mathrm{e}^- + \overline{\nu}$) feature a broad, continuous energy spectrum, extending up to 2.27 MeV. In the acquisition system which was employed for collecting the data displayed in Fig. 6, measurement of the waveform amplitude at the shaper output was triggered by the coincidence between the signal from a scintillator and the output of the latch at the end of the MAPS readout chain. In order to keep the acquisition rate inside the scope bandwidth, the comparator threshold was set so as to reject pulses below 40 mV. Based on the spectral characteristics of the ^{90}Sr/^{90}Y, about 45% of the particles have minimum ionizing energy and produce the distinct Landau shaped distribution of Fig. 6 (red histogram), with a most probable value (MPV) of 80 mV. The corresponding collected charge, 1250 electrons, and signal-to-noise ratio, 10, can be obtained by taking into account the ^{55}Fe calibration data of section 4.2. Particles at smaller than MIP (minimum ionizing particle) energy release a larger amount of charge, deforming the distribution shape at amplitudes exceeding 180 mV and even saturating the shaper output signal.

5. THE Apsel1 CHIP: PRELIMINARY RESULTS

The Apsel1 chip was submitted in August 2005 and delivered in January 2006. The second prototype includes five single pixel cells, all provided with a 60 fF injection capacitance. One of them consists of the standalone readout circuit (ROC) not connected to the DNW sensor, while the other four are DNW-MAPS with different sensor area. In the prototype, an 8 by 8 pixel matrix was also integrated, capable of generating a trigger signal as the wired OR of all of the latch outputs and featuring a row by row, 8-line parallel readout. In the design of the front-end electronics for the new prototype, the noise and gain issues raised by the Apsel0 chip were addressed by implementing a folded cascode circuit with active load stage in the charge preamplifier. Moreover, the input NMOS transistor dimensions, W/L=16/0.25, were optimized for a sensor parasitic capacitance C_D of 460 fF. The estimation of C_D was based on the model parameters provided by the manufacturer, which proved to be in good agreement with the characterization results of the pn junction structures mentioned in section 4.1. The drain current in the input element was set to 30 μA so as to improve significantly the front-end noise performances. Simulations predicted a power

Table II : description of the single cell structures in the Apsel1 chip.

Cell name	Description
channel 1	sensor area=900 μm^2 (reference pixel, same layout as the matrix pixels), C_D=460 fF
channel 2	sensor area=1000 μm^2 (N-well extension), C_D=470 fF
channel 3	sensor area=2000 μm^2 (N-well extension), C_D=610 fF
channel 4	preamplifier input not connected to the DNW sensor, C_D=0
channel 5	sensor area=900 μm^2 (same as channel 1, with shaper MIM capacitors laid over the readout electronics), C_D=460 fF

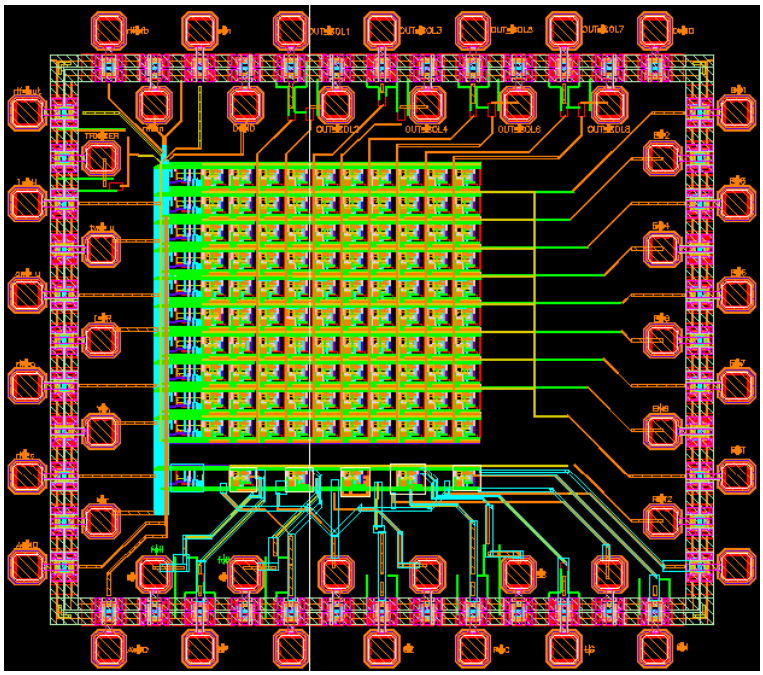

Figure 7: layout of the Apsel1 prototype. The chip size is about 1.3 mm × 1.2 mm.

dissipation of about 60 µW per channel. With the exception of the just mentioned changes in the charge preamplifier, no modifications were made to the readout electronics with respect to the Apsel0 prototype. The experimental results presented in this section are relevant to the five single pixel cells, which are described in table II. Some of the structures were conceived to study particular design solutions. In the case of channel 2 and channel 3, the DNW collecting electrode area was extended by merging with standard N-well diffusions along its contour. The layout of the chip is shown in Fig. 7. The five test structures are located at the chip bottom, below the sensor matrix (which actually contains 10×10 elements, the outmost ring consisting of dummy cells). The circuits are serviced by 48 bonding pads, supplying power and signals to the chip and delivering analog and digital signals to the outer world. A simplified cross-sectional view of the single pixel structure with standard N-well extension is shown in Fig. 8, where specific parasitic capacitances between the DNW and the internal P-well (C_{dnpw}) and between the N-well (and the DNW) and the P-type epitaxial layer (C_{nwpe}) are emphasized. Since C_{nwpe} is about a factor of seven smaller than C_{dnpw}, using the N-well layer to increase the sensor area might improve its performances (e.g. by improving its charge collection properties) with less significant impact on the noise performances than in the case of directly extending the DNW area. Fig. 9 shows the signal at the shaper output of the channel 1 DNW-MAPS as a response to an injected charge of 750 electrons. The waveforms were acquired at the

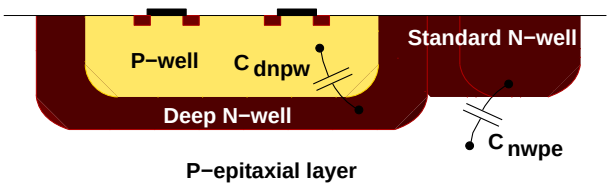

Figure 8: increasing the collecting electrode area by means of standard N-well extensions.

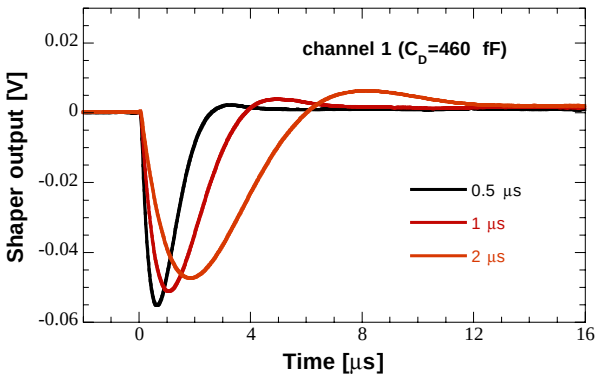

Figure 9: signal at the shaper output of the channel 1 DNW-MAPS at the three different peaking times (detector capacitance C_D=460 fF, injected charge Q_{inj}=750 electrons).

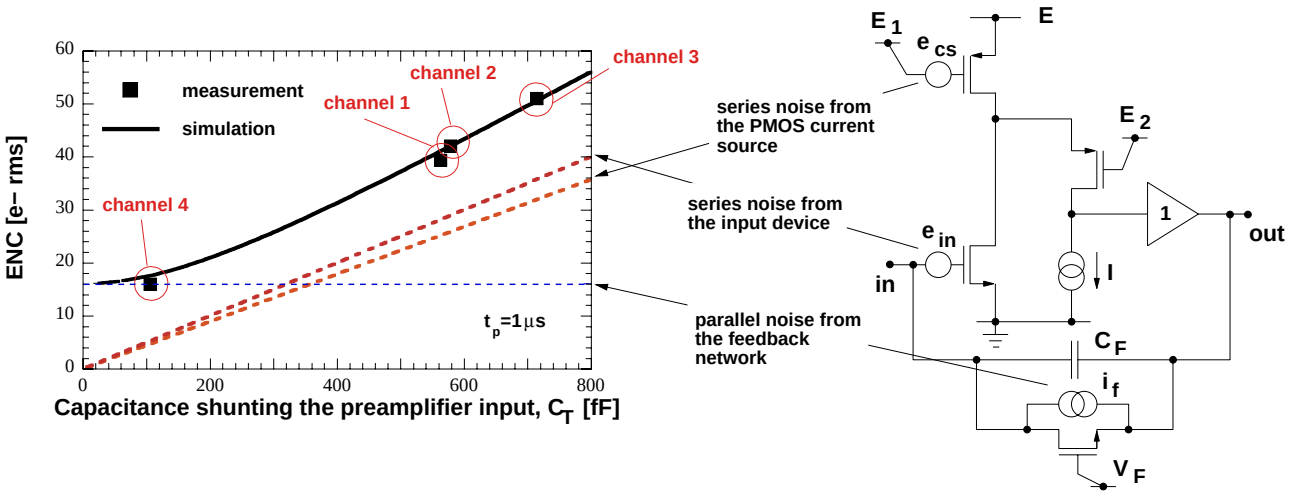

Figure 10: equivalent noise charge as a function of the capacitance shunting the preamplifier input terminal, C_T. Measurement data are compared to simulation results. Noise contributions to the total ENC are specified in a simplified schematic representation of the preamplifier.

three available peaking times. A slight overshoot can be observed, caused by a residual parasitic capacitance between the preamplifier input and the shaper output terminal. The equivalent noise charge and the charge sensitivity, measured for the same device, is shown in table III. ENC was found to be about 40 electrons, irrespective of the peaking time, in good agreement with post layout simulations. Based on the ^{90}Sr test results discussed in section 4.2, where a collected charge of 1250 electrons was found, the most probable signal-to-noise ratio should be slightly larger than 30. The availability of test structures with different detector capacitances could be exploited to measure the ENC slope with varying peaking time. The measurement result, about 70 e$^-$/pF, is displayed in table IV and, again, does not feature any dependence on t_p.

Table III : ENC and charge sensitivity for the single cell DNW-MAPS with the same layout as the matrix pixels (channel 1, C_D=460 fF).

Peaking time [µs]	ENC [e$^-$ rms]	Charge sensitivity [mV/fC]
0.5	41	466
1	39	432
2	39	406

Table IV : ENC slope at the three different peaking times.

Peaking time [µs]	$\frac{dENC}{dC_D}$ [e$^-$/pF]
0.5	70
1	68
2	68

The equivalent noise charge as a function of the total capacitance C_T shunting the charge preamplifier input is shown in Fig. 10 for a peaking time of 1 µs. As in the case of Fig. 4, C_T is the sum of the MIM calibration capacitance C_{inj} (60 fF), the feedback MOS capacitance C_F (unchanged, 8 fF), the preamplifier input capacitance C_{in} (about 40 fF) and the sensor parasitic capacitance C_D (see table II). In Fig 10, the measurement results are compared to the simulation data. The main noise contributions are represented by the voltage sources e_{in} and e_{cs} and by the current source i_f in a simplified schematic of the charge preamplifier. The good agreement between simulation and experimental results demonstrates that the noise parameters provided by the STMicroelectronics design kit are quite accurate. As shown in the ENC plot, the series noise in the preamplifier input device alone cannot account for the noise performances of the readout circuit. In this case the equivalent noise charge equation is actually more complicated than (1) and is given by (4) where symbols have the following meanings:

- $S_{w,in}$ is the power spectral density of the series white noise and $A_{f,in}$ is the power coefficient of the series 1/f noise in the preamplifier input element;

- $S_{w,cs}$ is the power spectral density of the series white noise and $A_{f,cs}$ is the power coefficient of the series 1/f noise in the PMOS current source;

- $S_{w,f}$ is the power spectral density of the parallel white noise and $A_{f,f}$ is the power coefficient of the parallel 1/f noise in the feedback MOSFET;

$$ENC = \left\{ C_T^2 \left[A_1 \frac{S_{w,in} + S_{w,cs}\frac{g_{m,cs}^2}{g_{m,in}^2}}{t_p} + A_2 \left(A_{f,in} + A_{f,cs}\frac{g_{m,cs}^2}{g_{m,in}^2} \right) \right] + A_3 S_{w,f} t_p + A_4(t_p) A_{f,f} R_F^2 \right\}^{1/2} \quad (4)$$

- $g_{m,in}$ and $g_{m,cs}$ are the channel transconductances of the preamplifier input element and of the PMOS current source;
- R_F is the equivalent resistance provided by the MOSFET in the preamplifier feedback network;
- A_3 and $A_4(t_p)$ are shaping coefficients featuring the following expressions:

$$A_3 = \frac{1}{2\pi} \int_0^{+\infty} \frac{1}{(1+x^2)^2} dx, \quad (5)$$

$$A_4(t_p) = \int_0^{+\infty} \frac{x}{\left(1 + x^2 \frac{\tau_F^2}{t_p^2}\right)(1+x^2)^2} dx. \quad (6)$$

Expressions for A_1 and A_2 are provided by (2) and (3). In (6), $\tau_F = R_F C_F$. As shown by (4), at large detector capacitances the ENC is dominated by the series noise contributions from the preamplifier input device and from the PMOS biasing the input element itself. At small C_D values, the parallel contributions from the NMOSFET in the feedback network, which are independent of C_D, prevail. For C_D=460 fF (corresponding to C_T=570 fF), which is the sensor capacitance featured by the matrix pixels, the parallel term is responsible for about 5% of the total ENC.

6. CONCLUSION

In this paper, a novel kind of CMOS monolithic active pixel sensor, called the deep N-well (DNW) MAPS, has been presented and described. The proposed MAPS takes advantage of the deep N-well structure available in deep submicron CMOS processes to collect the charge released in the epitaxial layer and to increase the complexity and the functional density of the readout electronics integrated at the pixel level. The charge signal is processed by means of a standard front-end circuit for capacitive detectors, therefore decoupling the charge sensitivity from the detector capacitance. Measurements performed on the first DNW-MAPS prototype, Apsel0, demonstrated that the device is capable to detect ionizing radiation. The preliminary characterization of the second prototype, Apsel1, indicates that the gain and noise issues raised by the Apsel0 chip have been correctly addressed. Future tests on the small pixel matrix available in the Apsel1 chip are expected to provide information about the sensor cluster size. These first steps should be intended as a proof of feasibility for the proposed monolithic sensor. In view of the application to future experiments at the next generation colliders, several solutions are being investigated in order to make the device compliant with the foreseen spatial resolution constraints. They might involve using more scaled CMOS technologies and/or simplifying the front-end electronics by removing the shaper from the processing chain. Another quite important issue, that of power dissipation, will be addressed in future designs by implementing power cycling techniques, which could be exploited in accelerating machines of the International Linear Collider kind.

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