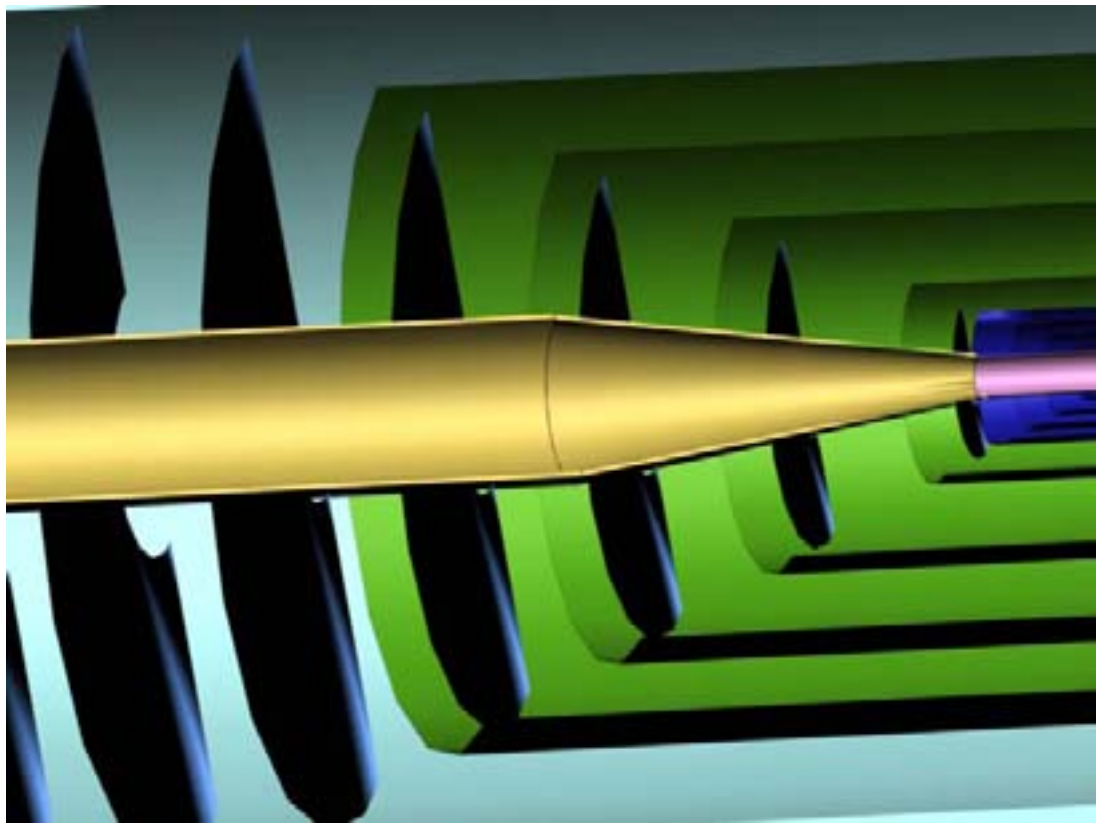
Review of Silicon Inner Tracker



H.J.Kim (KyungPook National U.)

Talk Outline

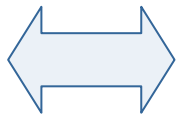
- Configuration optimization of BIT and FIT
- Silicon Sensor R&D
- Electronics R&D
- Summary and Plan

Detail study will be presented by E.Won

1) "A Simulation Study of Silicon IT for GLD", Tues 1:30pm
2) "Status of DSSD R&D for Inner Tracking", Thurs. 1:30-1:50

IT Collaboration for GLD

Kyungpook/
Seoul Nat. Univ.



Korea/
Chonnam Univ.

- Configuration optimization
- mask design
- DSSD simulation
- Sensor characterization
- Radiation damage study

- Configuration study
- hybrid development
- Readout Electronics

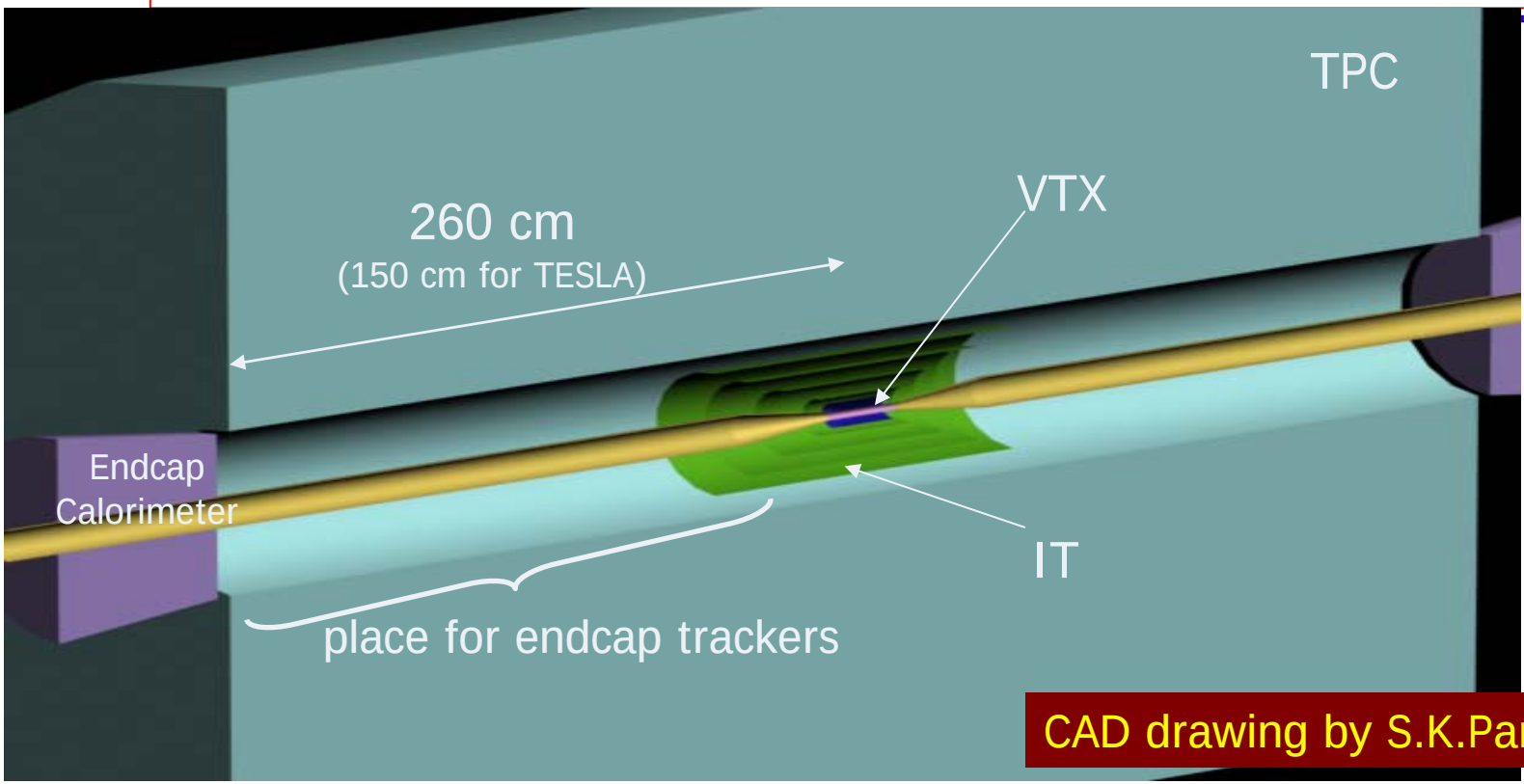
4 faculty members and 7 graduate students.
(Not all are in full time)

Configuration

- Barrel Inner Tracker design optimization
- Forward Inner Tracker baseline design

- Endcap Silicon Tracker between TPC and CAL
- Background study
- Single side vs Double side SD
- IT Optimization for physics improvement

GLD Geometry (vertex and tracking only)

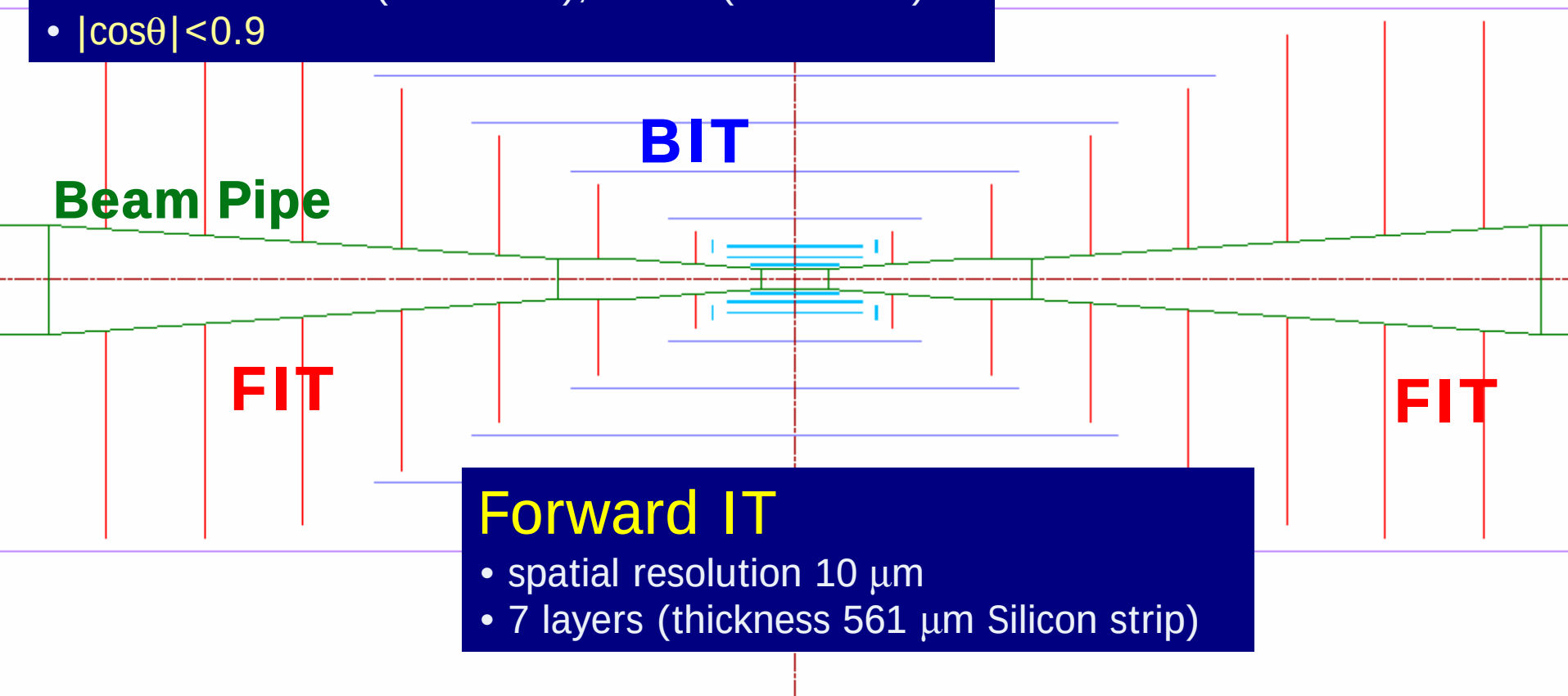


items	ACFA8	snowmass
barrel IT	4 layers	4 layers
forward IT	did not exist	7 layers
software	“gld v1”	various updates

Barrel/Forward Intermediate Trackers ("snowmass parameters")

Barrel IT

- spatial resolution 10 μm
- 4 layers (thickness 561 μm Silicon strip)
- r=9 cm (innermost), 30 cm (outermost)
- half z = 18.5 cm (innermost), 62 cm (outermost)
- $|\cos\theta|<0.9$



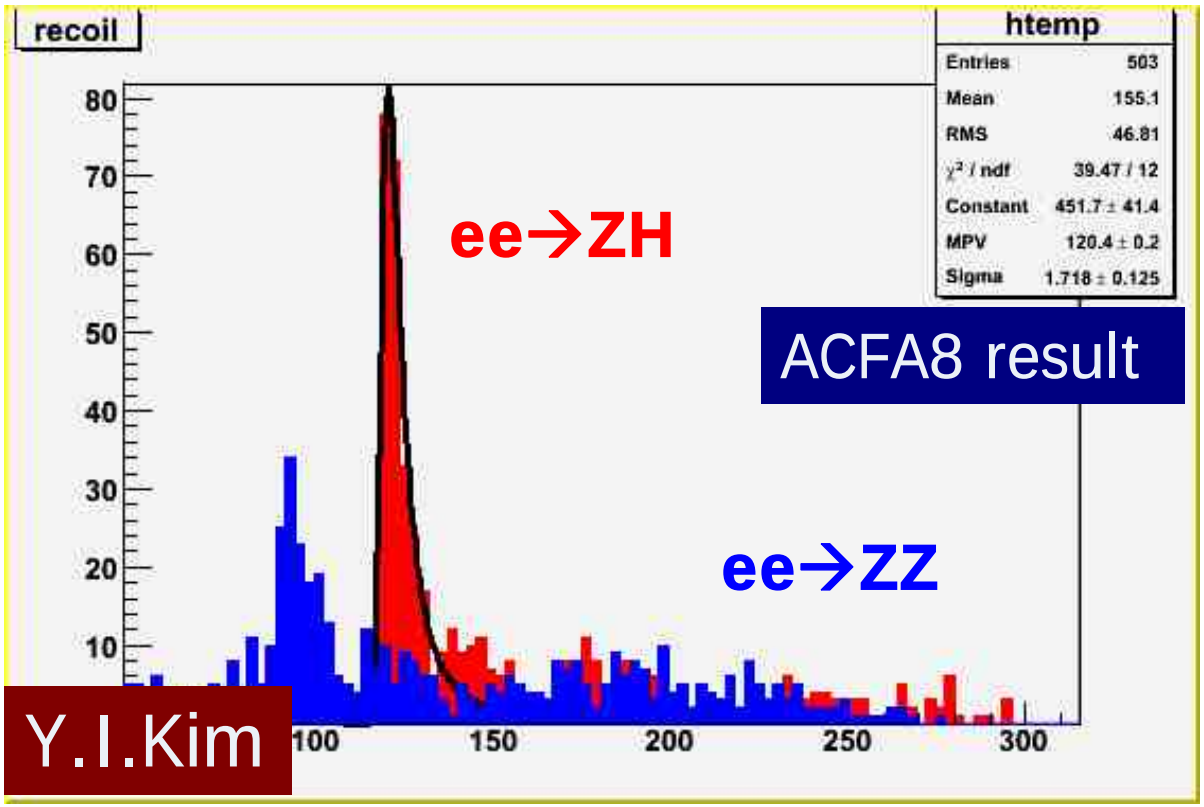
Forward IT

- spatial resolution 10 μm
- 7 layers (thickness 561 μm Silicon strip)

e+e- → ZH, ZZ Study (ongoing)

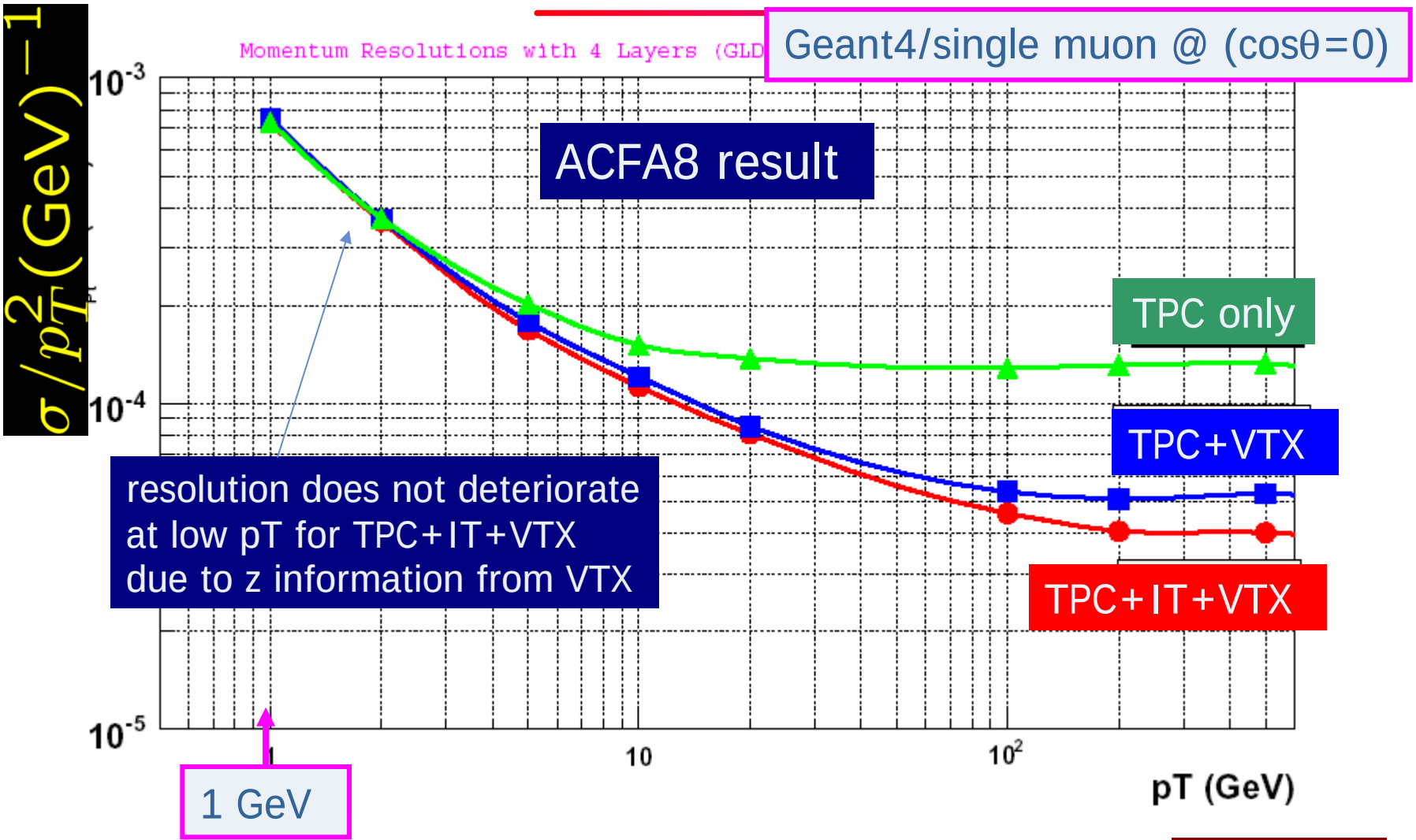
GLD default configuration

- input m_H = 120 GeV + PYTHIA + Geant4



We have been (and will be) working on roles of IT in terms of physics ...

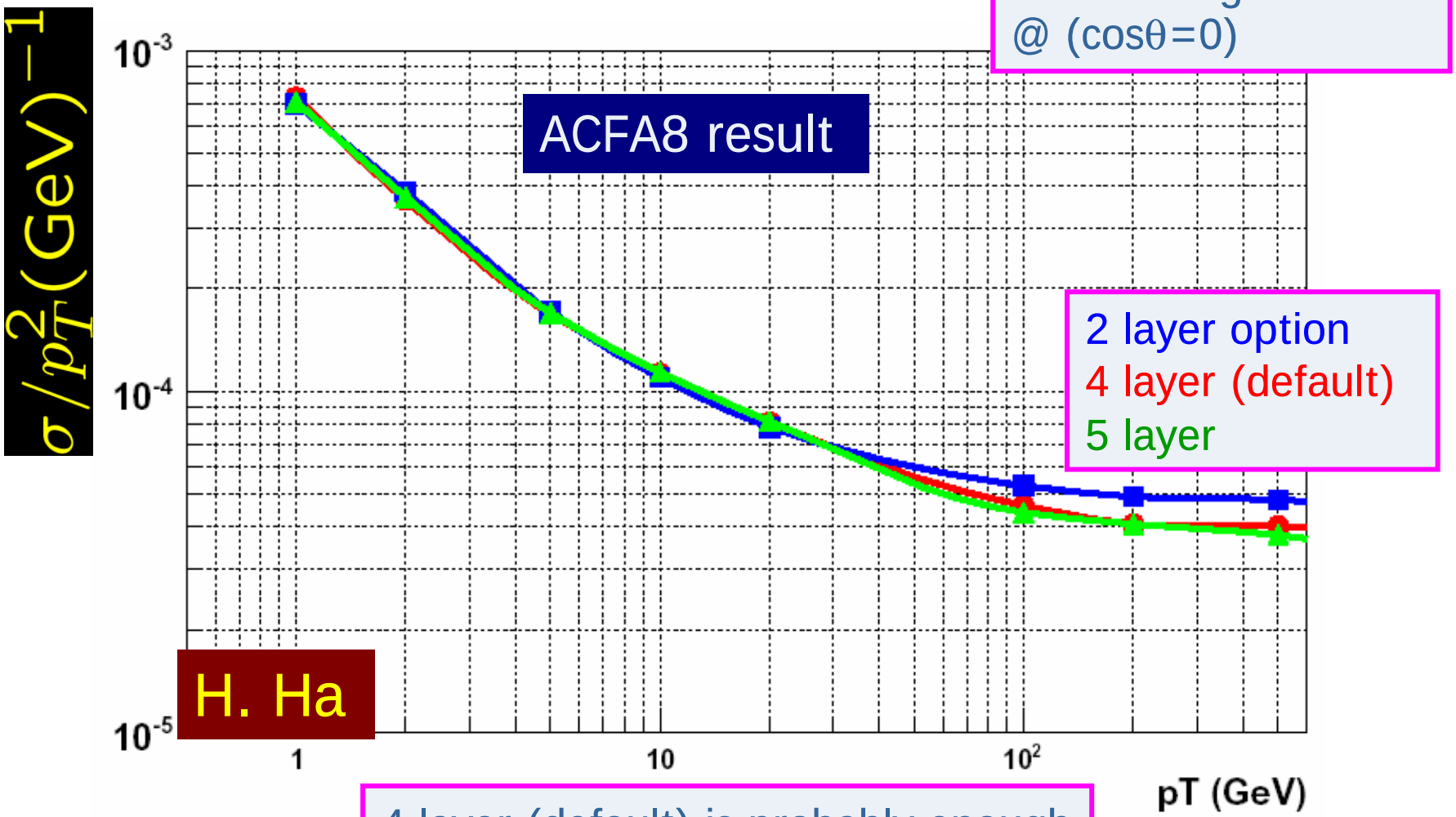
With and W/O IT



- Without IT: 5 x 10^{-5} $(GeV)^{-1}$ (high momentum limit)
- With IT: 4 x 10^{-5} $(GeV)^{-1}$

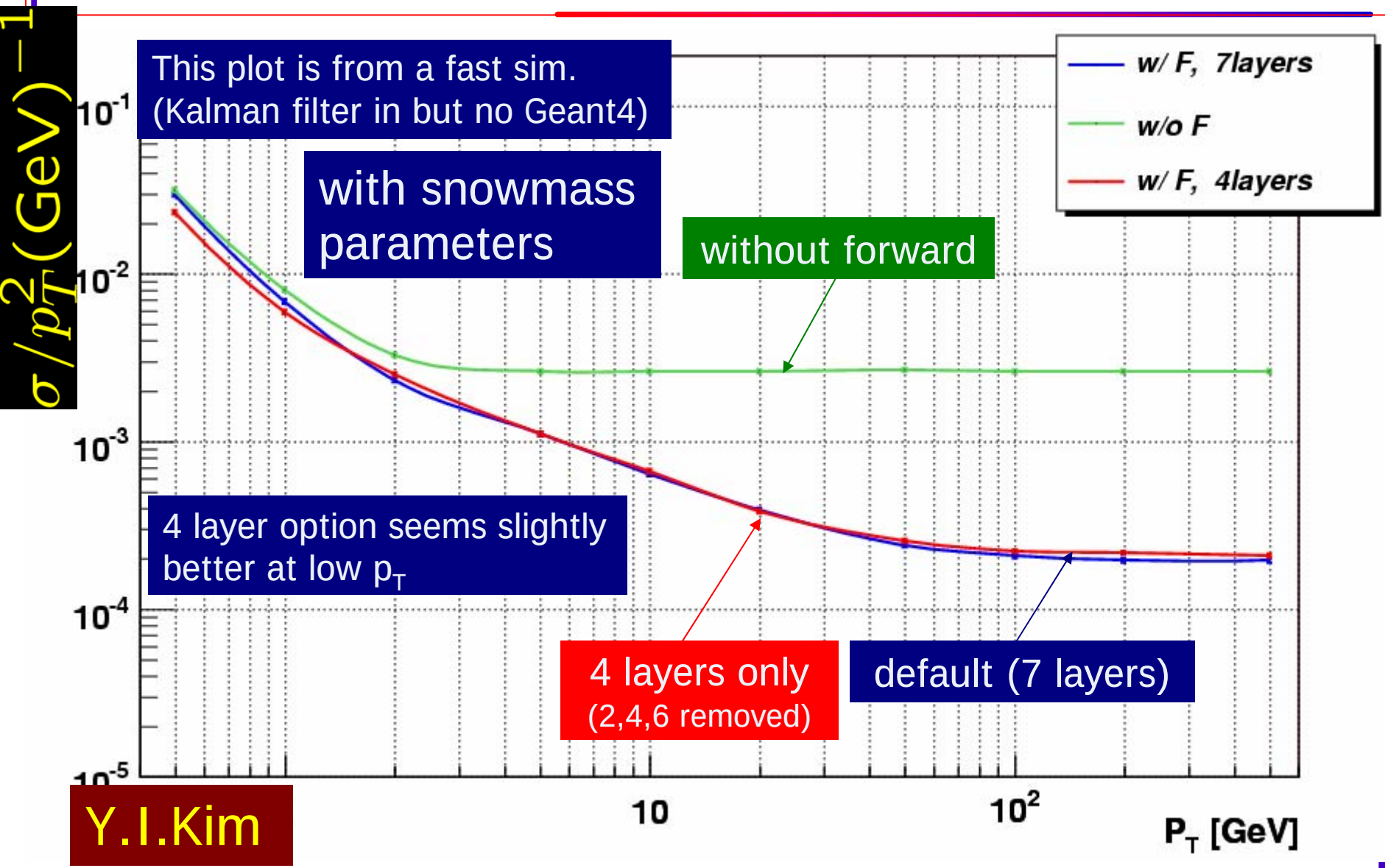
H. Ha

Number of layers vs. resolution



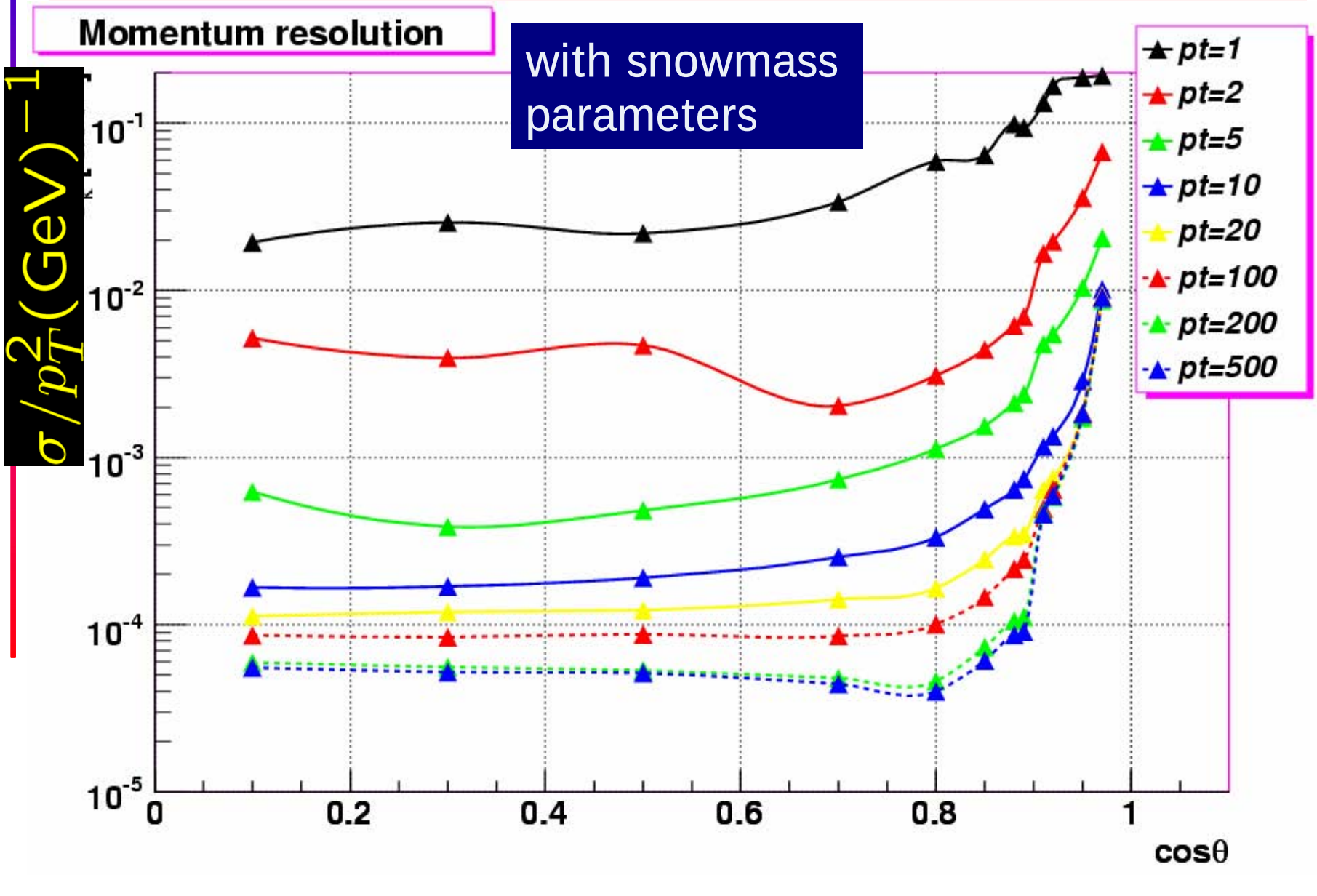
4 layer (default) is probably enough

Number of layers vs. resolution (forward)



Y.I.Kim

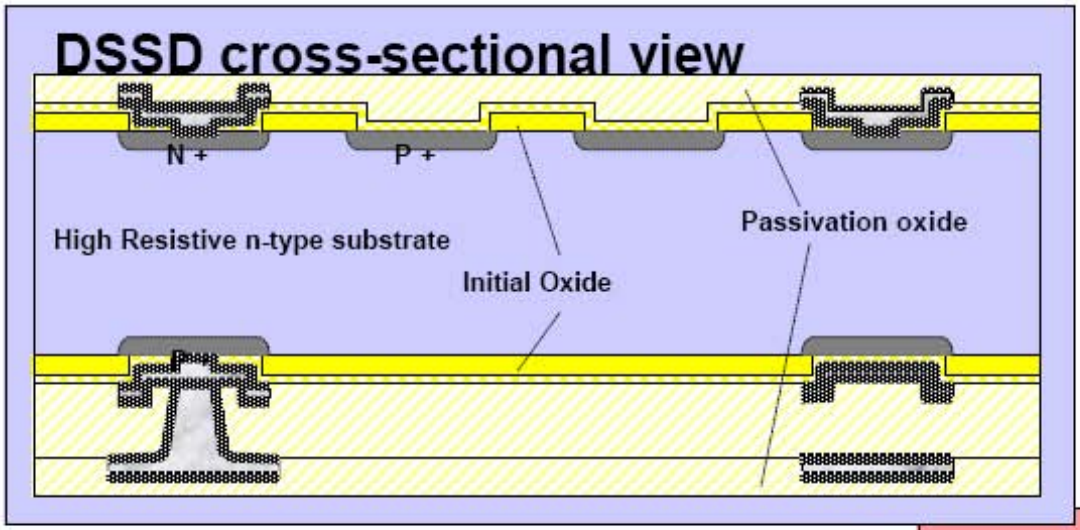
Resolution vs. p_T

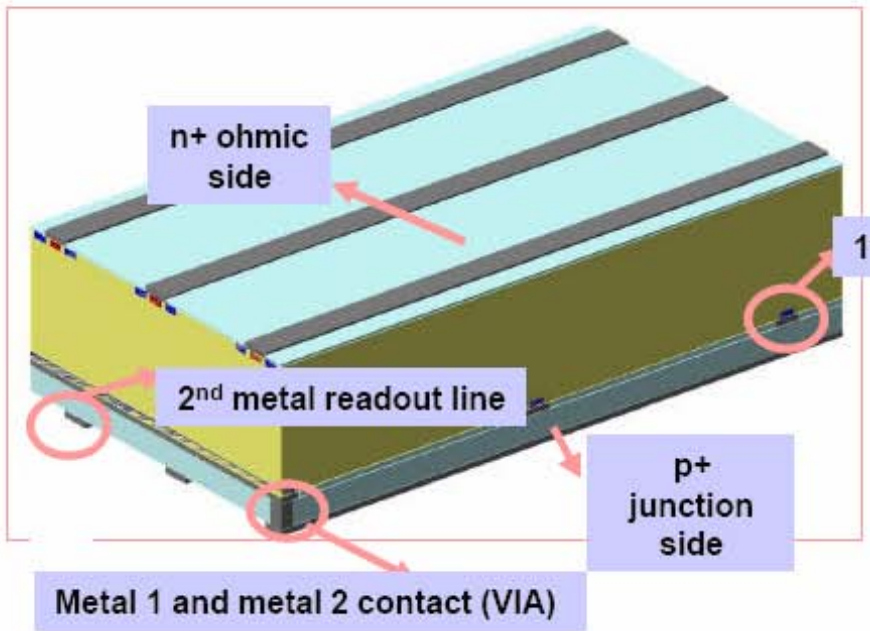


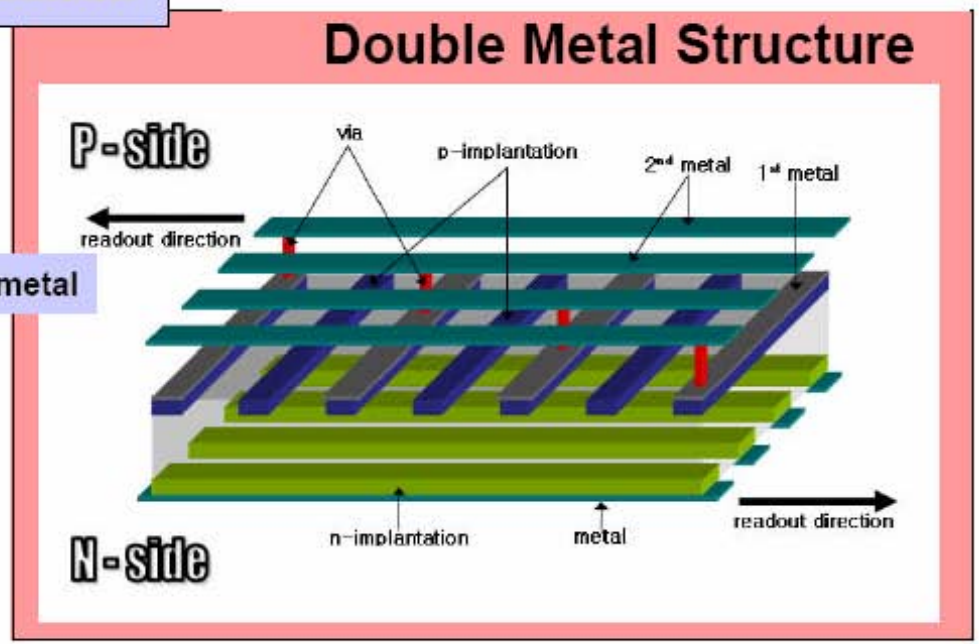
Silicon sensor

- Double side, single side sensor and pxiel sensor
- Characterization of DSSD sensor and S/N
- DC vs AC type
- Radiation damage

DSSD Schematic







DSSD Parameters

LIST	DC-TYPE		unit
	p+ side	n+ side	
Sensor size	55610 X 29460 (include sawing line)		μm
Wafer thickness	380		μm
pitch	100	50	μm
readout trace pitch	50	50	μm
implant strip #	511	511	sensor
number of readout	511	511	sensor
strip length	25600	51072	μm
strip width	9	9	μm

N-side Design

64ch 50μm pitch

512ch 50μm pitch

32ch 50μm pitch

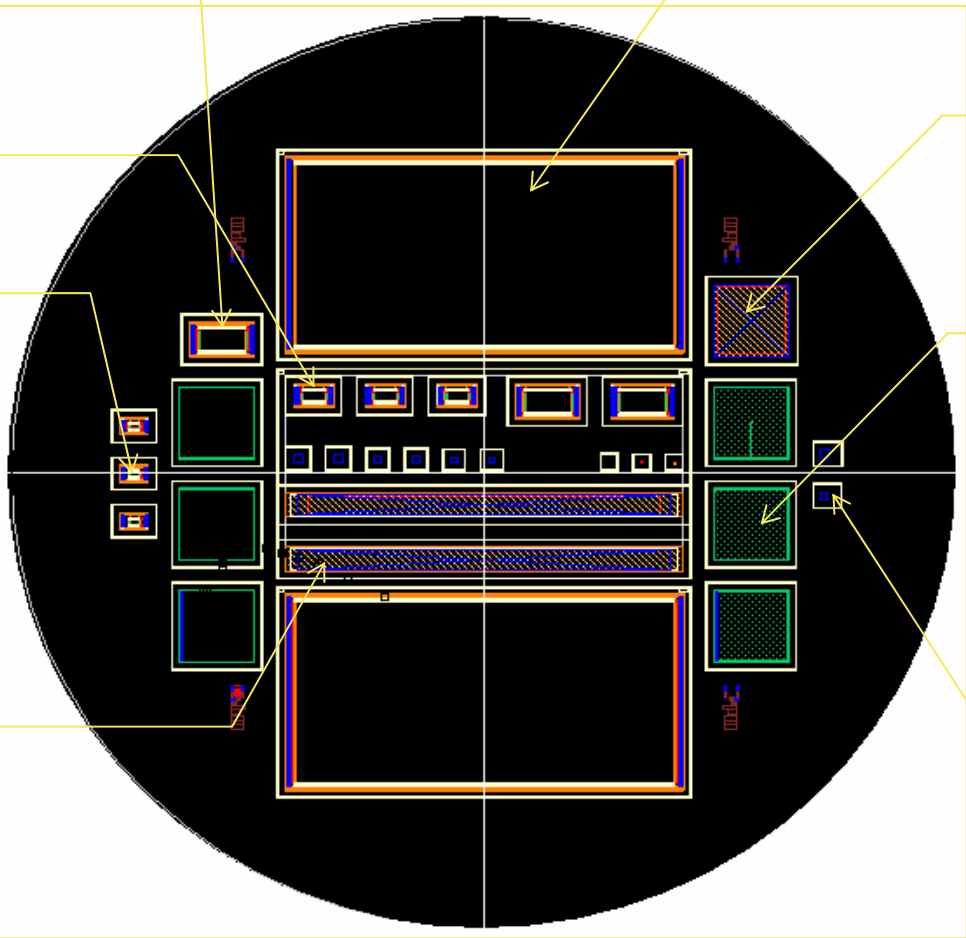
1x1cm^2 PIN diode

16ch 50μm pitch

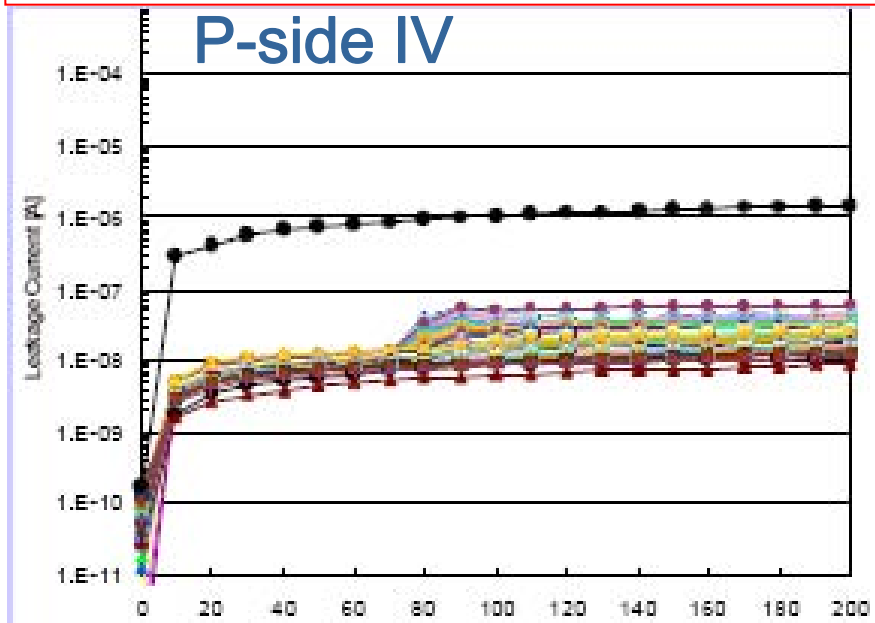
For SDD R&D

Rear-side of SSD

Pixel Array

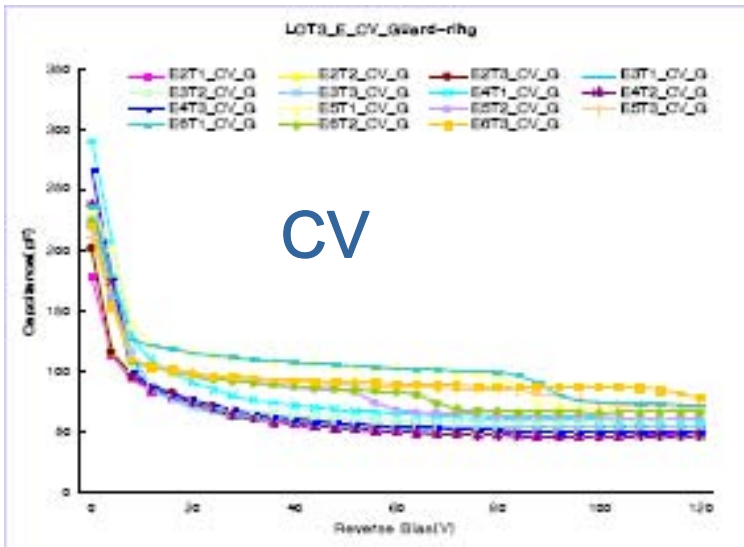


DSSD's from Latest Fab out

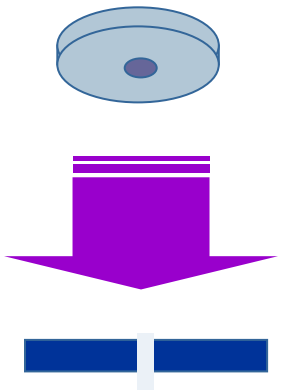


- P-side Guard Ring
  ~ 1uA/sensor @100V
- All P-strips
  ~ 8-50nA/strip @100V
- No extremely Leaky P-strips

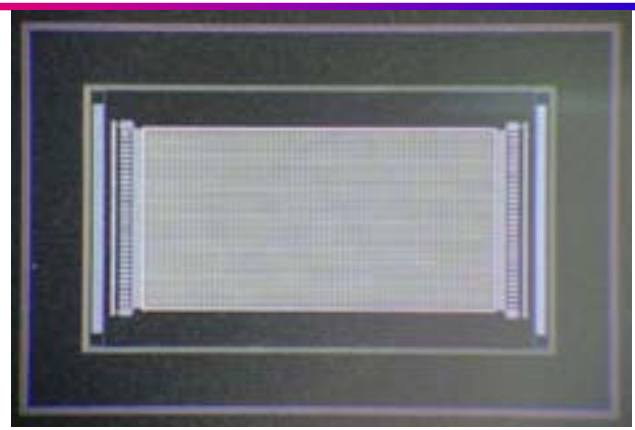
- Full Depletion Voltage ~100V
- Operation Voltage ~120V



Sr-90 beta Source Test



Radiation Source (^{90}Sr β)

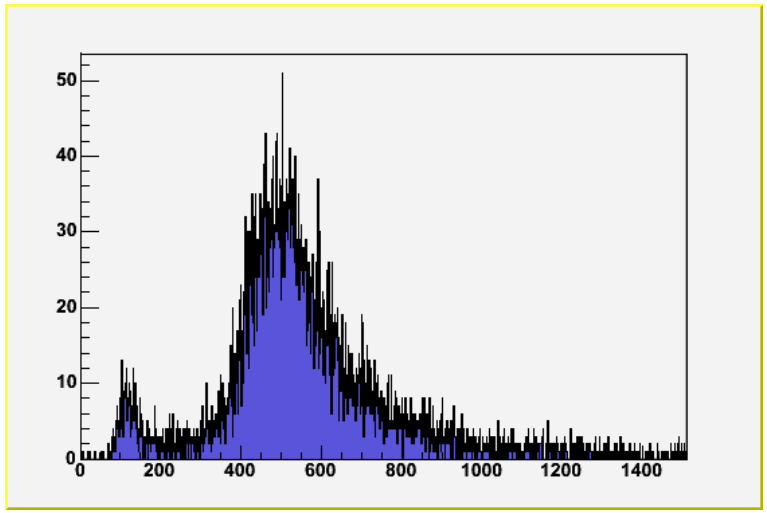


Test Si Detector

Data acquisition

Reference Detector

Trigger



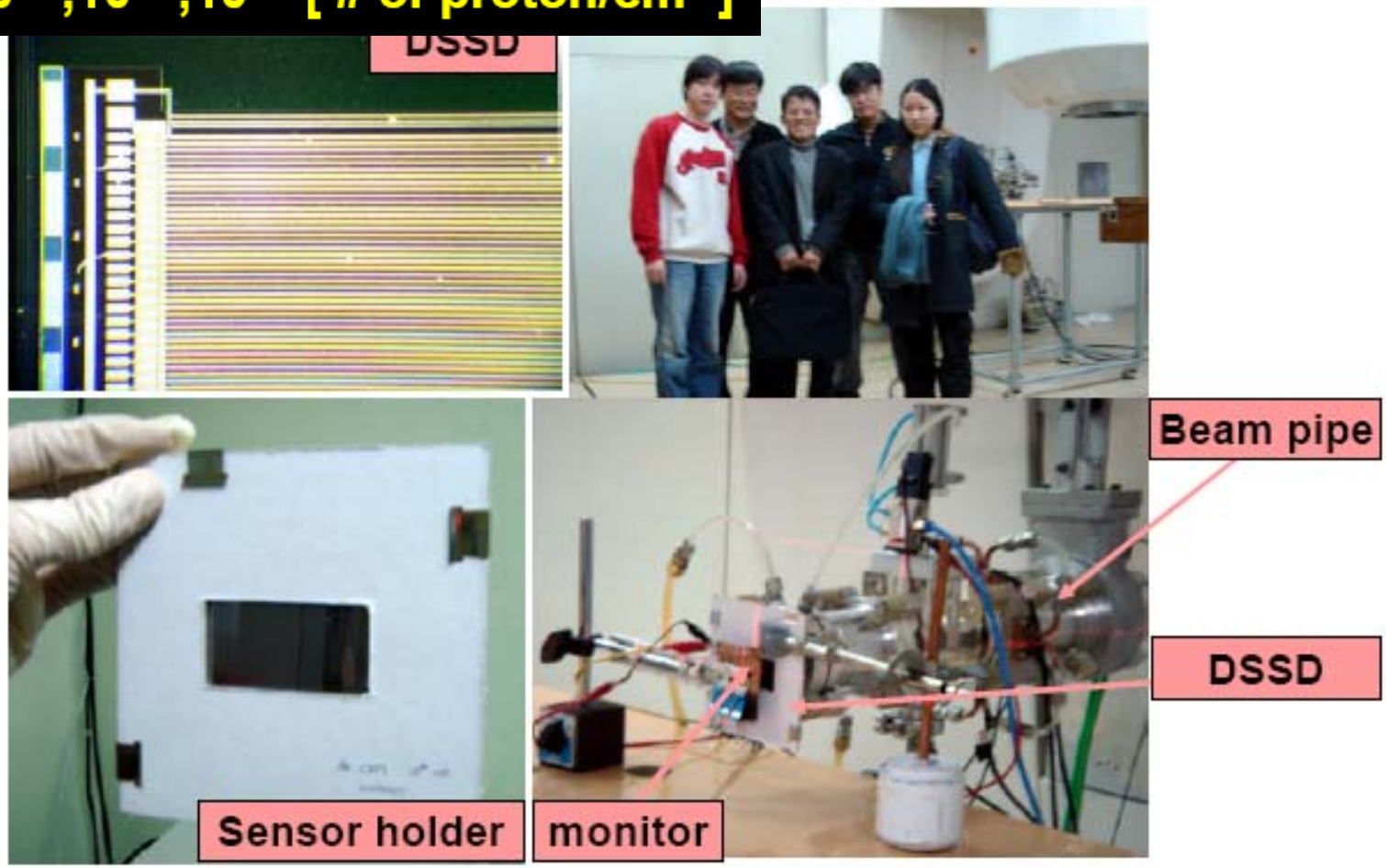
Pedestal sigma = 15.9

S/N = 25

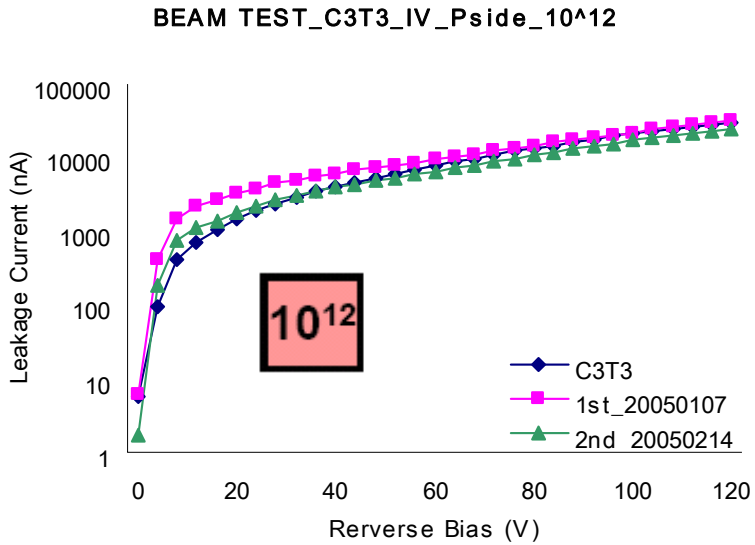
Sensor Irradiation Test

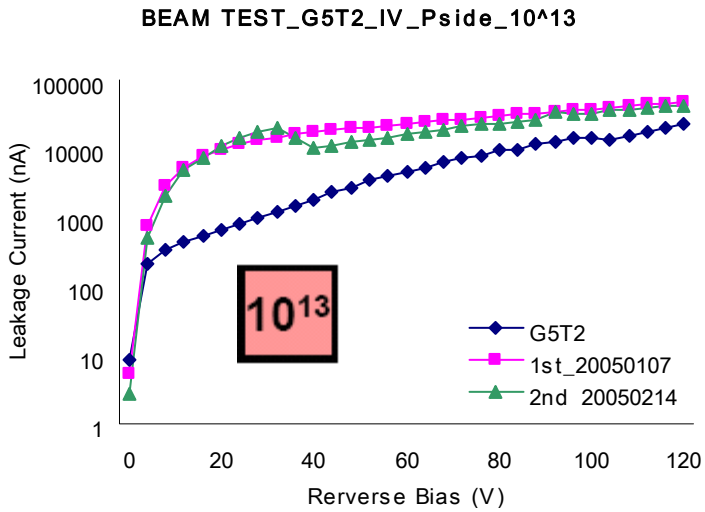
cyclotron in Korea Institute of Radiological and Medical Sciences : 35MeV proton cyclotron

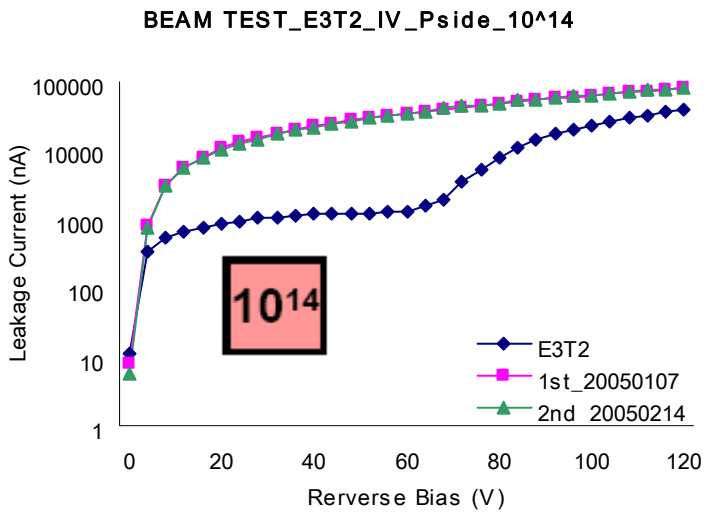
10^{12} ,10^{13} ,10^{14} ,10^{15} [# of proton/cm^2]

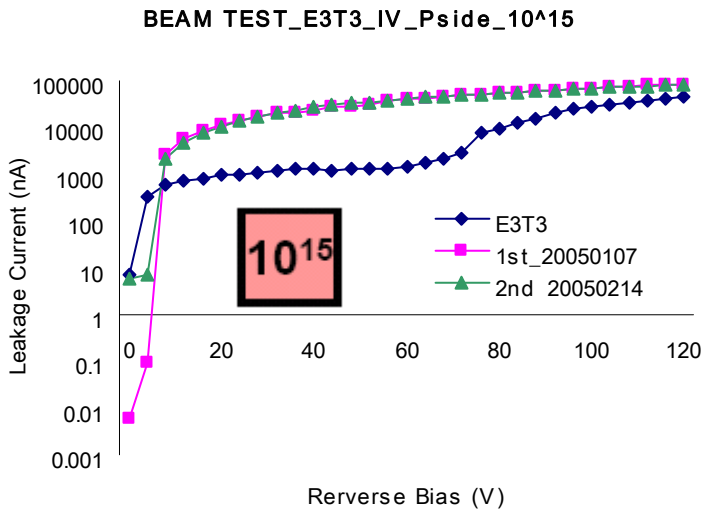


I/V before and after irradiation









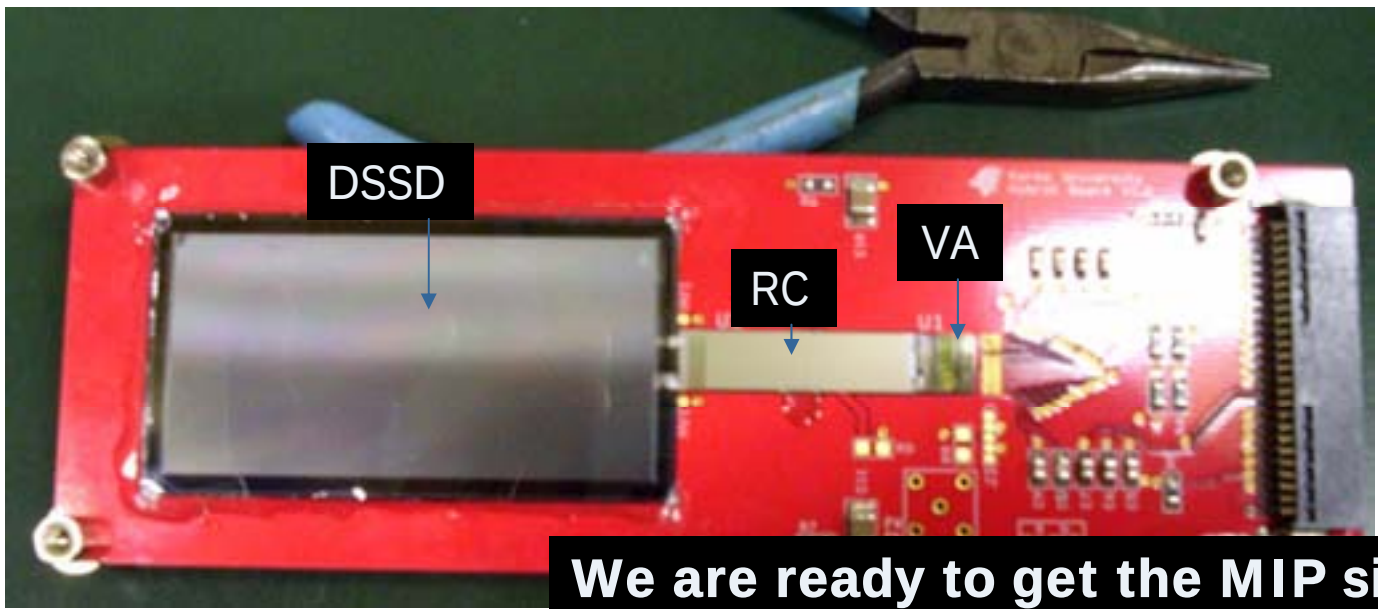
Electronics & support structure

- PreAmp (+shaping and holder with VA)
- Hibrid board (control +HV)
- FADC

- New Readout Electronics with pipeline
- Long ladder issue (S/N)
- Support Structure

Status of Hybrid Board

- **We mounted latest fab out DSSDs to the hybrid** (August 9)
  - ✓ VA1 + RC sensor + 511 channel DSSD
- **Wire bonding done** (August 11)
  - ✓ pads – VA : by a company (LP electronics in Korea)
  - ✓ VA – RC, RC – DSSD : done by a KEK expert (T.Tsuboyama)



We are ready to get the MIP signal!

Summary

- A lot of progress on BIT and FIT Configuration since ACFA8
  1) BIT Optimization
  2) FIT baseline configuration

- Silicon Sensor R&D is going as planned.
  1) DSSD design and fabrication
  2) Characterization & S/N OK
  3) Radiation damage test results.

- Readout electronics is in progress.

Future plan for study

- **Configuration**

1. Endcap Silicon Tracker between TPC and CAL
2. Background study
3. Single side vs Double side SD
4. IT Optimization for physics improvement

- **Silicon Sensor R&D**

1. Single side sensor (and pixel sensor)
2. AC type
3. Larger wafer (6”, 8”)

- **Readout electronics & Support Structure**

1. New Readout Electronics with pipeline
2. Long ladder issue (S/N, shaping time)