The LCFI Project

Snowmass 2005

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CCLRC Rutherford Appleton Laboratory

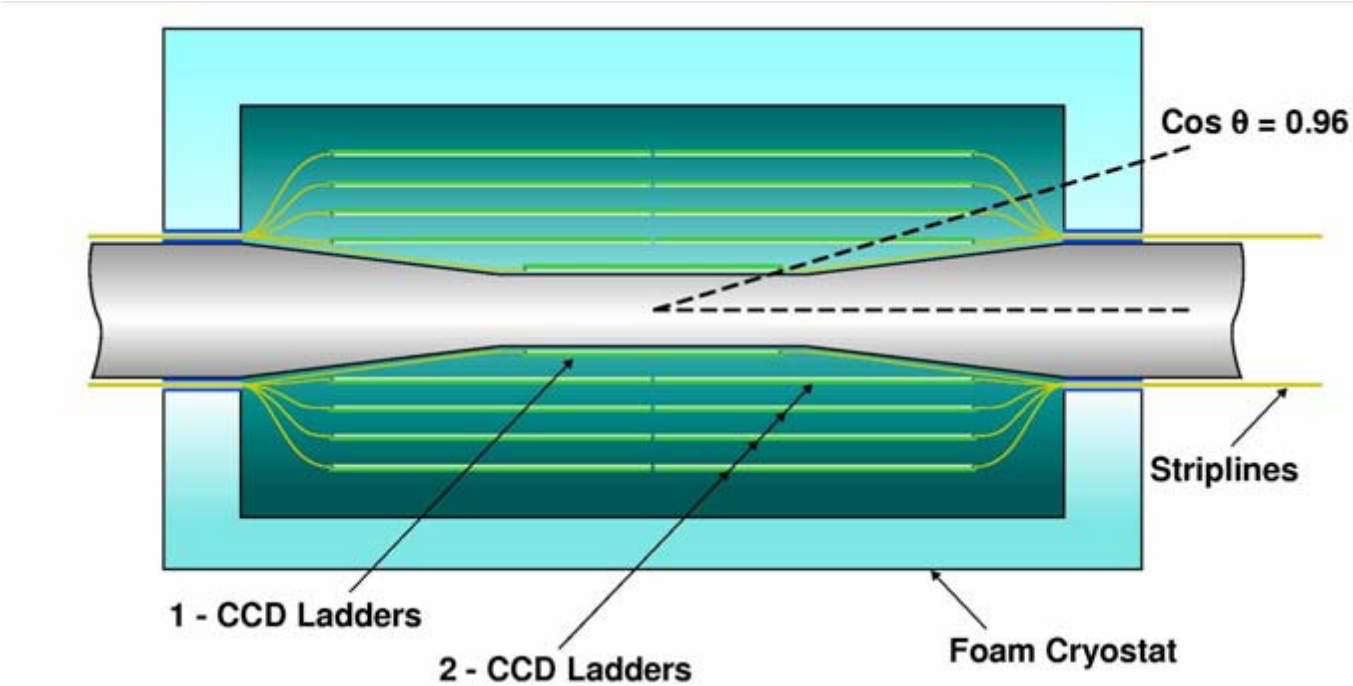
For the LCFI Collaboration

LCFI Research Programme

R&D programme for ILC vertex detector:

1. **Physics Studies** *(Sonja's talk)*
2. **Mechanical Development**
3. **Detector Development**

Baseline Vertex Detector



- 800 Mchannels of 20×20 μm pixels in 5 layers
- Optimisation:
  - Inner radius (1.5 cm?)
  - Readout time (50 μs?)
  - Ladder thickness (0.1% X_0?)

LCFI Mechanical Studies

1. Thin Ladder Mechanics

- **Materials and designs for $\Delta T \approx 100K$**
- **Preference for uniform material in tracking volume**
- ***CCDs routinely thinned to epitaxial layer***

2. Global Design

- **Ensure ladder designs practical**

3. Cooling

- **Gas cooling has always been assumed…**

Mechanical Options

Target of 0.1% X_0 per layer

(100μm silicon equivalent)

1. Unsupported Silicon

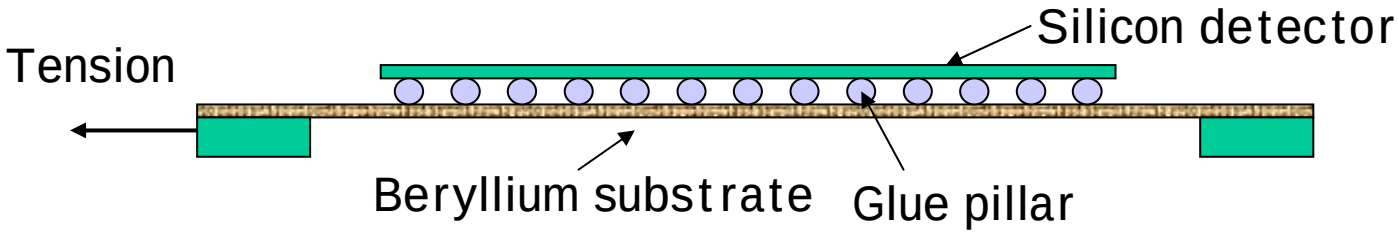
- Longitudinal tensioning provides stiffness
- No lateral stability
- Not believed to be promising

2. Thin Substrates

- Detector thinned to epitaxial layer (20μm)
- Silicon glued to low mass substrate for lateral stability
- Longitudinal stiffness still from tension
- Beryllium has best specific stiffness

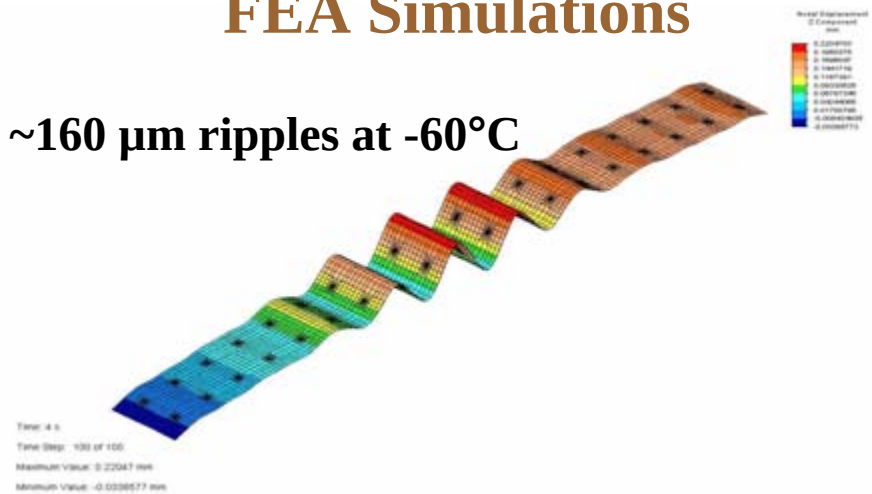
3. Rigid Structures

Mechanical Studies of Be-Si

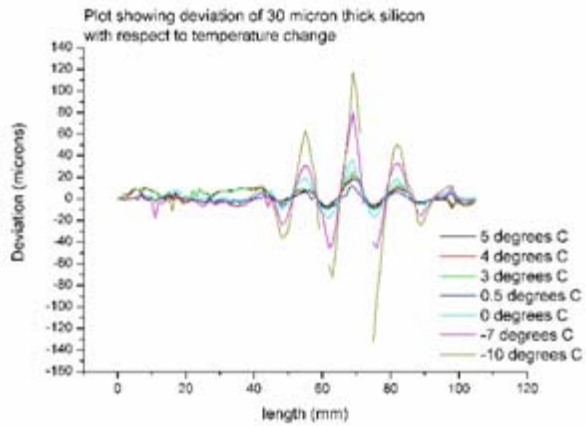


FEA Simulations

~160 µm ripples at -60°C



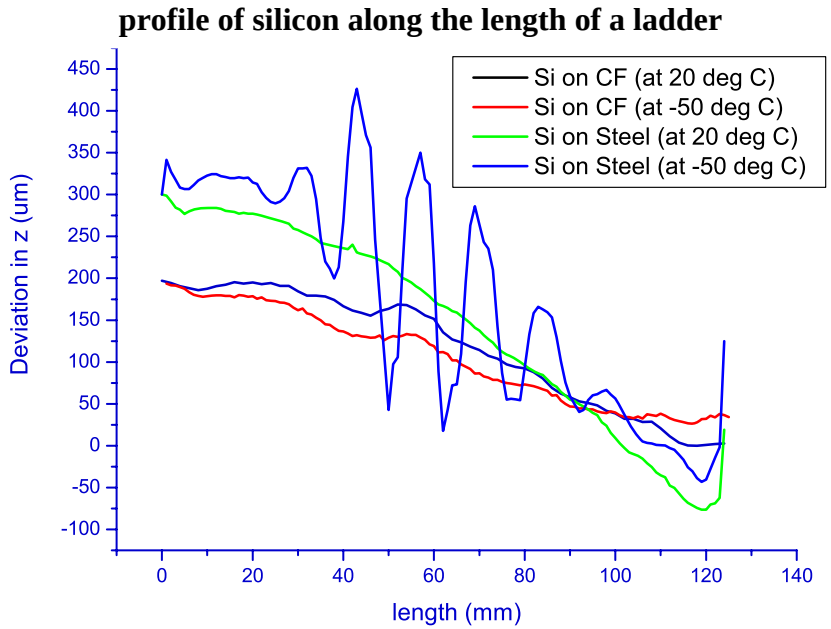
Physical Prototyping



- **Good qualitative agreement**
- **Minimum thickness ~ 0.15% X_0**

Carbon Fibre Substrates

- **Carbon fibre has better CTE match than beryllium**



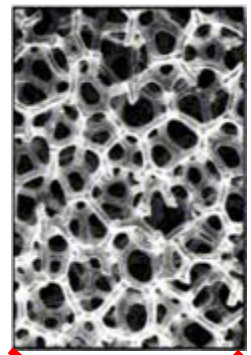
- **Prototype ~ 0.09% X_0**
  - **No rippling down to < 200K**
  - **Lateral stability insufficient**

Other Thin Substrates

- **Considerations for other materials**
  - **CTE match**
  - **thickness**
  - **financial**
- **Ceramics, advanced materials….**
- ***Diamond samples in hand***

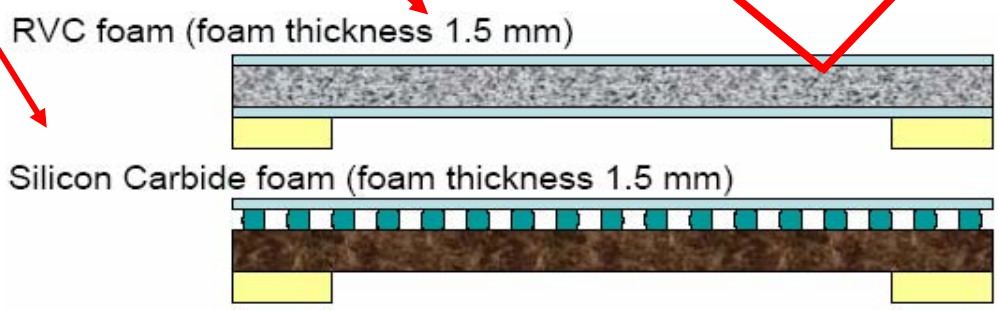
Rigid Structures

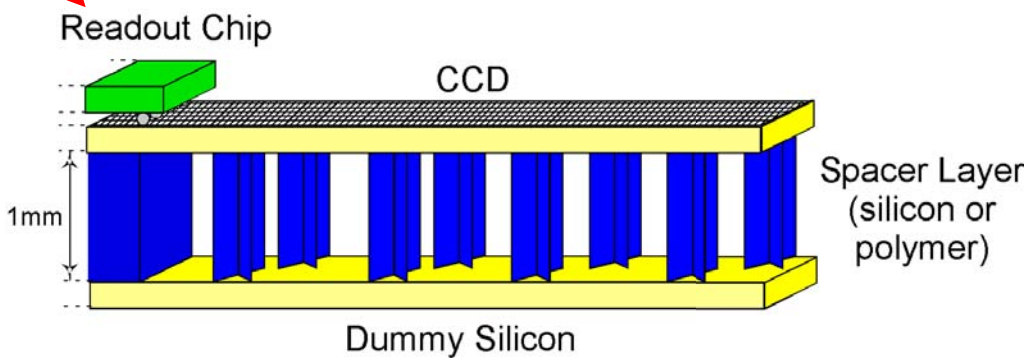
Foam: substrate or sandwich core



- **Macroscopically uniform**
- **No tensioning needed**

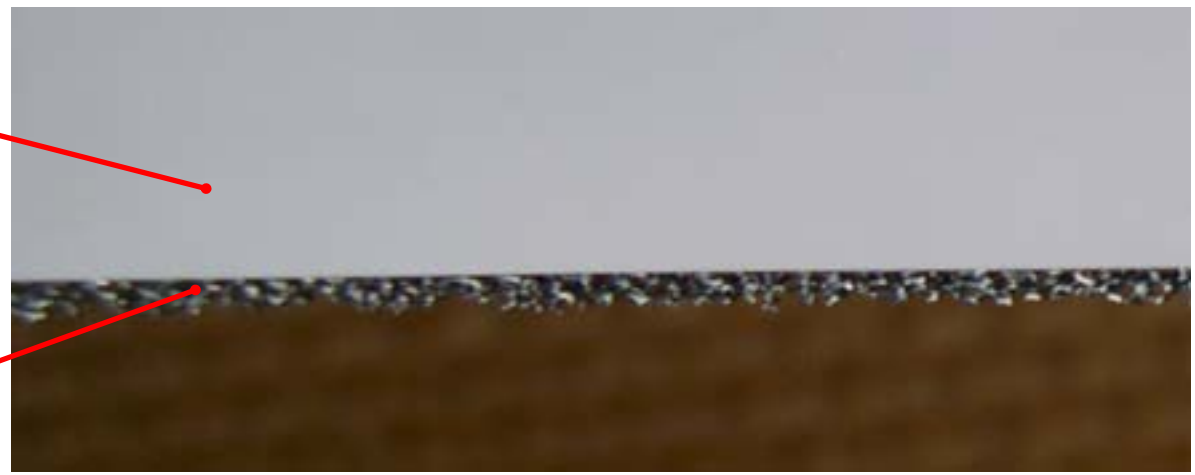
Other approaches exist



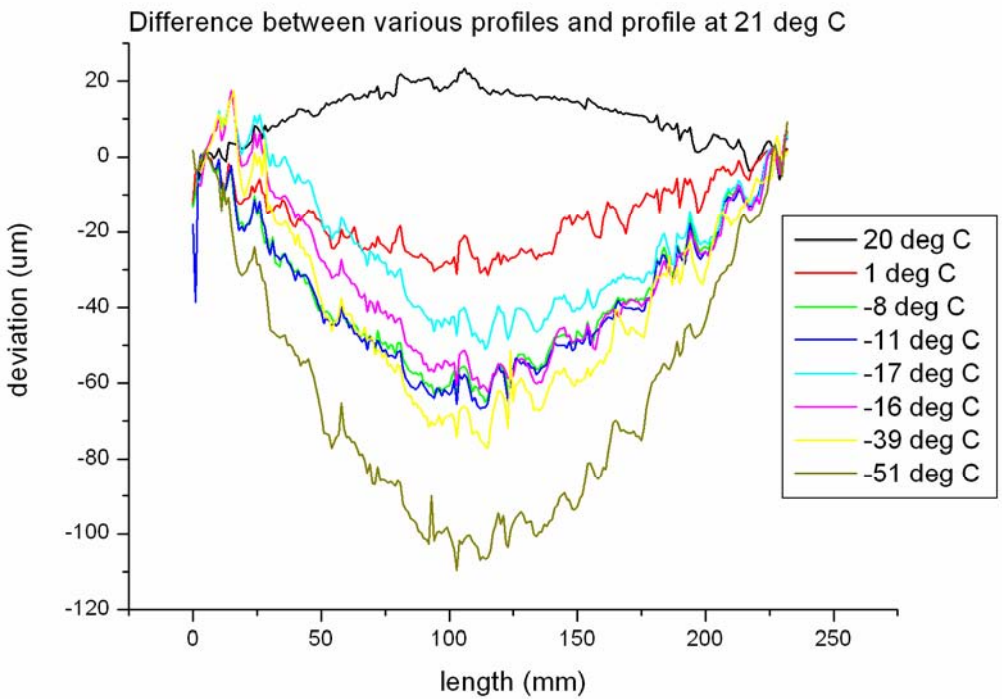


Foam Prototypes

- 3% RVC
  - Sandwich
  - 0.09% X_0
  - Mechanically unsatisfactory
  - Working on glue application
- 8% Silicon Carbide
  - Single-sided
  - 0.14% X0
  - 3-4% believed possible

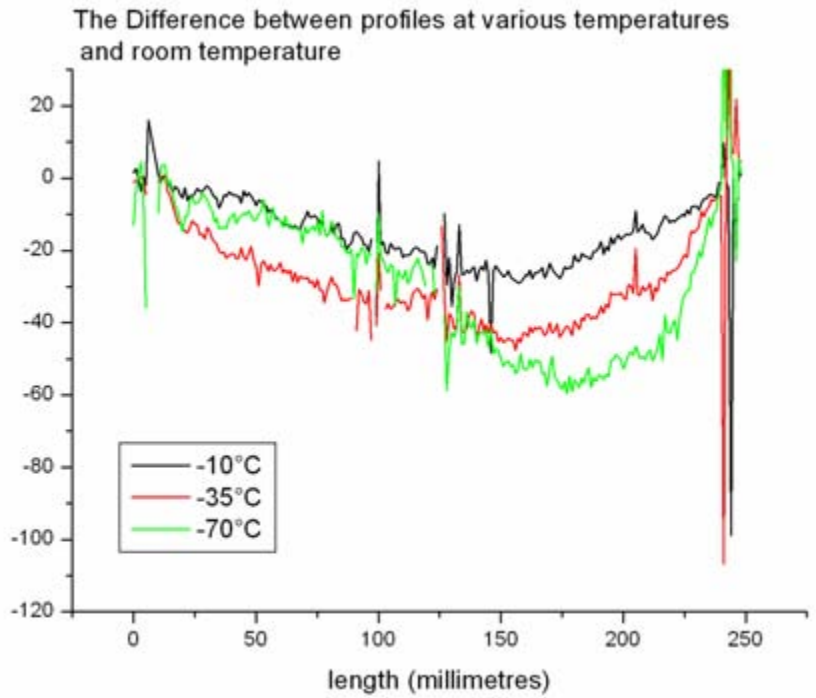


Silicon Carbide Foam

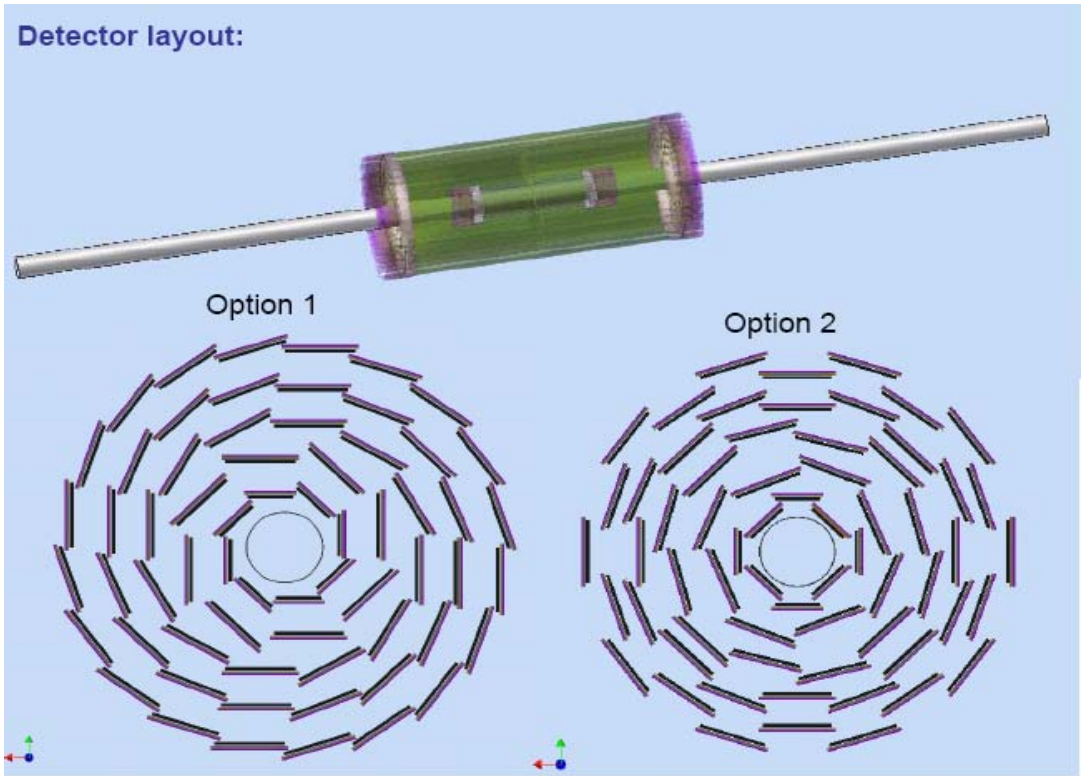


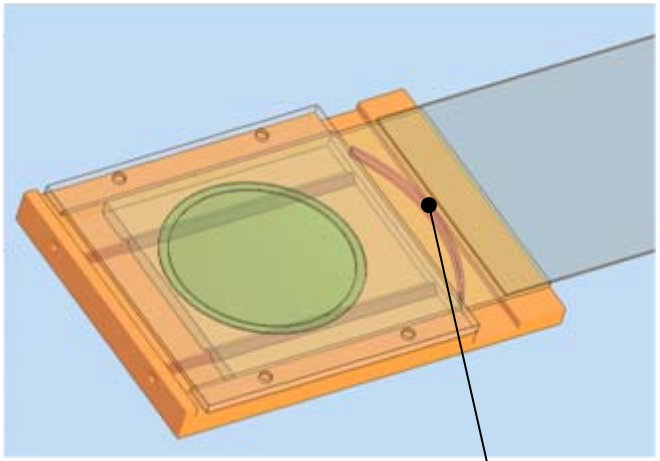
Thin glue layer

Glue "pillars"

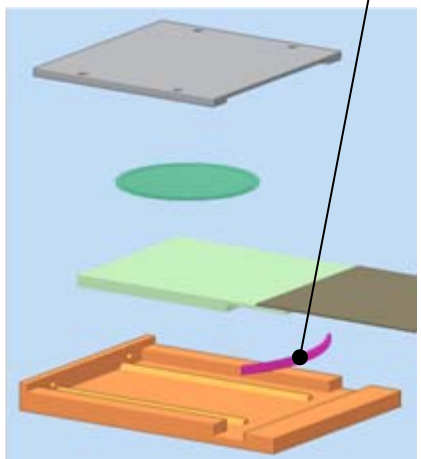


Global Design Work





Ladder end with leaf spring



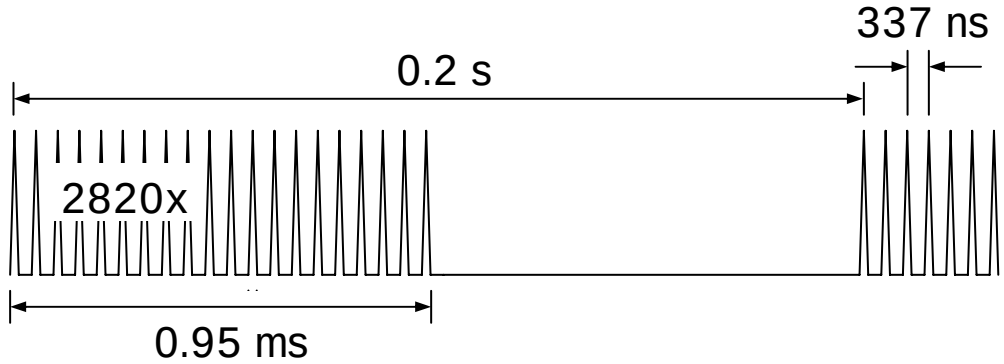
- **Enough detail for ladder design "sanity check"**

Mechanical Plans

- **Continue work on ladder designs**
  - **Foams looking promising**
  - **Settle on favoured technology ~ 2 years**
  - **Start looking at production issues**
- **Increase effort on global and cooling design**

Sensors: The Challenge

Beam Time Structure:



What readout speed is needed?

- **Inner layer 1.6 MPixel sensors**
- **Once per bunch = 300ns per frame : *too fast***
- **Once per train ~200 hits/mm^2 : *too slow***
- **10 hits/mm^2 => 50μs per frame: just right**

(Fastest commercial imaging ~ 1 ms/MPixel)

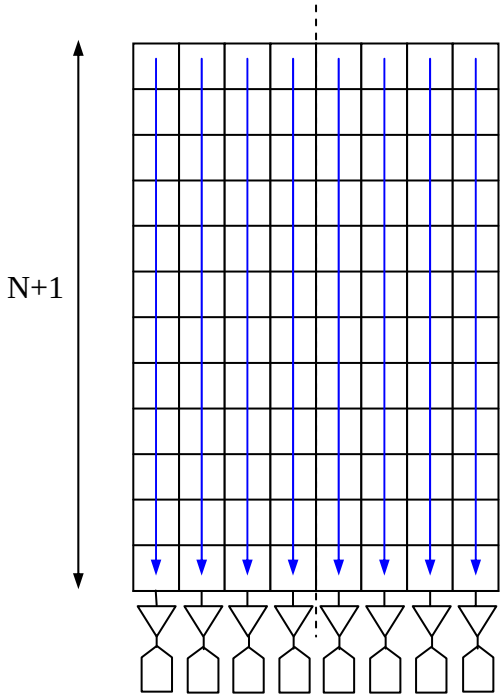
Power dissipation – gas volume cooling

Sensor Research

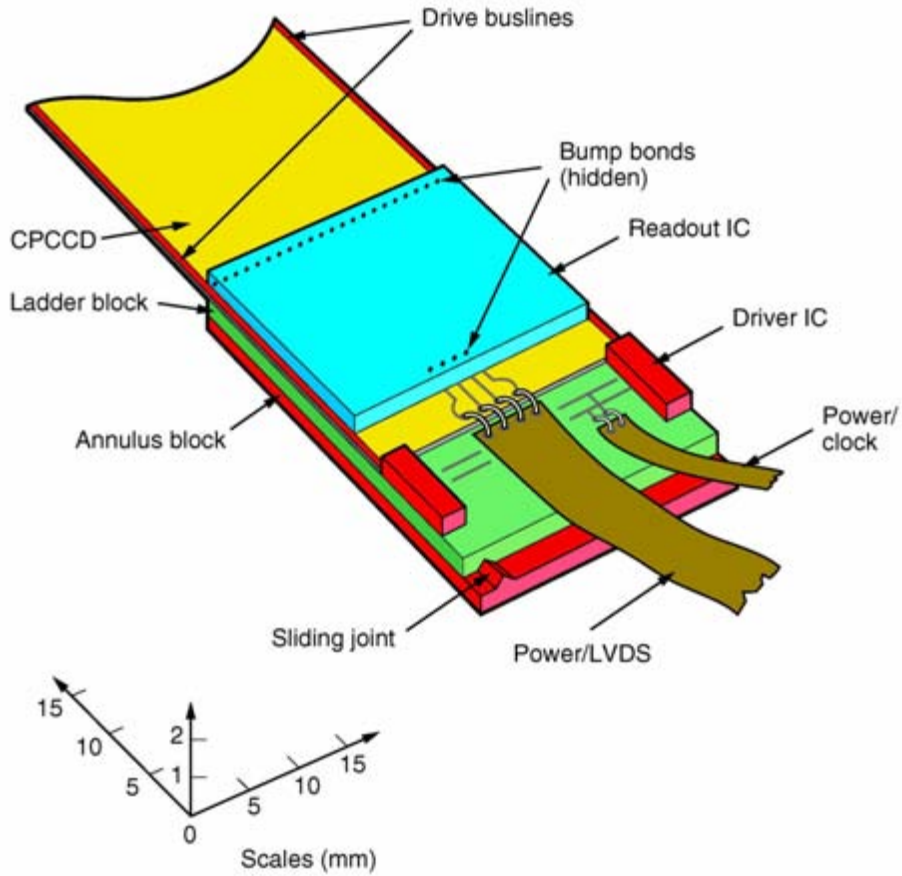
1. **Column Parallel CCDs**
   - Focus so far - building on past experience
   - Readout during bunch train
   - Clock drive major challenge
2. **Storage Sensors**
   - Increased robustness
   - Reduced driver requirements
   - ISIS and FAPS technologies

Column Parallel CCD

- **Separate amplifier and readout for each column**
- **50 MHz clock rate**



Column Parallel CCD
Readout time = $(N+1)/F_{out}$



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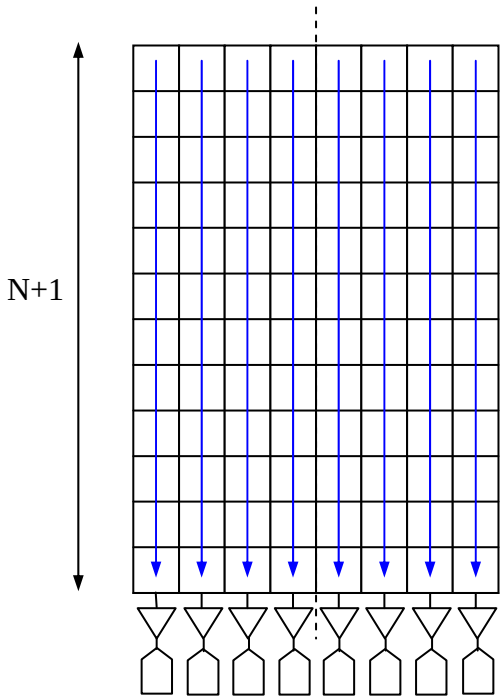

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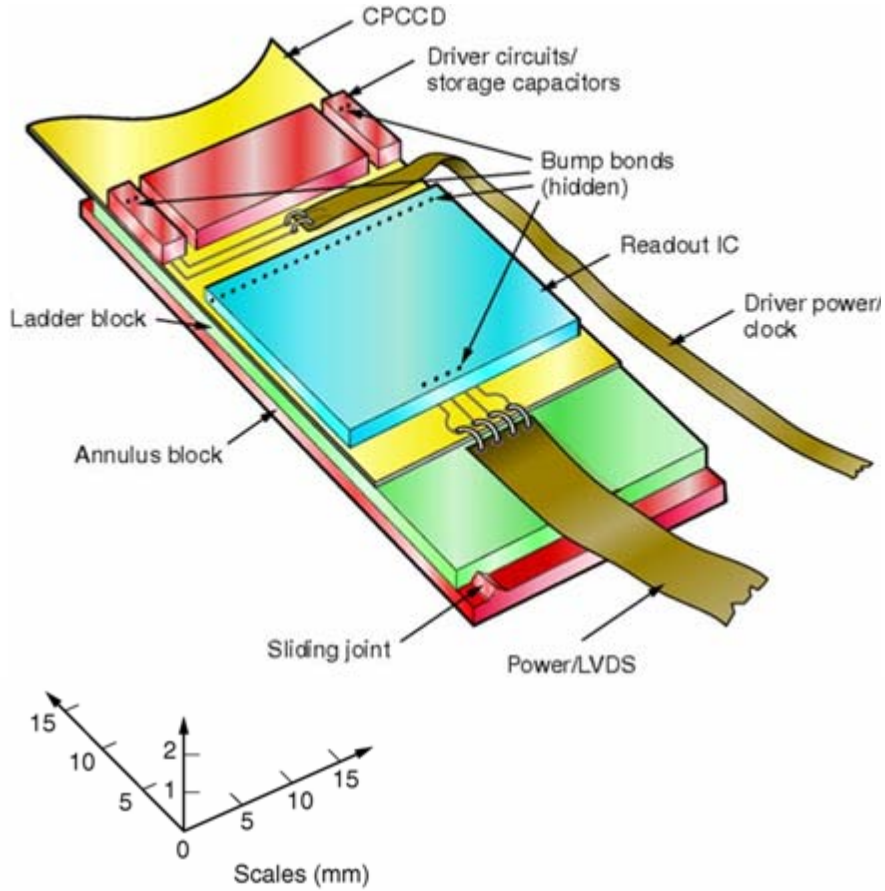
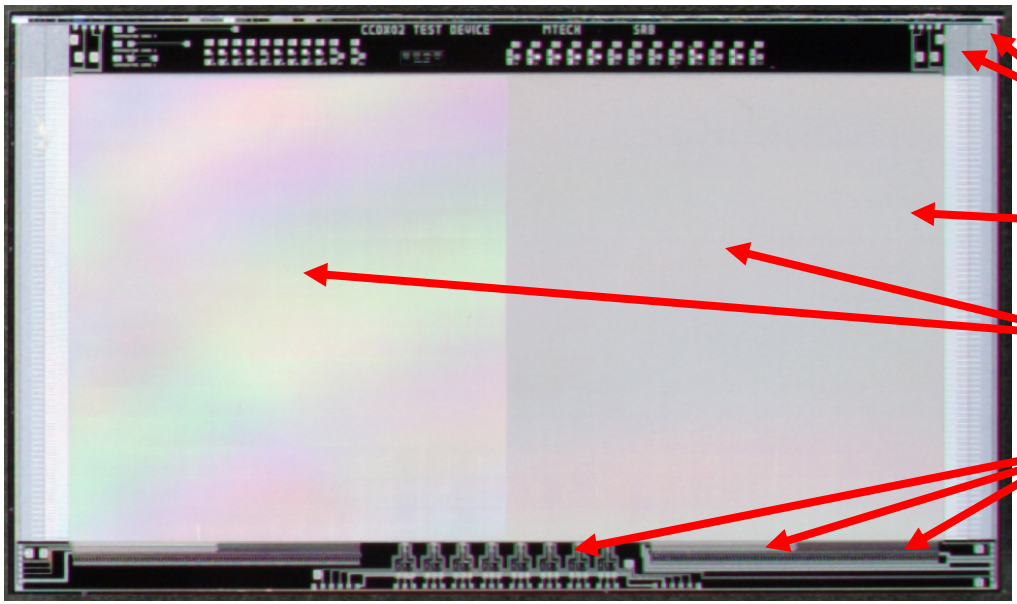


- **Clock drive is real challenge**

Prototype CP CCD



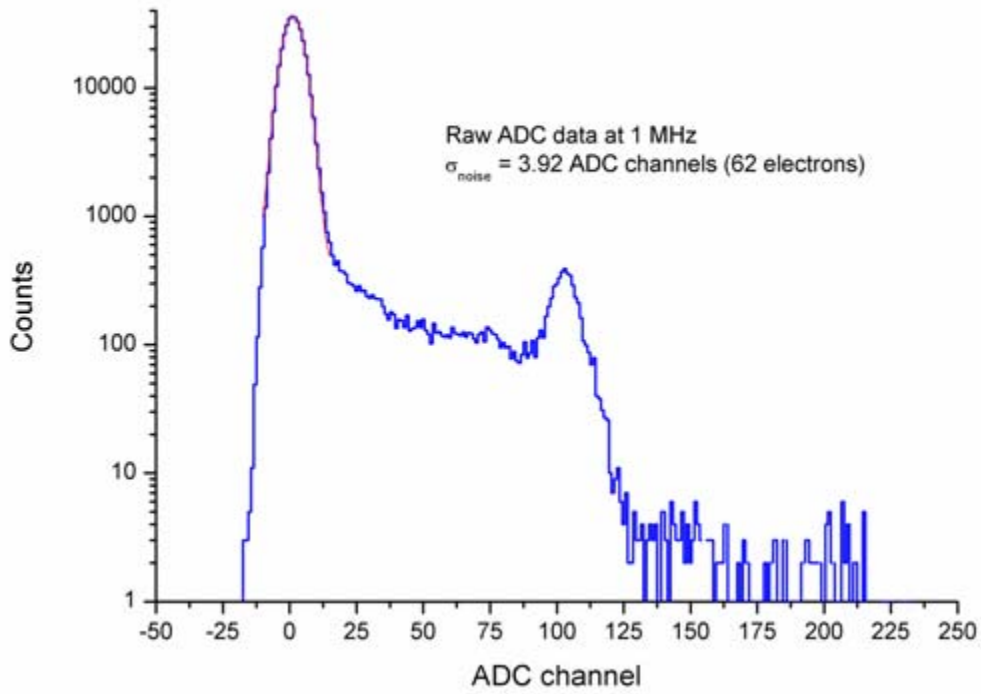
CPC1 produced by E2V

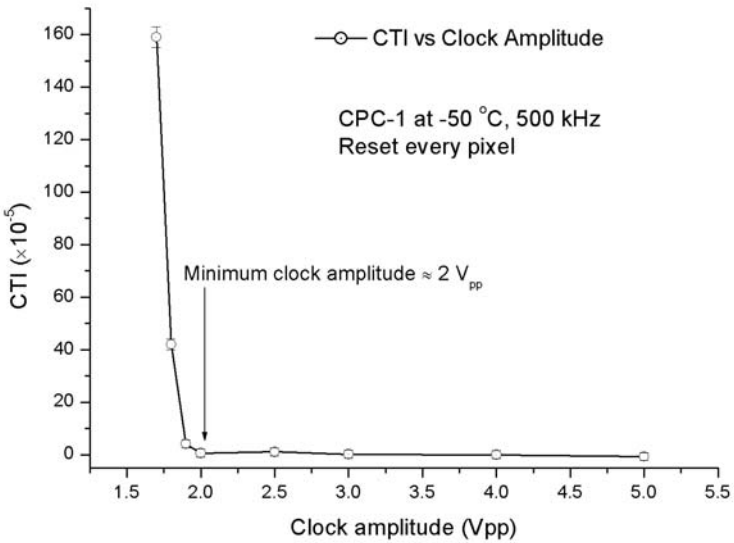
- Two phase operation
- Metal strapping for clock
- 2 different gate shapes
- 3 different types of output
- 2 different implant levels

➢*Clock with highest frequency at lowest voltage*

CPC1 Results

- **Noise ~ 100 electrons (60 after filter)**
- **Minimum clock ~1.9 V**



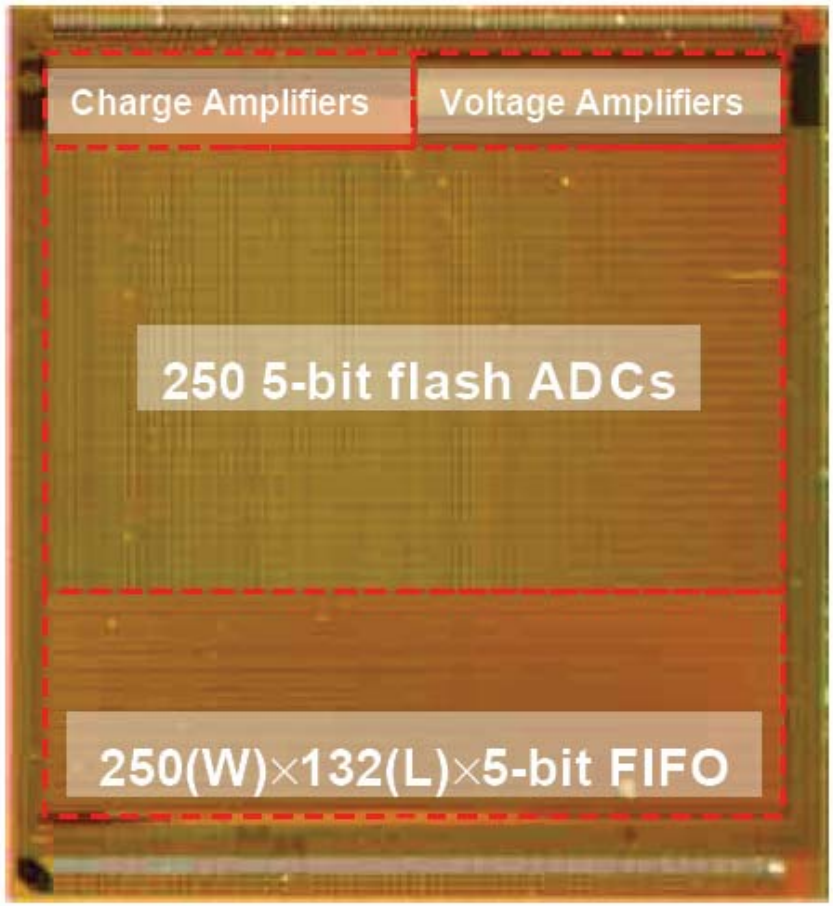


- **Maximum frequency > 25 MHz**
  - **inherent clock asymmetry**

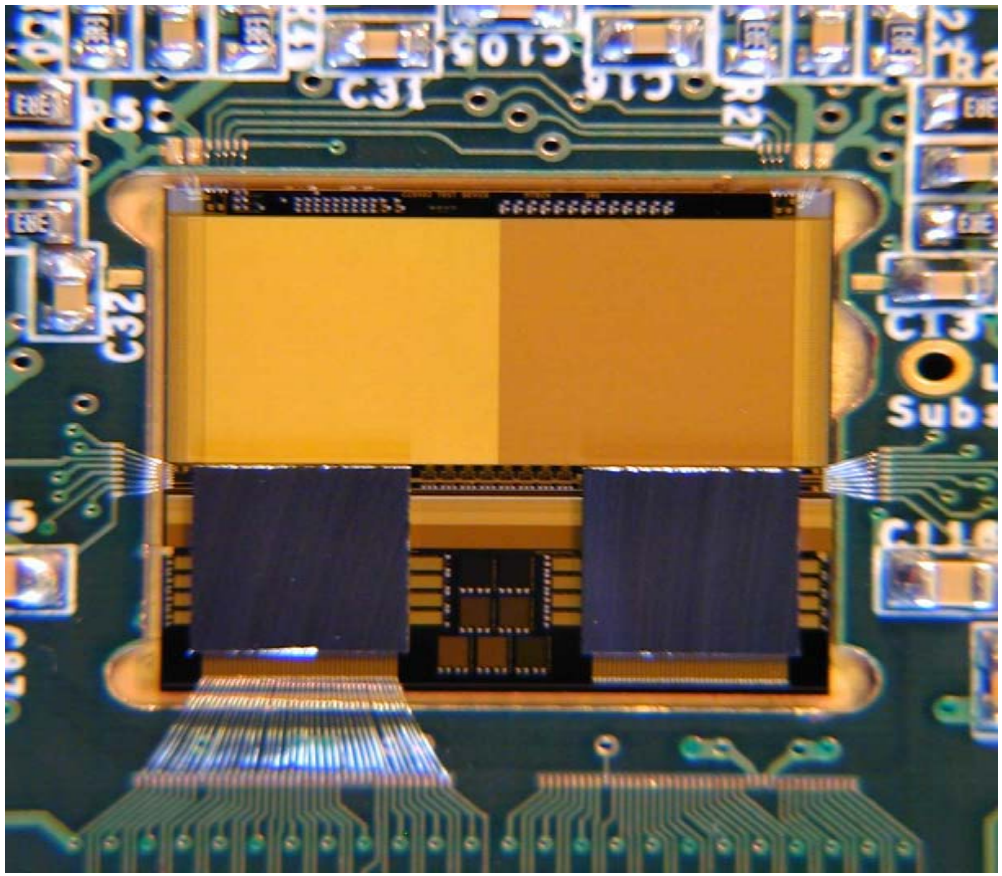
CP Readout ASIC

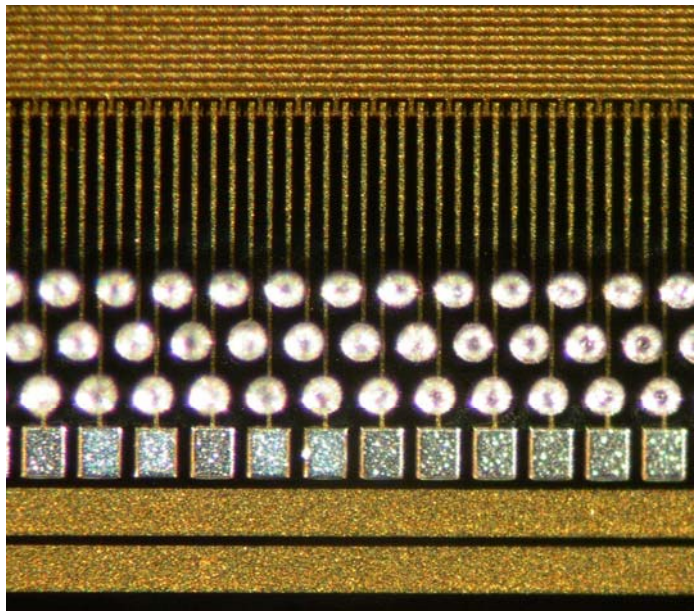
CPR1 designed by RAL ME Group

- **IBM 0.25 µm process**
- **250 parallel channels with 20 µm pitch**
- **Designed for 50 MHz**
- **Data multiplexed out through 2 pads**



Bumped Assemblies

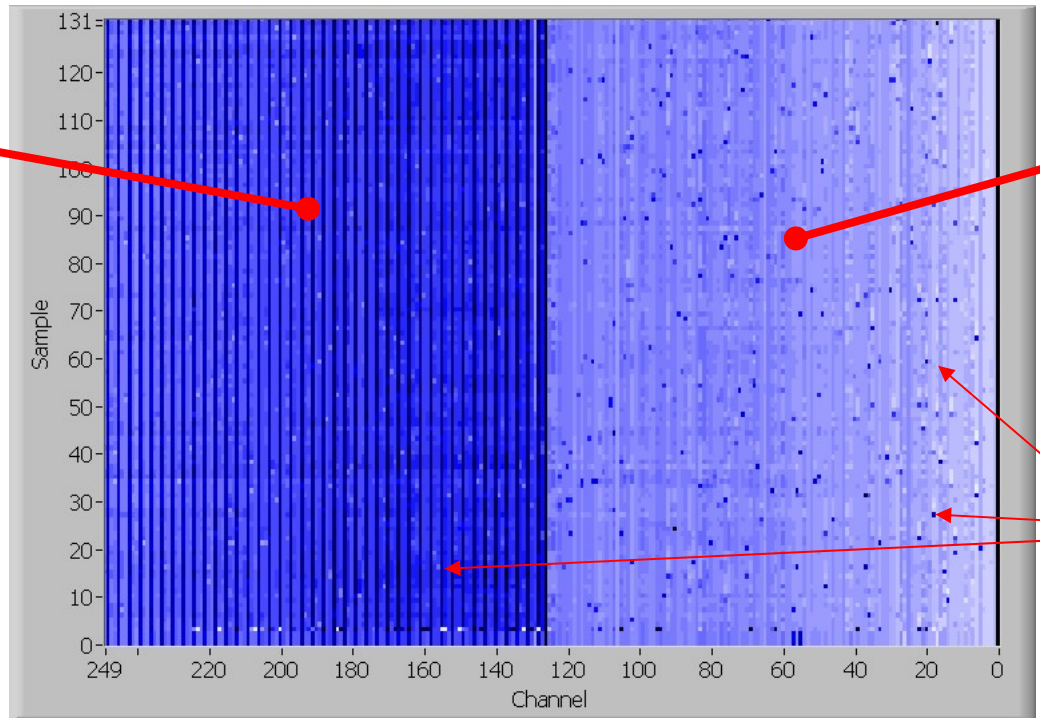




- **Bonding by VTT, Finland**
- **Bump yield very high**
- **Some whole chip failures**
  - ***Not fully understood***

Testing Results

Charge Amplifiers
(inverting)



Voltage Amplifiers
(non-inverting)

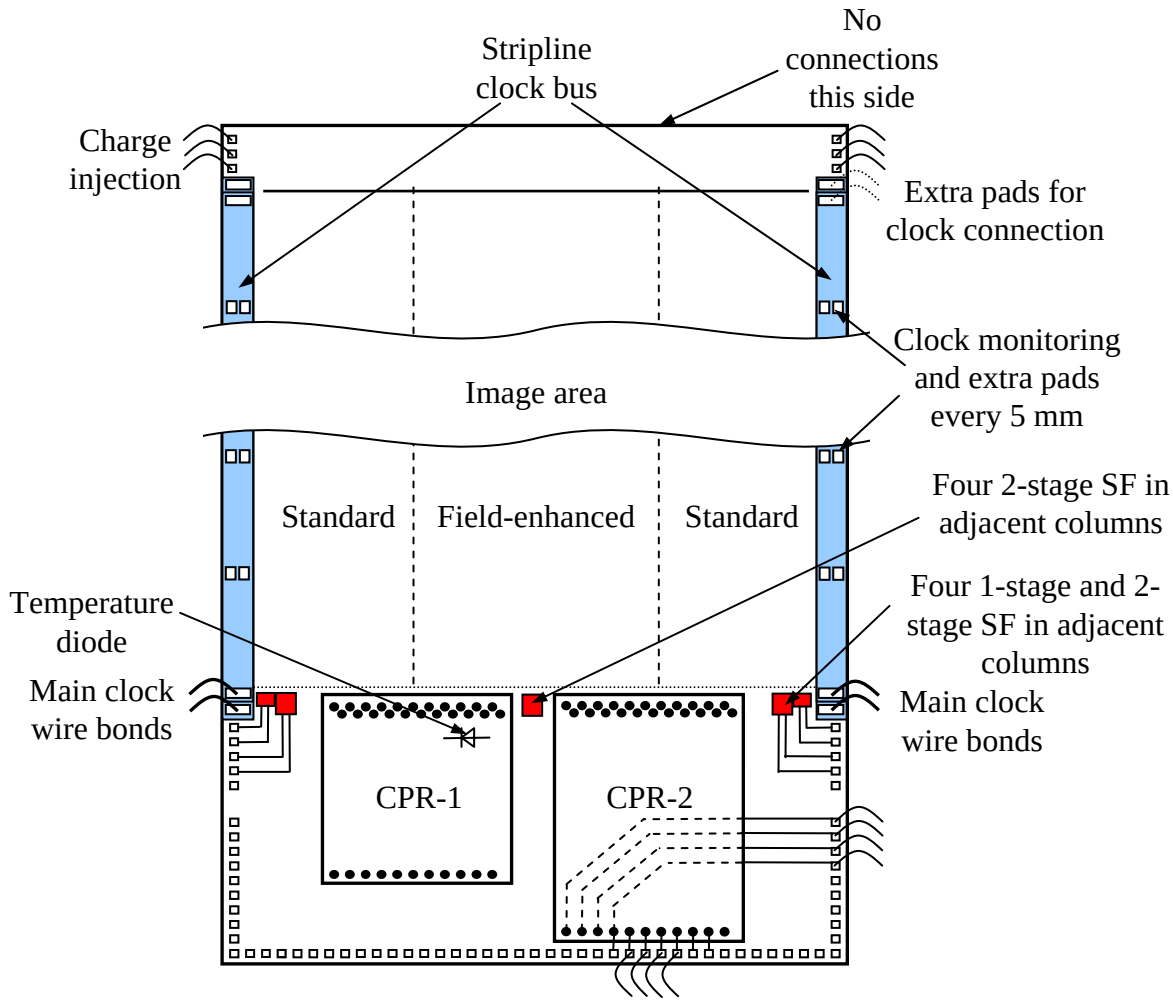
6 keV X-rays

- Charge amplifiers work
- Negligible noise from CPR
- *Column parallel operation demonstrated*

- No signal in ~20% of voltage channels
- Readout chip very sensitive to timing and bias issues
- Gain decrease towards centre of chip

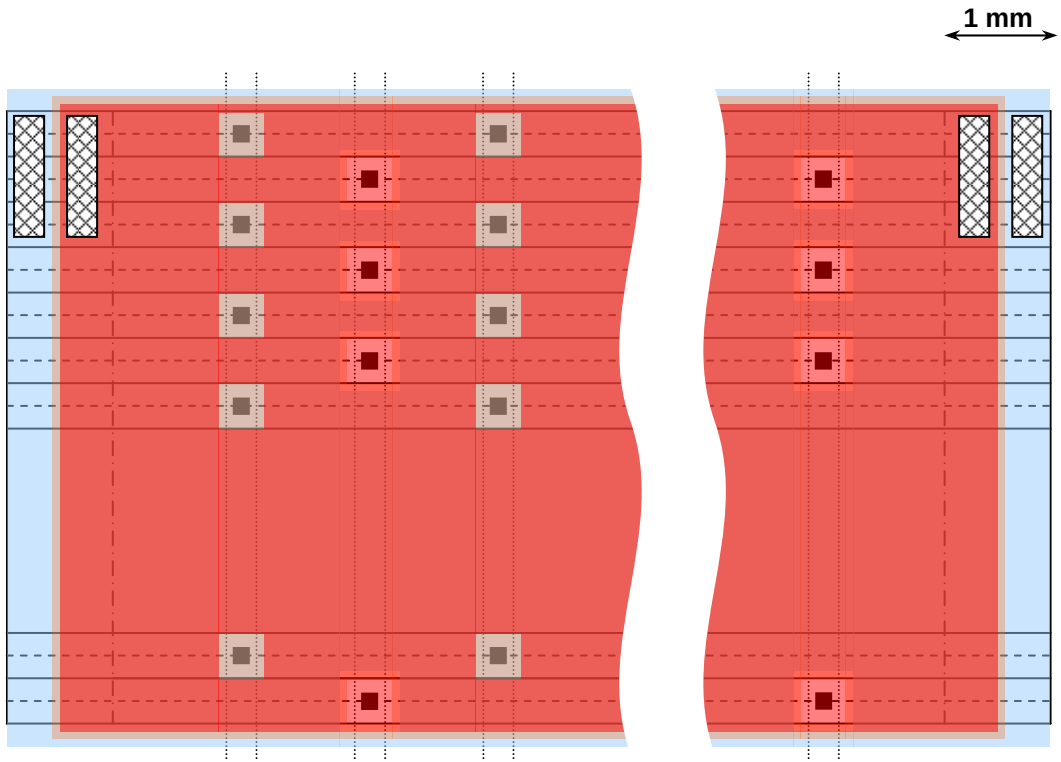
Next Generation: CPC2

- **Double metal now available from E2V**
- **Symmetric clock design**
- **“Busline-free” option**
- **Compatible with old and new readout chips**

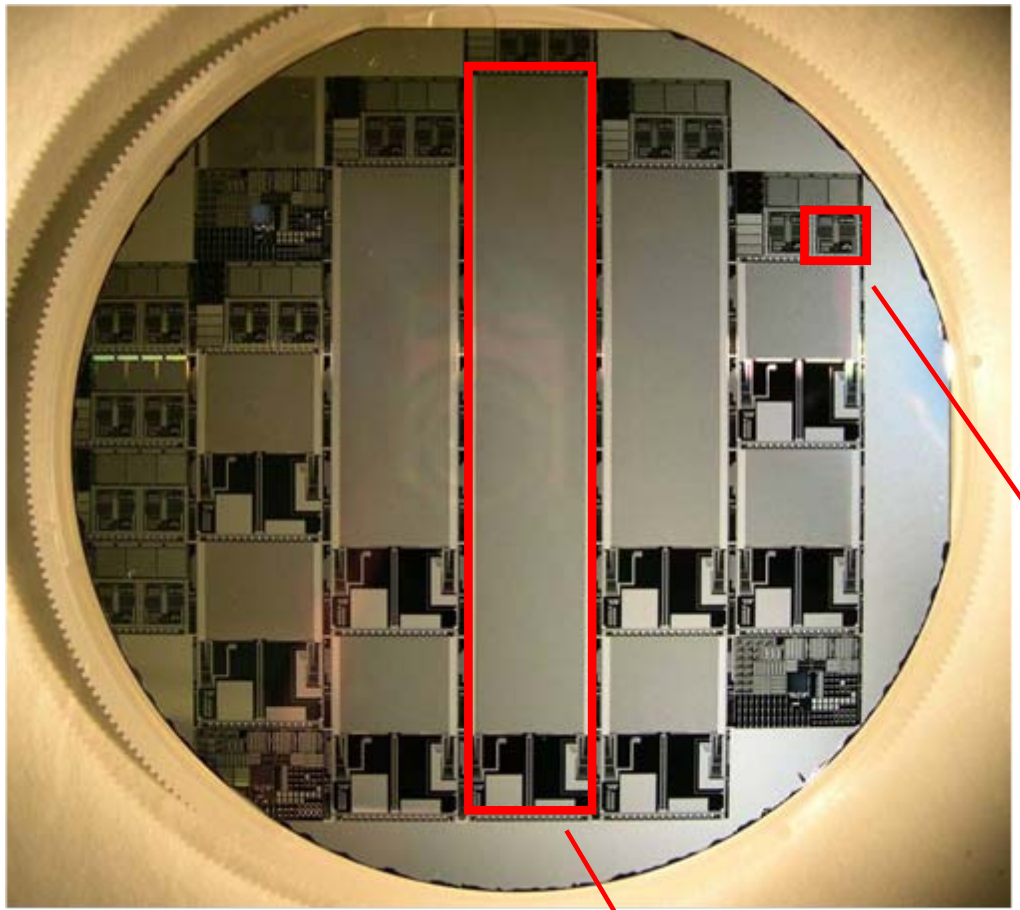


Busline Free CCDs

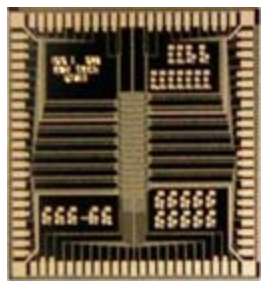
- **Clock signals transmitted via distributed drive planes**
  - **Faster propagation**
  - **More uniform**



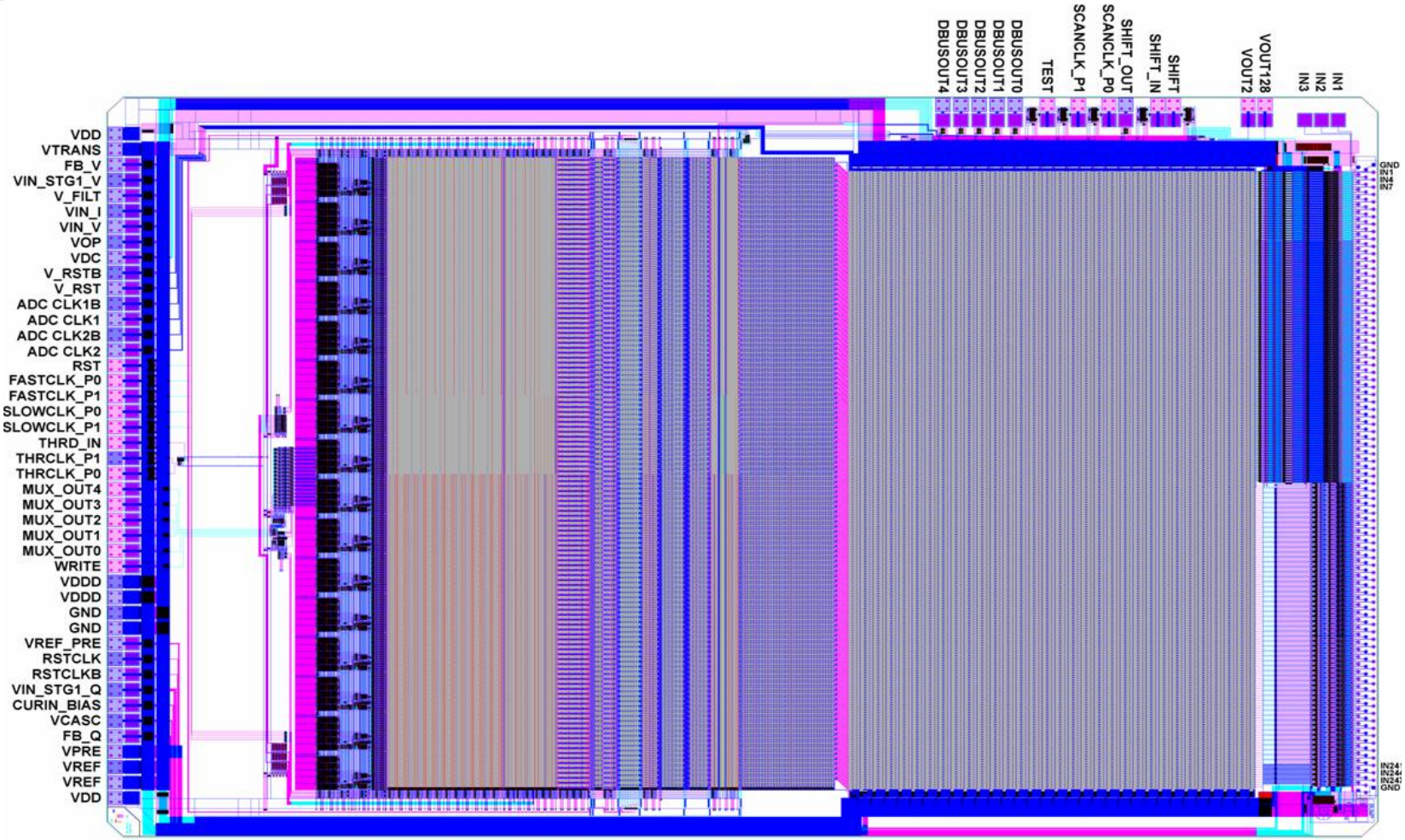
CPC2 Production



- **Dedicated batch at e2v**
- **3 sizes of CPCCD**
  - ***up to 92 mm active length***
- **First wafers in DC probing**
- **Wafers include 16×16 ISIS**

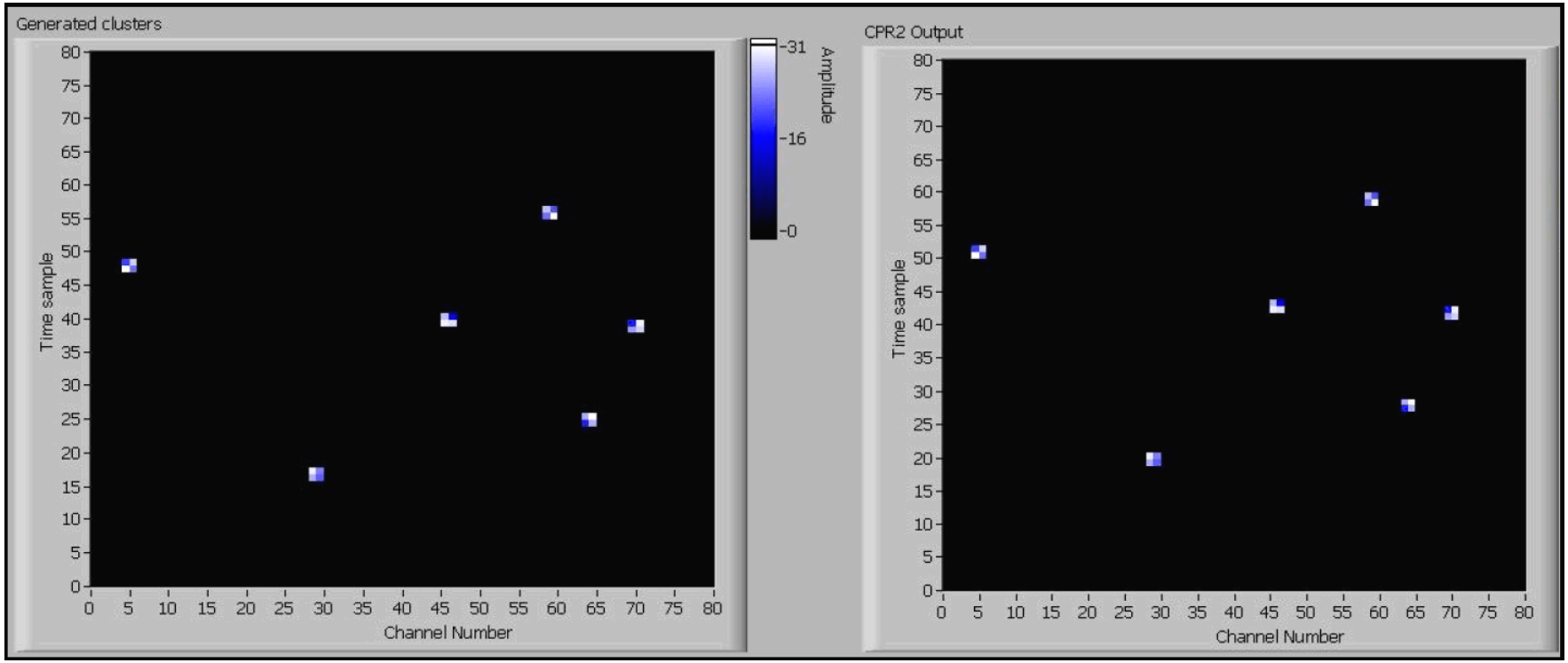


Next Generation: CPR2



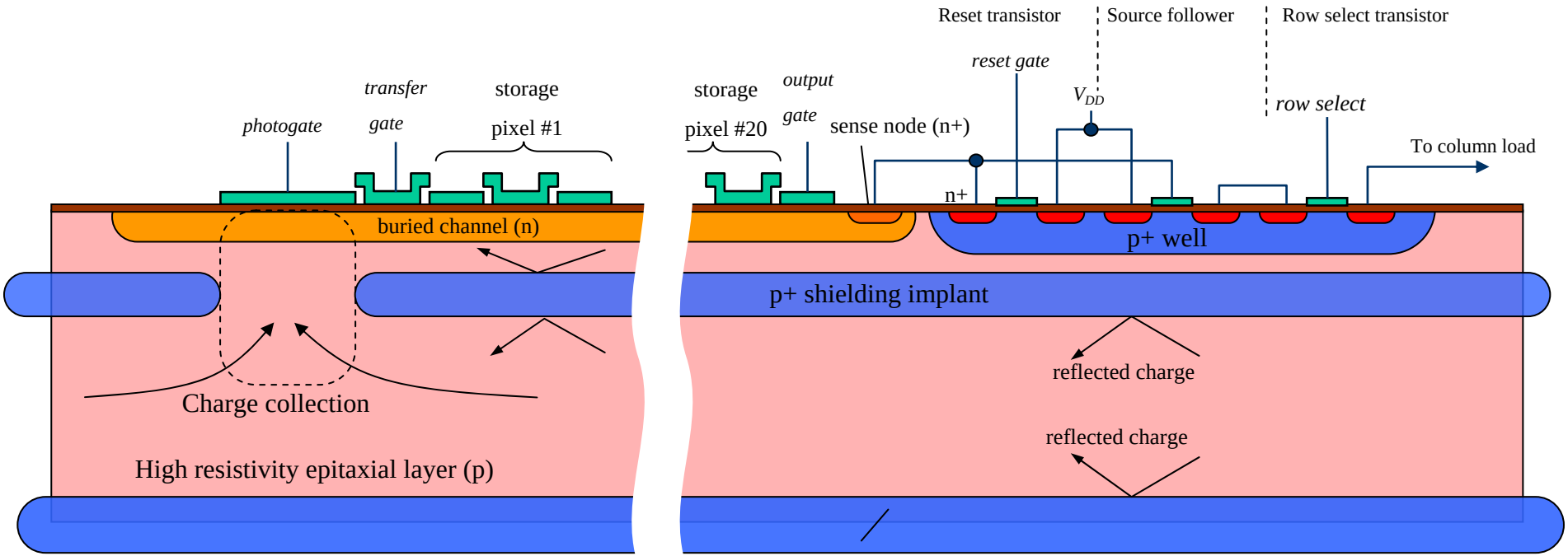
Output | **Sparsification & Multiplexing** | **Cluster Finding** | **Binary Conversion** | **5-bit ADC** | **Preamp Input**

CPR2 Testing

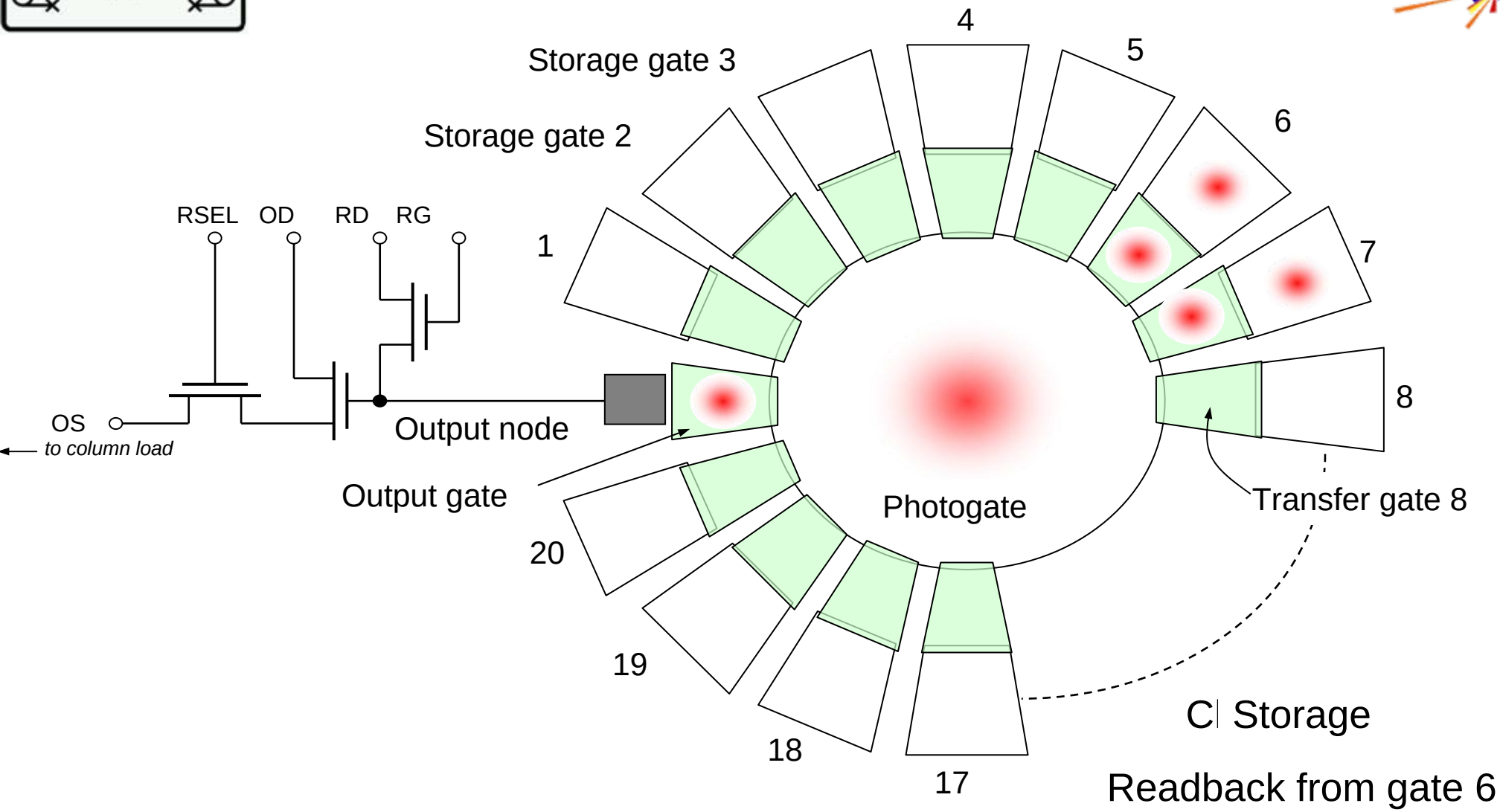


- **Cluster finding logic and sparse readout**
- **Improved amplifiers and ADCs**
- **Increased robustness**

In-situ Storage Imaging Sensor



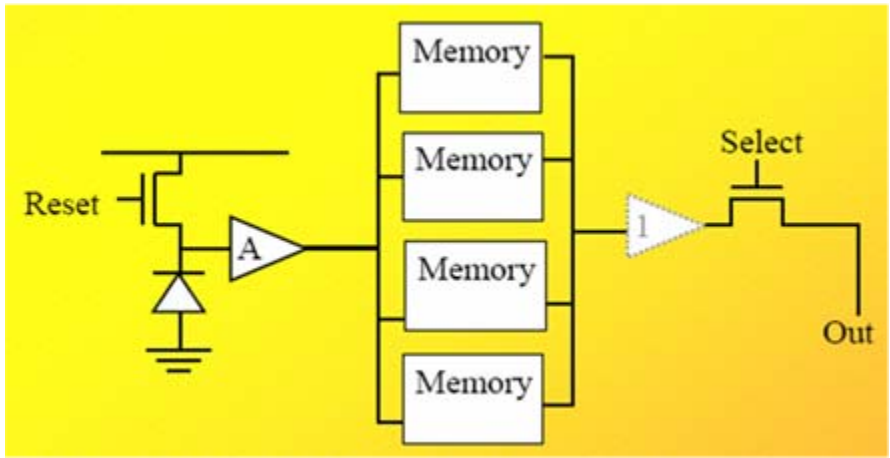
- **Orders of magnitude increased resistance to RF**
- **Much reduced clocking requirements *(readout ~1MHz)***
- **Combination of CCD and CMOS technology on small pitch**

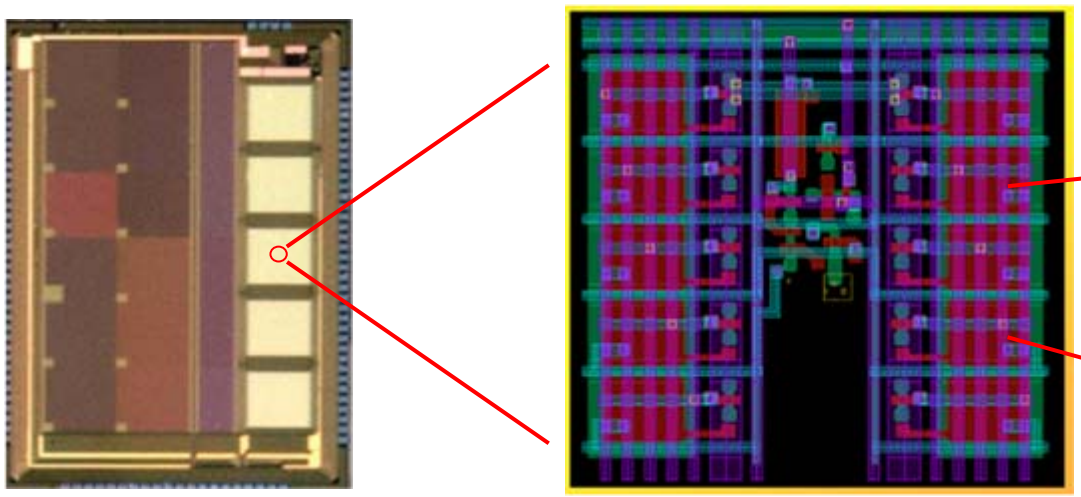


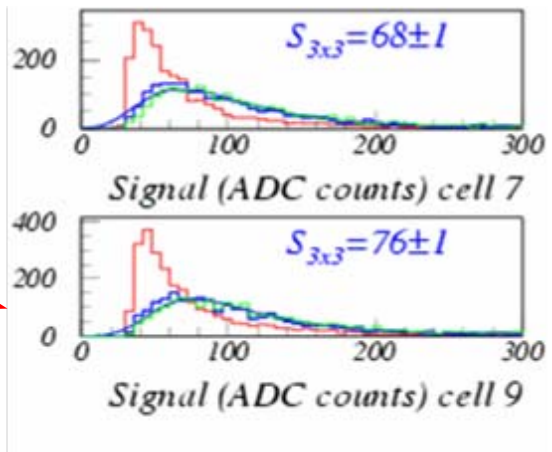
Idea by D. Burt and R. Bell (e2V)

Flexible Active Pixel Sensors

- **FAPS architecture**
  - **First prototypes in 2004**
  - **Pixels 20x20 μm²**
  - **3 metal layers**
  - **10 storage cells per pixel**







Detector Plans

- **Test and evaluate 2nd generation CPCCD & readout**
- **Test first ISIS prototypes**
- **Design 3rd generation CPCCDs and drivers**
- **Develop ISIS and FAPS test structures**

Summary

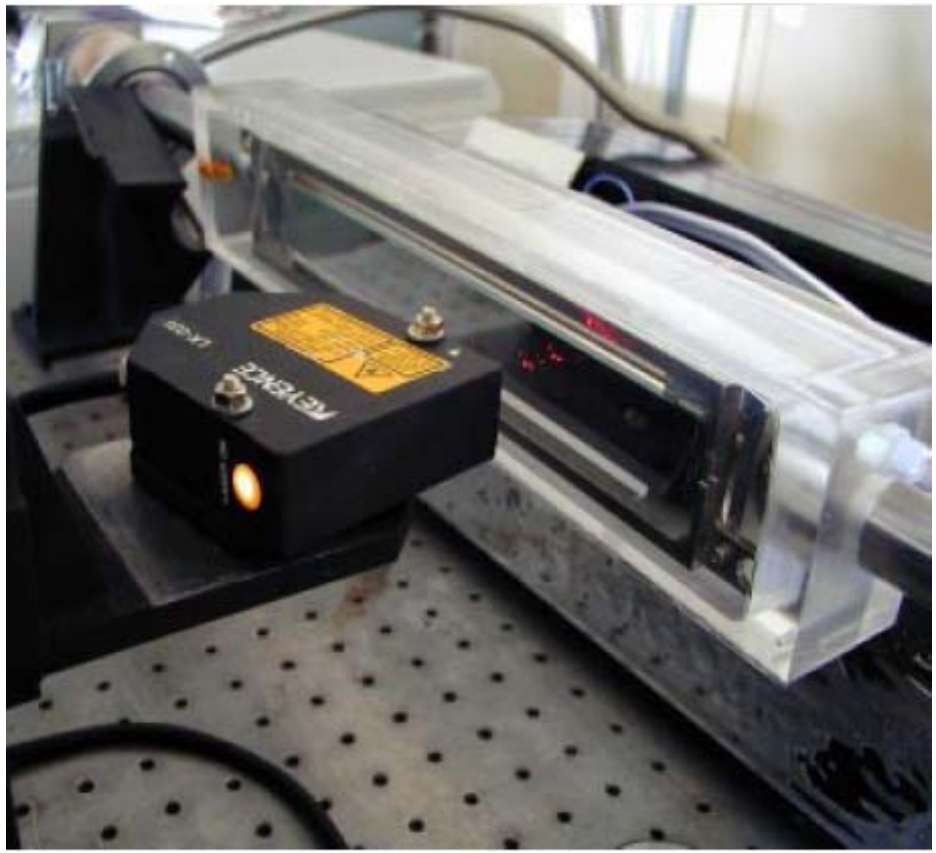
- **First generation sensors extensively studied**
  - **Column parallel CCD principle proven**
  - **Direct charge output demonstrated**
- **Next generations of sensors**
  - **Detector-scale CCDs, sparsification**
  - **Storage devices**
- **0.1% X_0 ladders seem achievable**
  - **Foams looking promising**

Exciting times ahead!

Backup Slides

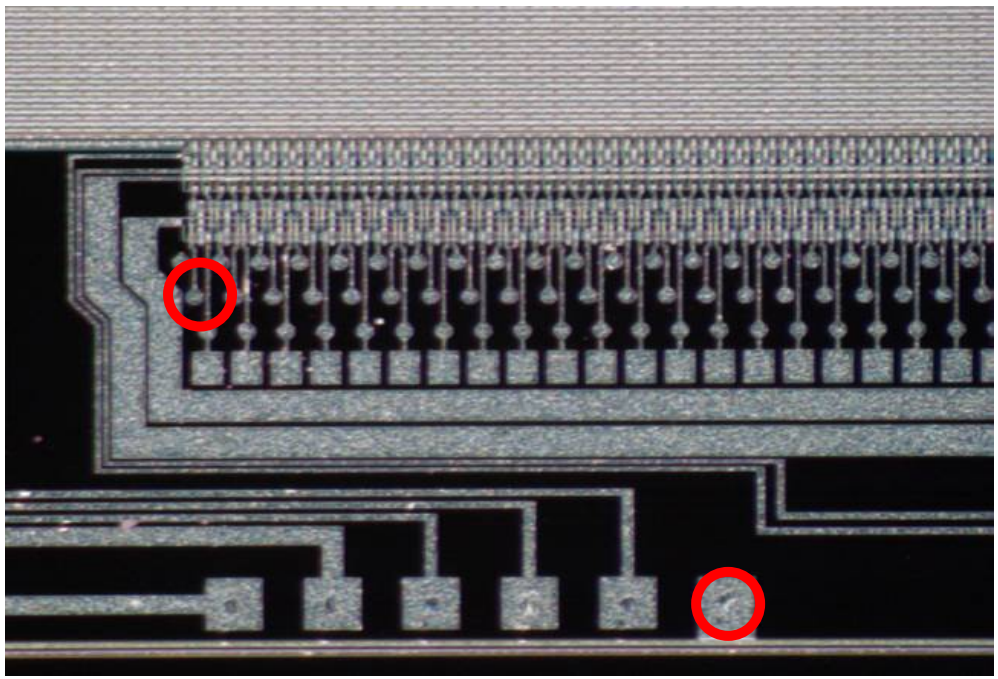
Laser Survey System

- **Laser displacement meter**
  - **Z precision ~ 1 μm**
- **2D motorised stage**
  - **X-Y precision < 1 μm**
- **Ladder in cryostat:**
  - **ΔT ~ 100°C**
- **Fast:**
  - **1D scan < 1 minute**
  - **Scan during cooling**



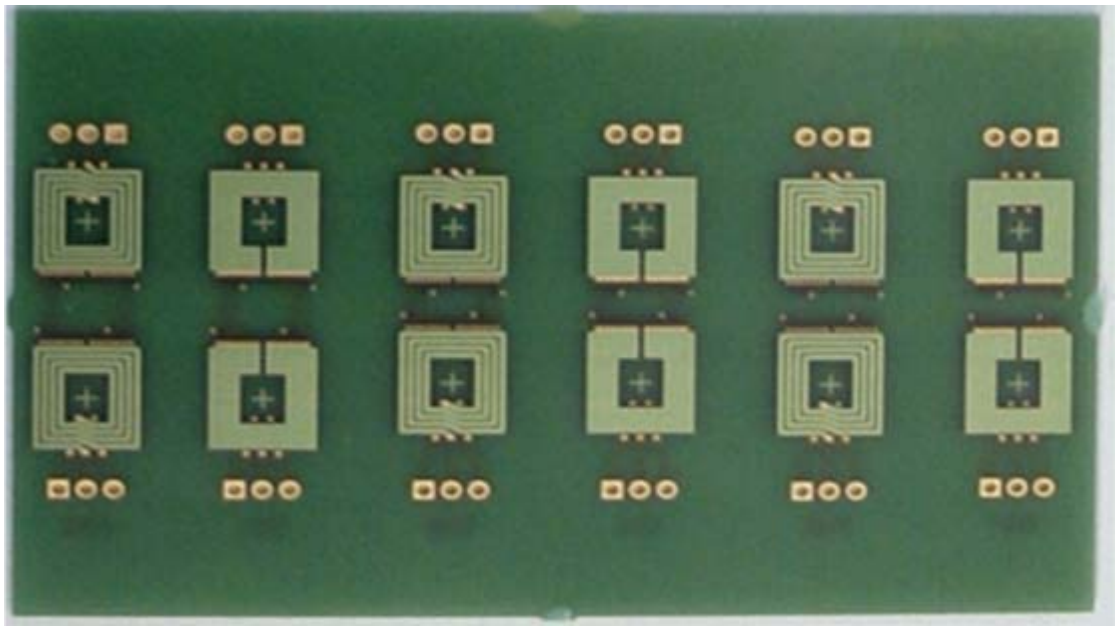
Bumping Failures

- **Short between CCD substrate and chip ground**
- **Possible mechanical damage**



CCD Drivers

- **Clock drivers are a big challenge**
  - **Working on air core PCB transformers**
  - **Long-term solution more likely to be IC with local storage**



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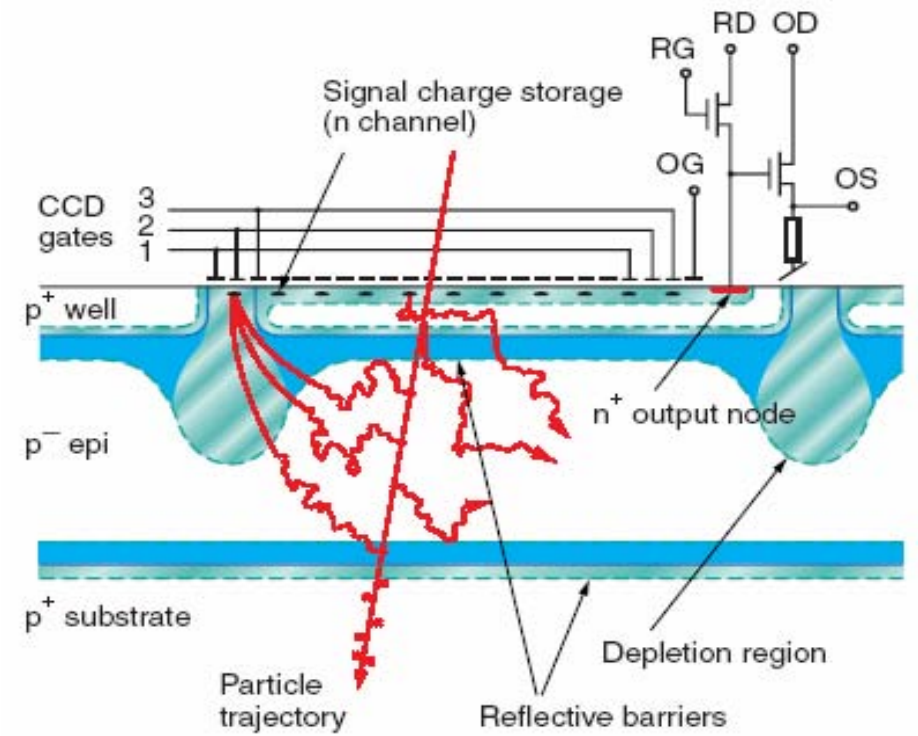

1. **Charge collection similar to CCD or CMOS**
2. **Charge transferred into local CCD array every 50µs**
3. **Local CCD array clocked at 20 kHz**
4. **Source follower for every pixel**
5. **Read out one row at a time**
   - ***Still column parallel***