Silicon Tracker Front-end chip tests and next version:

ongoing R&D at LPNHE-Paris in the framework of the SiLC R&D Collaboration

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ILCW05, Snowmass, August 14-28 2005

Inner and Outer Si-tracker Readout

- **Silicon strips Detector occupancy:**

Outer barrel and end caps layers: **GEANT-based studies: < 1 %**
Inner barrel and end caps layers: **GEANT-based studies: < 5 %**

- **Double & Multiple hit rates:** **Ambiguities to be estimated wrt shaping time**

- **Sparsification/calibration:** ➔ ***On the detector FE***

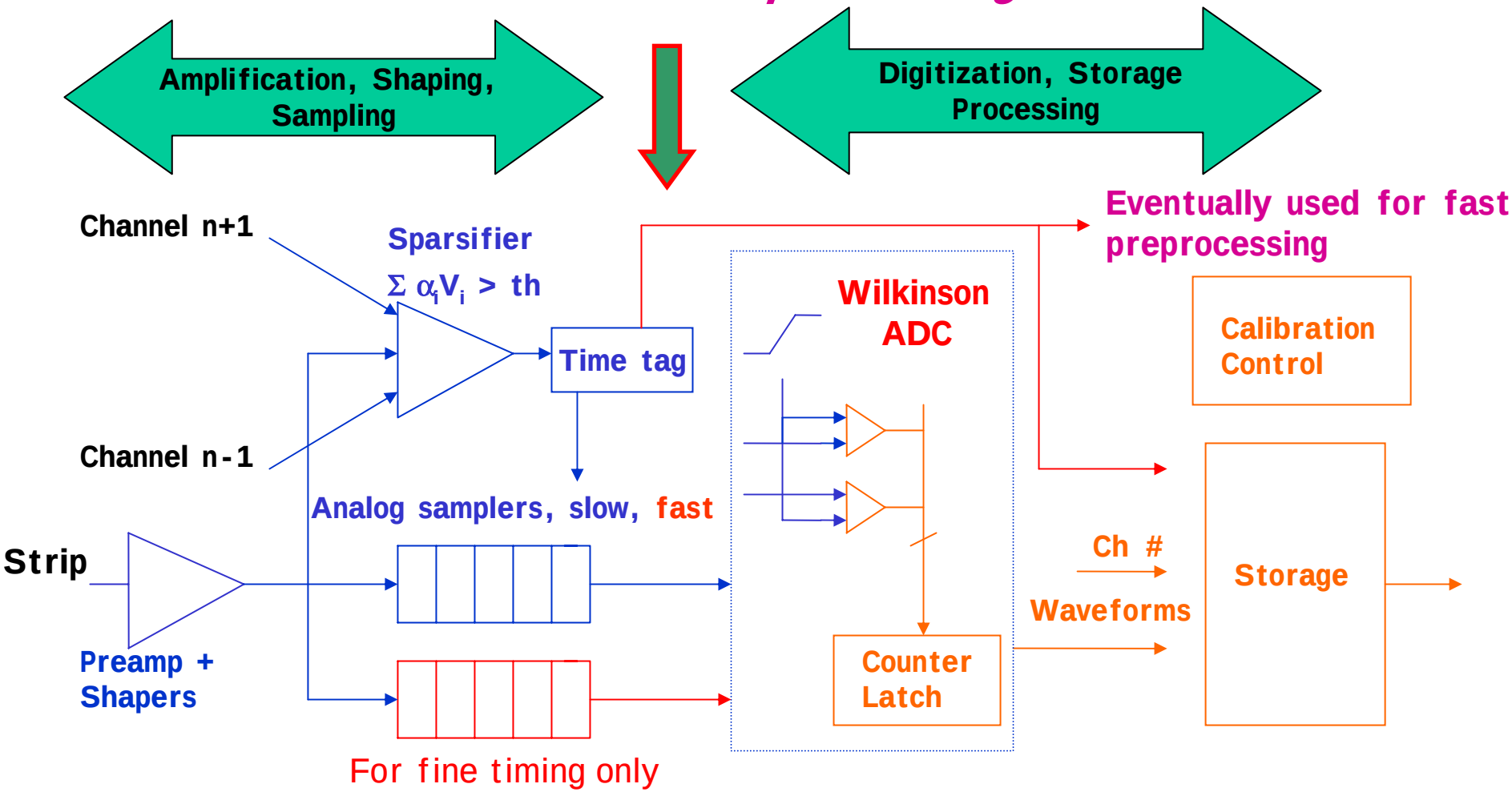
- **Pulse height needed:** **Cluster centroid to improve position resolution to 7–8μm**
➔ ***8-10 bit multiplexed A/D***

- **Timing information** **Included in the FE design. The principle & possible performances are being studied** ➔ ***Paris test bench & simulations***

- **Digital processing for cluster algorithm and fast-track processing algorithm.**
➔ ***Under study while designing FE***

- **Power dissipation studies:** **Present results do not anticipate a major pb**
➔ ***passive (or light) cooling might be achievable***
➔ ***FE Power cycling***

Front-end processing



Charge 1-40 MIP, S/N~ 15-20, Time resolution ~ 2ns

Present technologies

Deep Sub-Micron CMOS UMC 0.18 μm

Future possibilities:

SiGe &/or deeper DSM?

Time-stamping on all layers
(see new chip version)
and fine time resolution
on some layers: under study

Expected Performance for Charge measurements

Gain, noise:

- Preamp + Shaper

Gain 12mV/MIP over 1-45 MIP

280e- + 10.5e-/pF @ 3 μs

Power:

- Preamp + Shaper + Sparsifier

Preamp: 70 μW Shaper: 160 μW Sparsifier 50 μW

Sampling for the charge measurements: 100 - 200 μW (?)

(caveat: power dissipation depends on the design and speed of the analog samplers, currently under study)

- Shared ADC

ADC: 10 bits, 2-3 μs, 110 μW

Total: 500 – 600 μW/channel

Expected Performance for time measurements

Two different designs must be considered wrt the time measurement to be achieved:

- **Fine time measurement (~ 2 to 5 ns)**
- **Time stamping (order of 30 to 50 ns)**

Preamp + shaper + sampling have to be designed accordingly.

This will impact on the expected performance on power dissipation and technology choice.

Currently under study both on Lab test bench, and on simulations

Power Switching

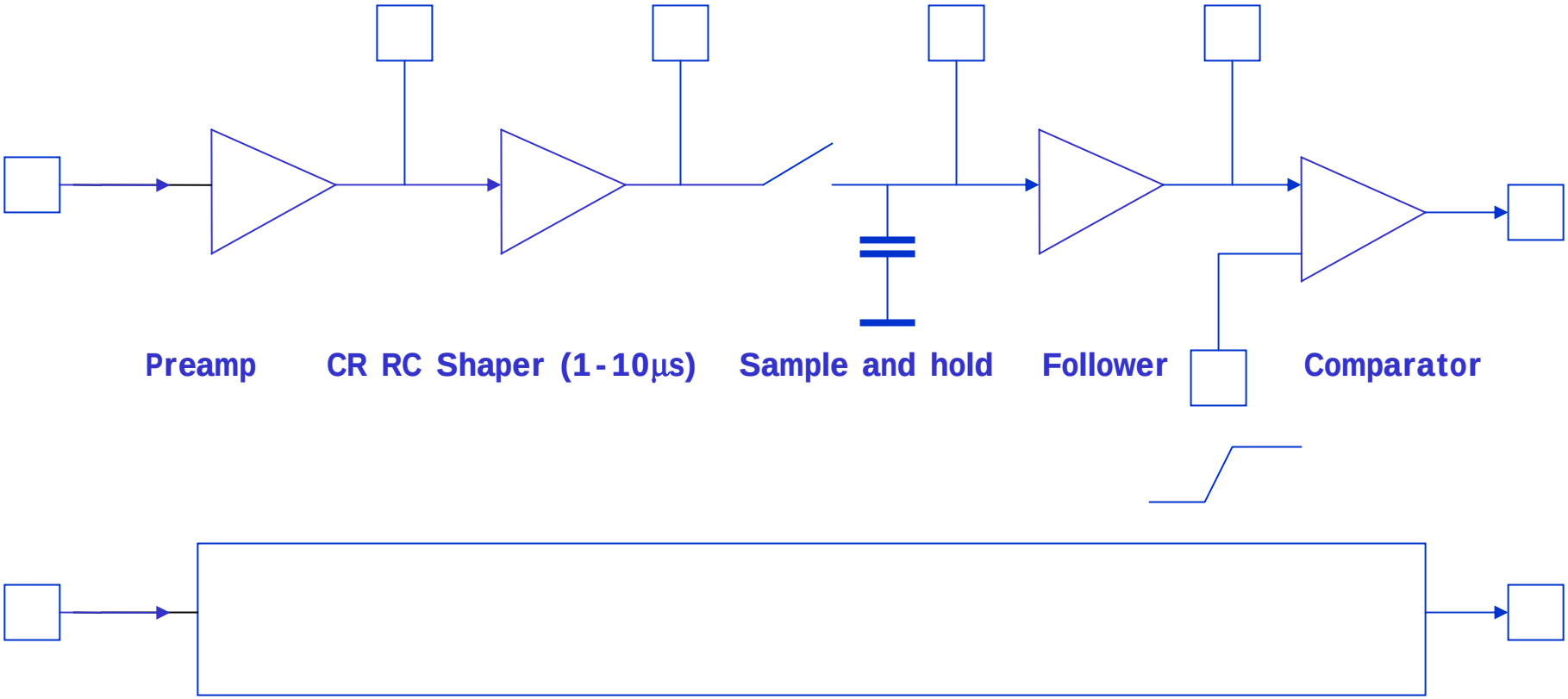
Power Switching (if OK with other sub-detectors)

If analog is running during collisions only:
e.g. 1.2/100 duty cycle and 2 10^6 channels, then:

Total: **500 10^{-6} x (4-10) 10^6 x 1.2/100**

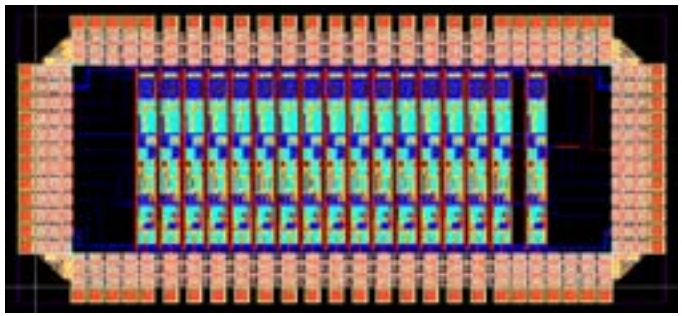
2 - 5 KWatts ***(24 – 60 Watts)***

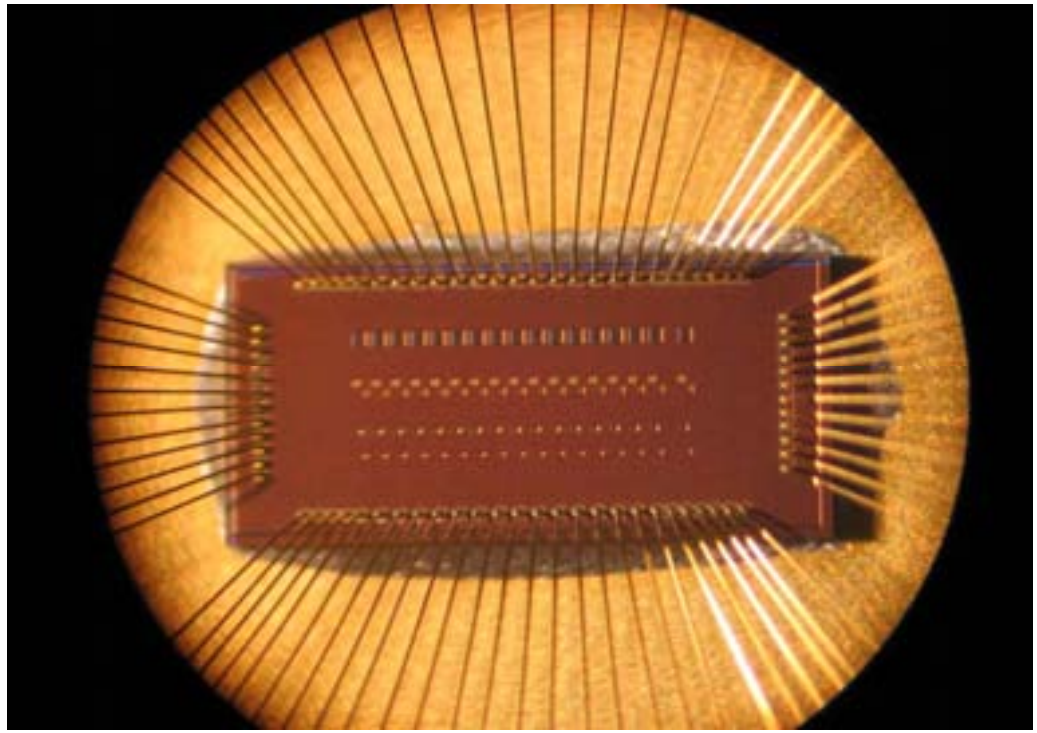
Test Chip



Technology CMOS UMC 180nm

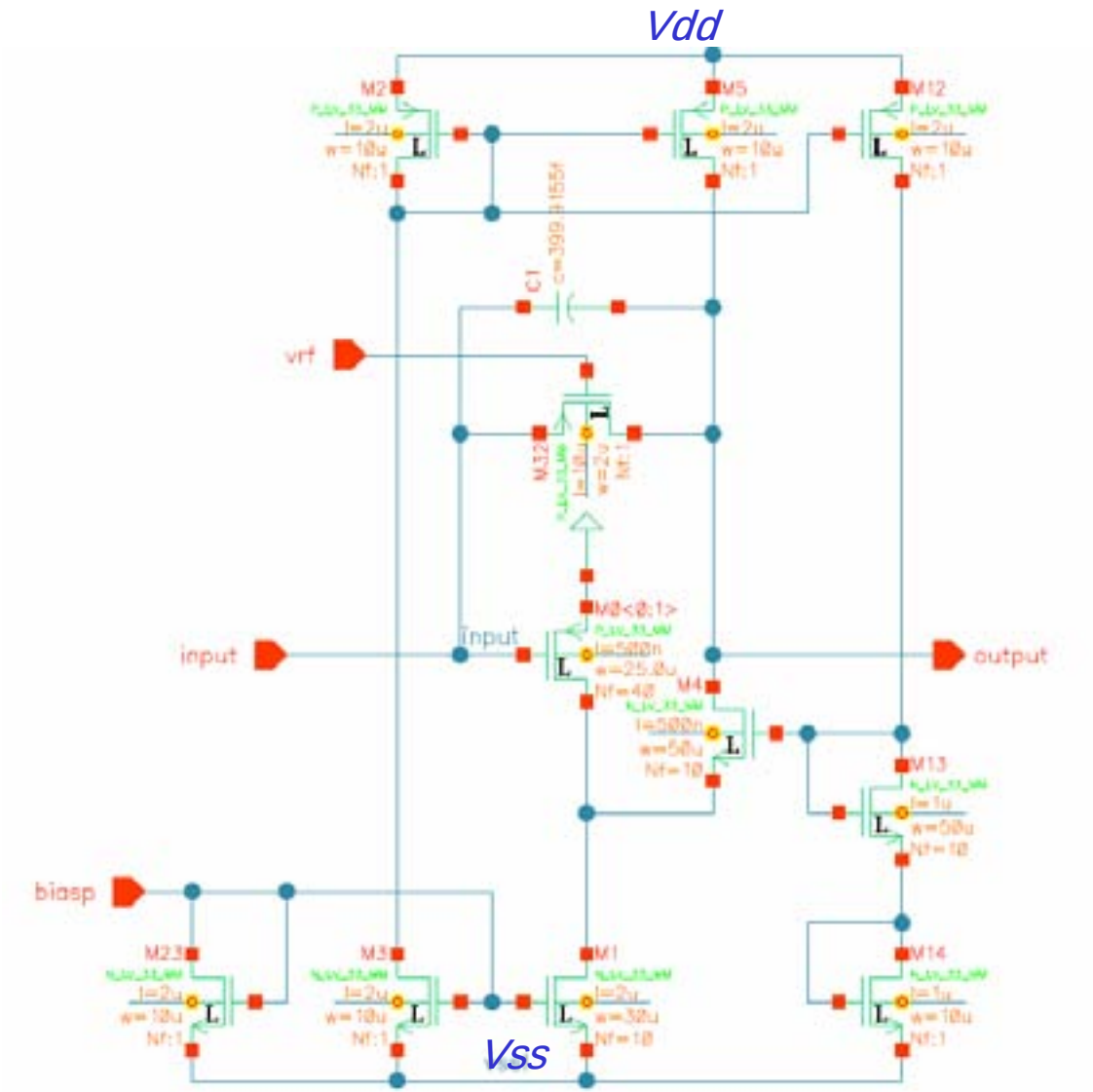
Layout and Silicon

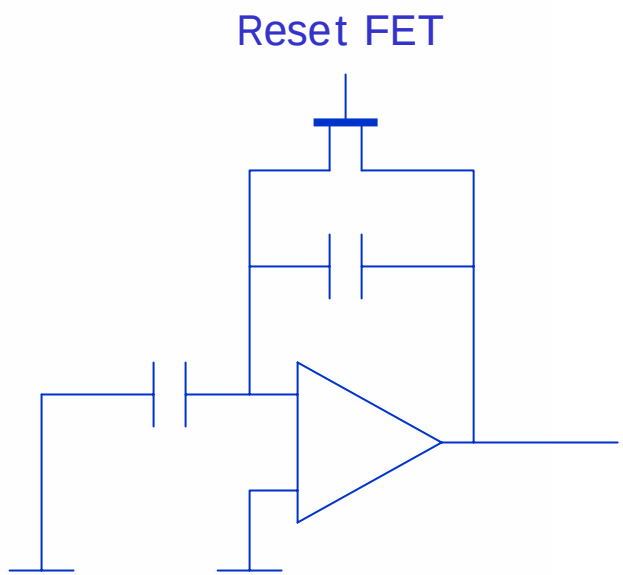




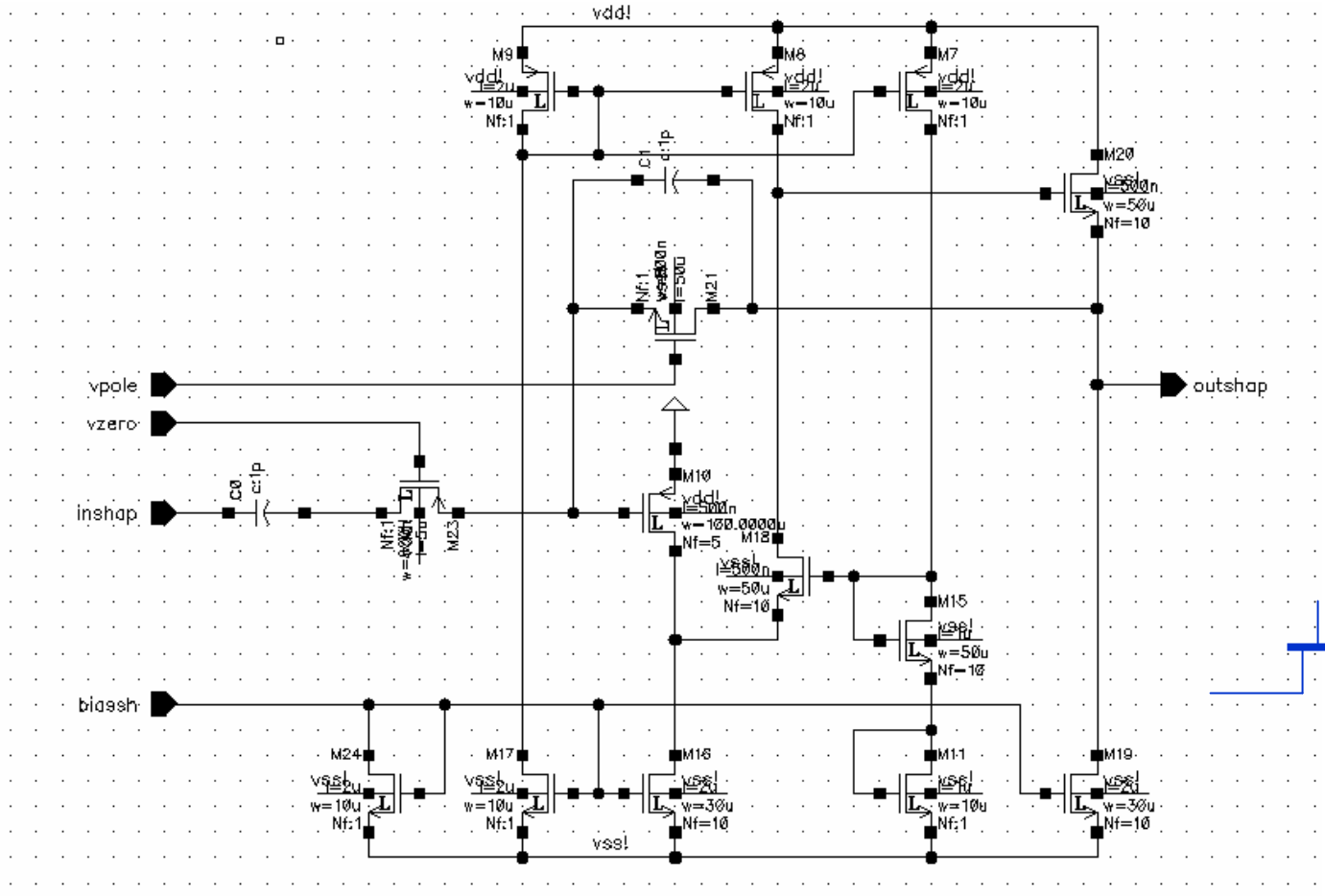
16 + 1 channel UMC 0.18 um chip (layout and picture)

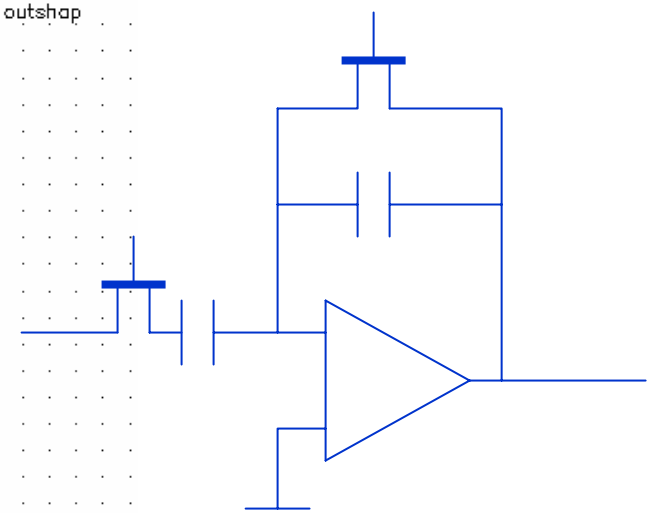
Preamp schematic block diagram





Shaper schematic block diagram





Overall Results. Preamp

9 chips (over 20) tested (ongoing work, with continuous feedback between simulations and measurements to understand the results)

-> One failure: On chip #8, comparator does not work.

Preamp:	-	Gain:	8mV/MIP	as expected: OK
	-	Dynamic range:	50 MIP	as expected: OK
	-	Linearity:	+/-1.5%	expected: +/-0.5%
				now well understood:

Transistor used as a resistor non linear with voltage:

Action to be taken: Optimize transistor or use resistors if not too large

- Noise @ 70 μW power, 3μs-20μs rise-fall times:

498 + 16.5 e-/pF 490 + 16.5 e-/pF expected OK

Conclusion: The design is fine and will be used for the next version

Overall Results, Shaper

Shaper: - Peaking time: **2-6 μs tunable peaking time presently achieved**

1-10 expected (but not really needed)

Action to be taken:

To define carefully the needed peaking time range:

- **shorter peaking time range e.g. to 0.5-2μs (preferred one)**
- **longer peaking time: 2-6μs looks reasonable.**
- Gain: **1.2 @ 3 μs OK** - Linearity: **6%, 3.5% simulated**

Action to be taken: use true resistors

- **Frequency response: 6 MHz bump ~ 650 e- added noise**

(details see below), now understood

Action to be taken: change RC networks values

- Noise @ 3 us shaping time and 70 μW power:

measured 584 + 10.1 e-/pF (6 MHz digital filtered)

274 + 8.9 e-/pF expected

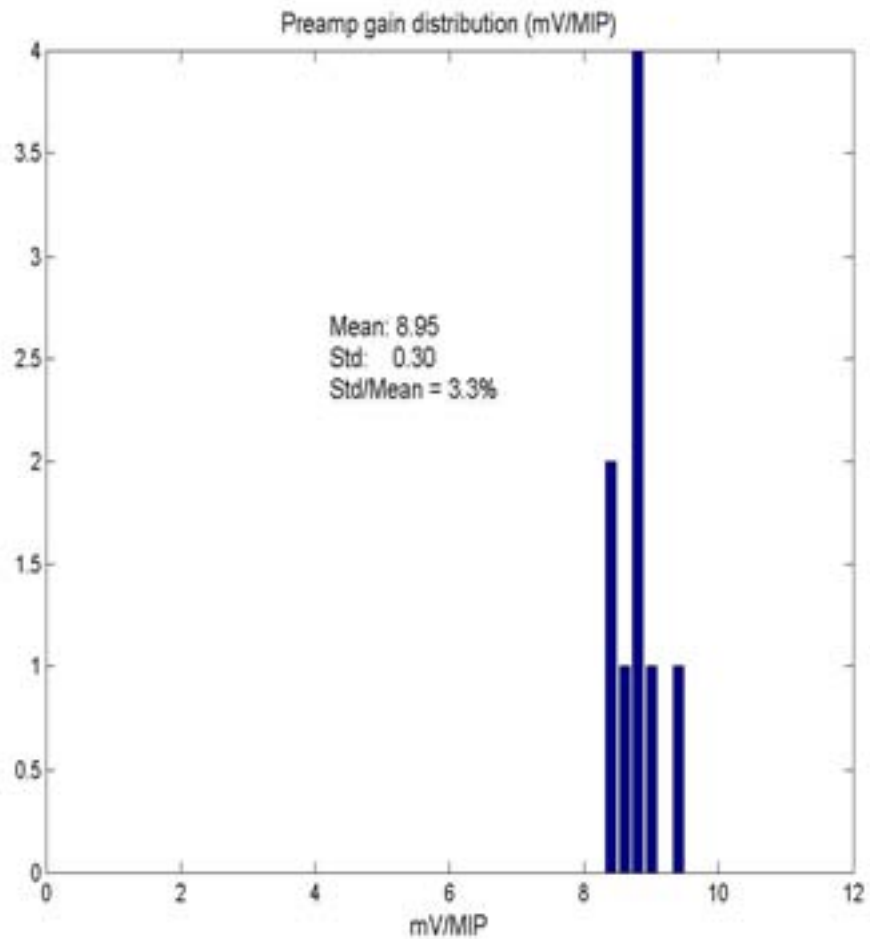
Action on shaper noise: use true resistors

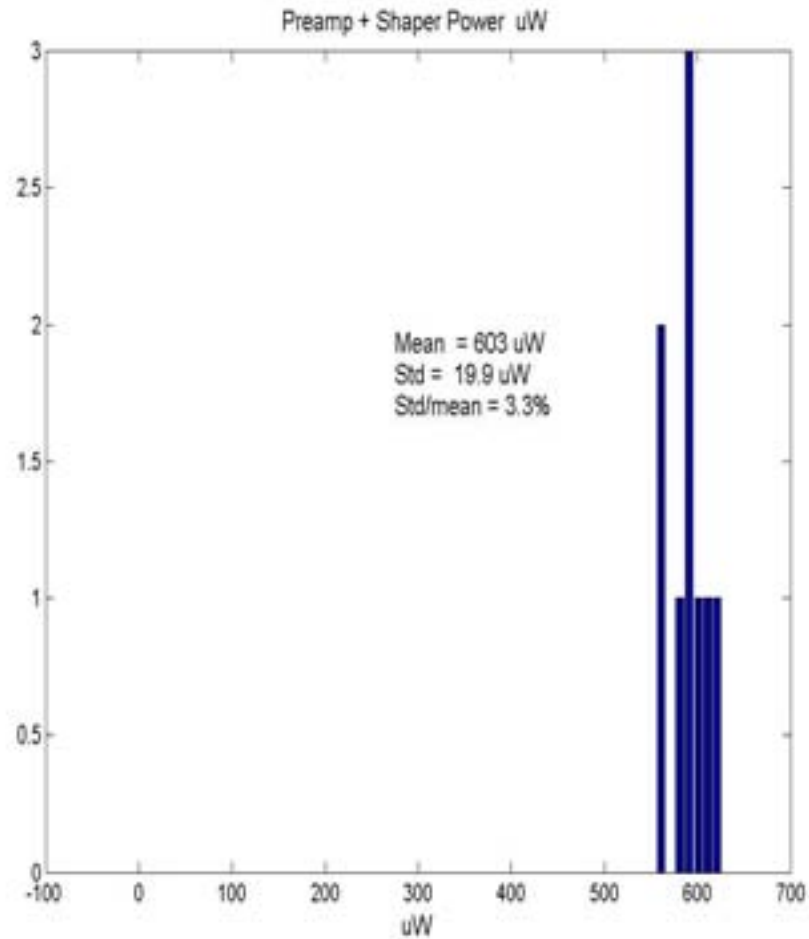
Overall Results, Sample and hold and Comparator

Sample and hold: **OK**

Comparator: tests in progress (V_t spreads critical at 12 mV/MIP)

Process spreads (same multiproject wafer)



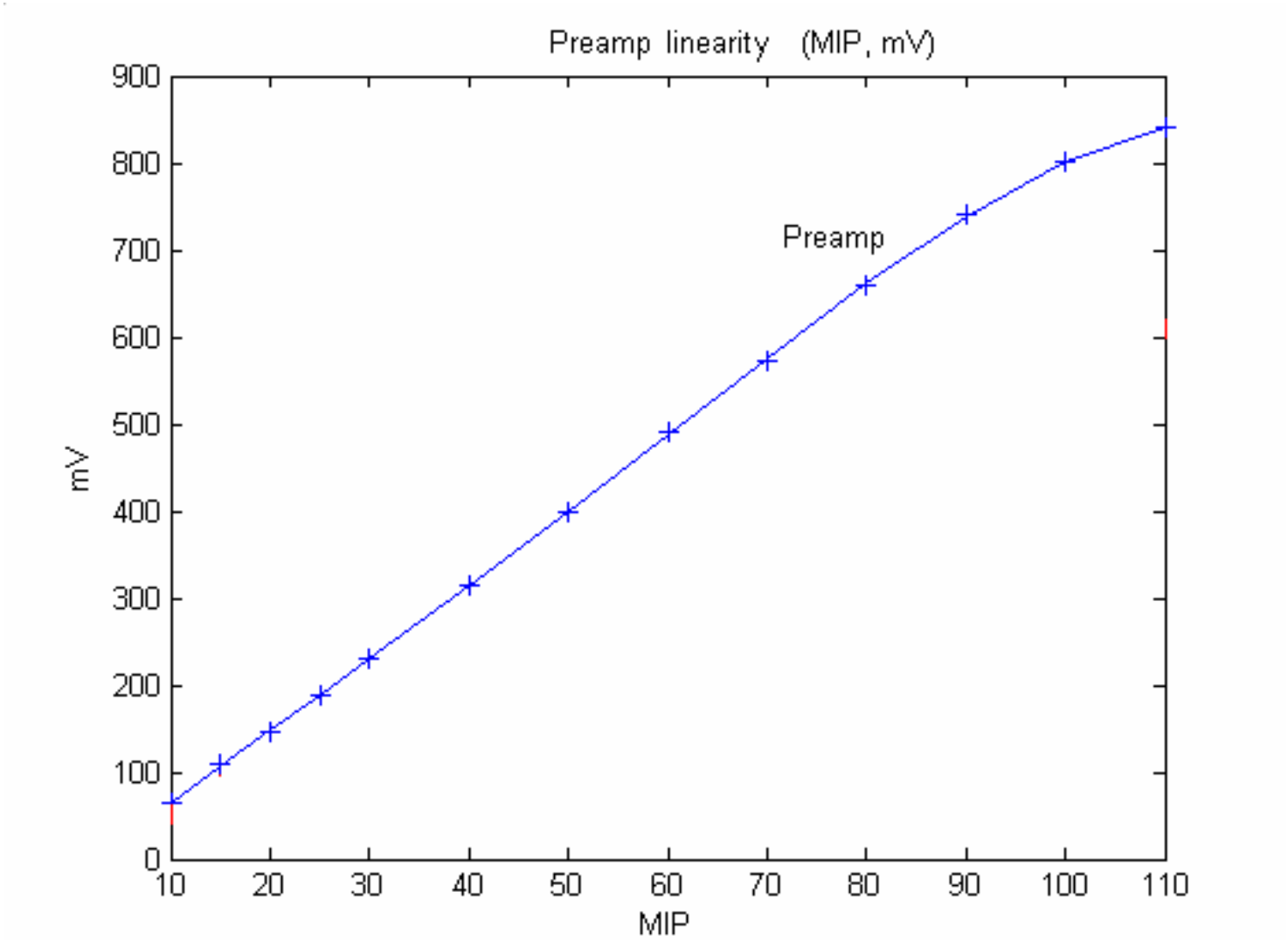


Preamp gain distribution

(Preamp + shaper) power distribution

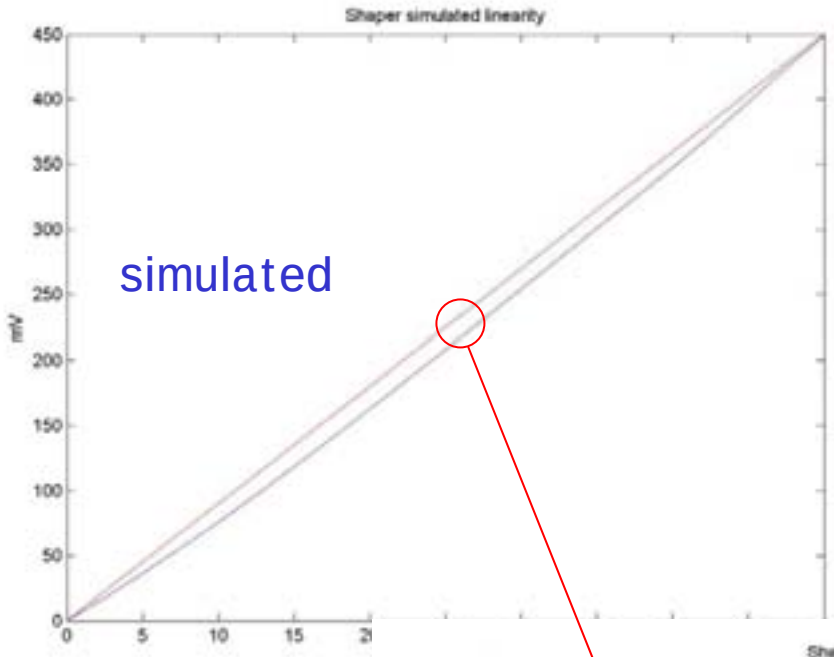
Process spreads: 3.3 % quite good

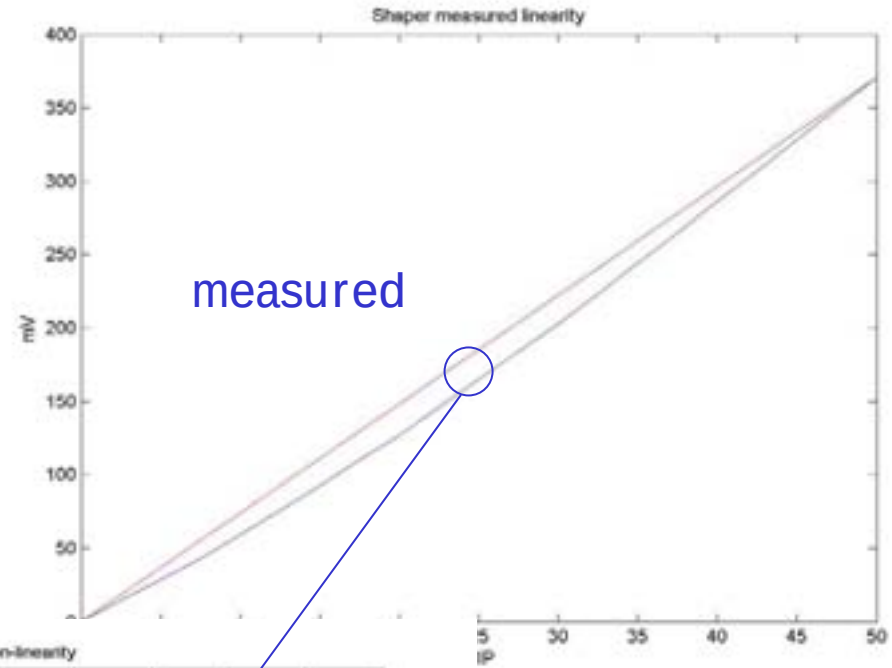
Preamp linearity

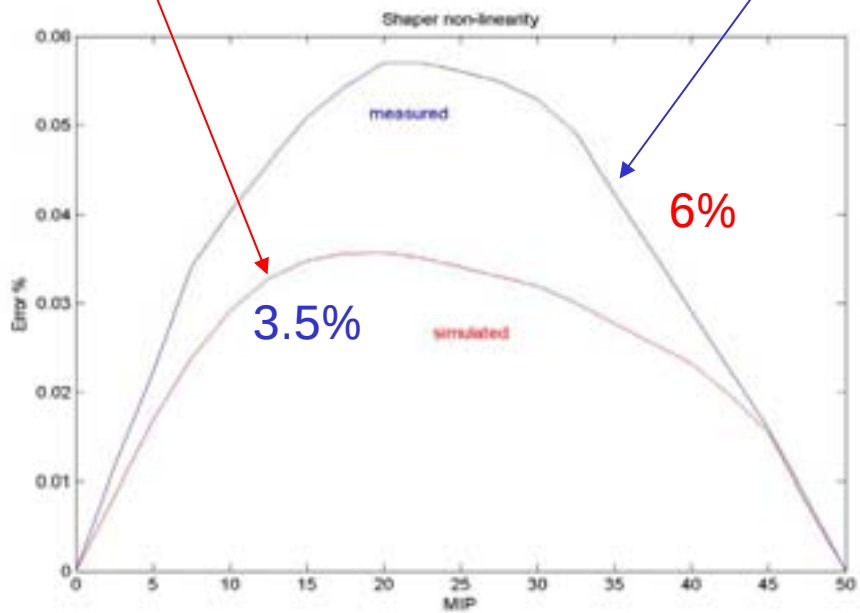


Non-linearity = +/- 1.5% (+/- .5% simulated)

Shaper linearity

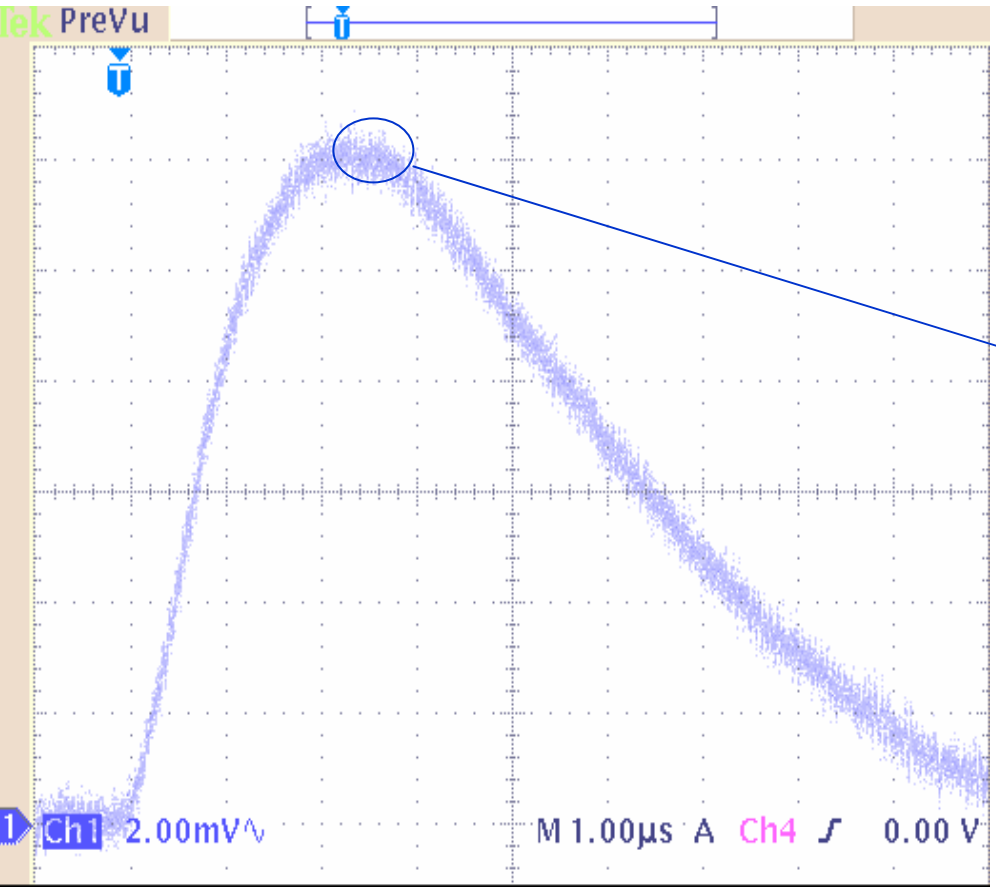


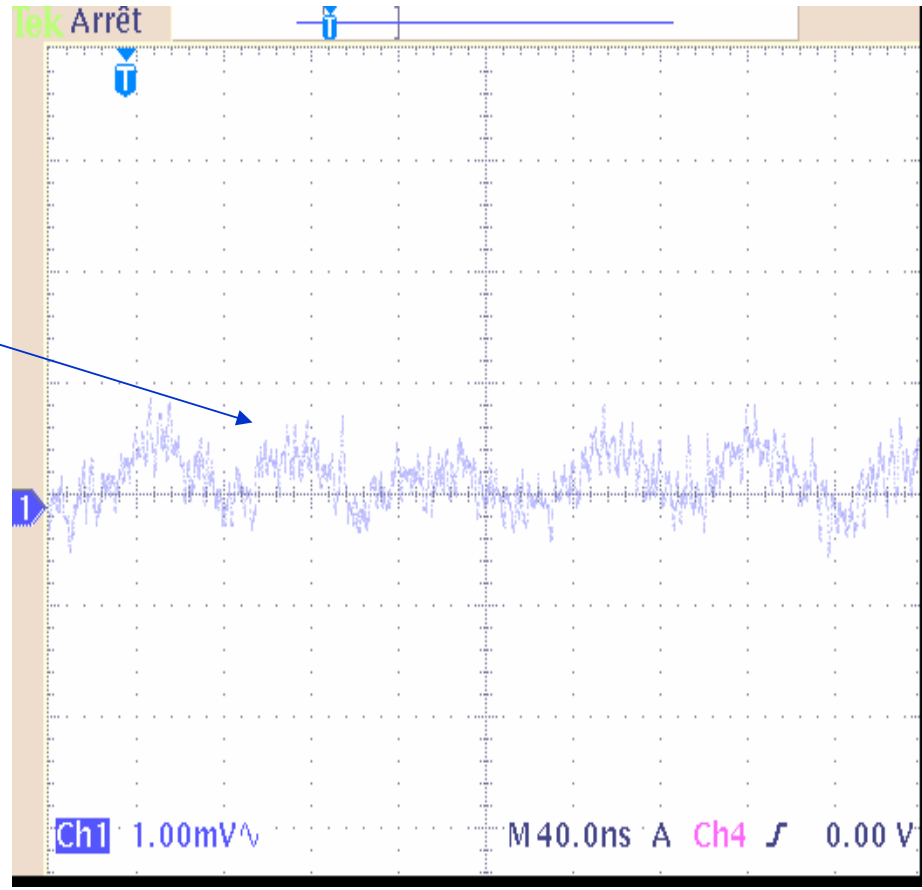




6% instead of
3.5 simulated

Measured Shaper output

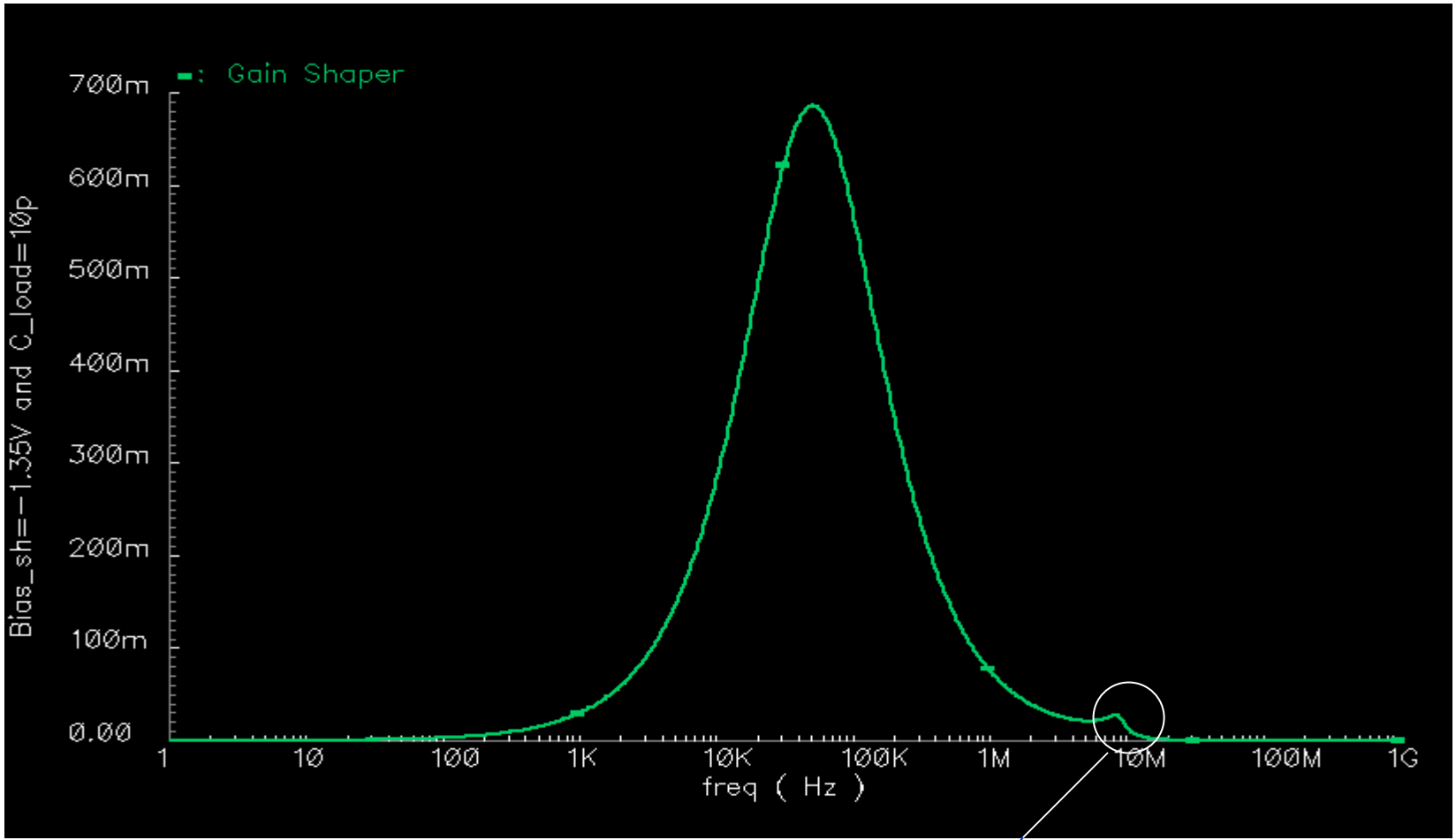




Waveform is as expected

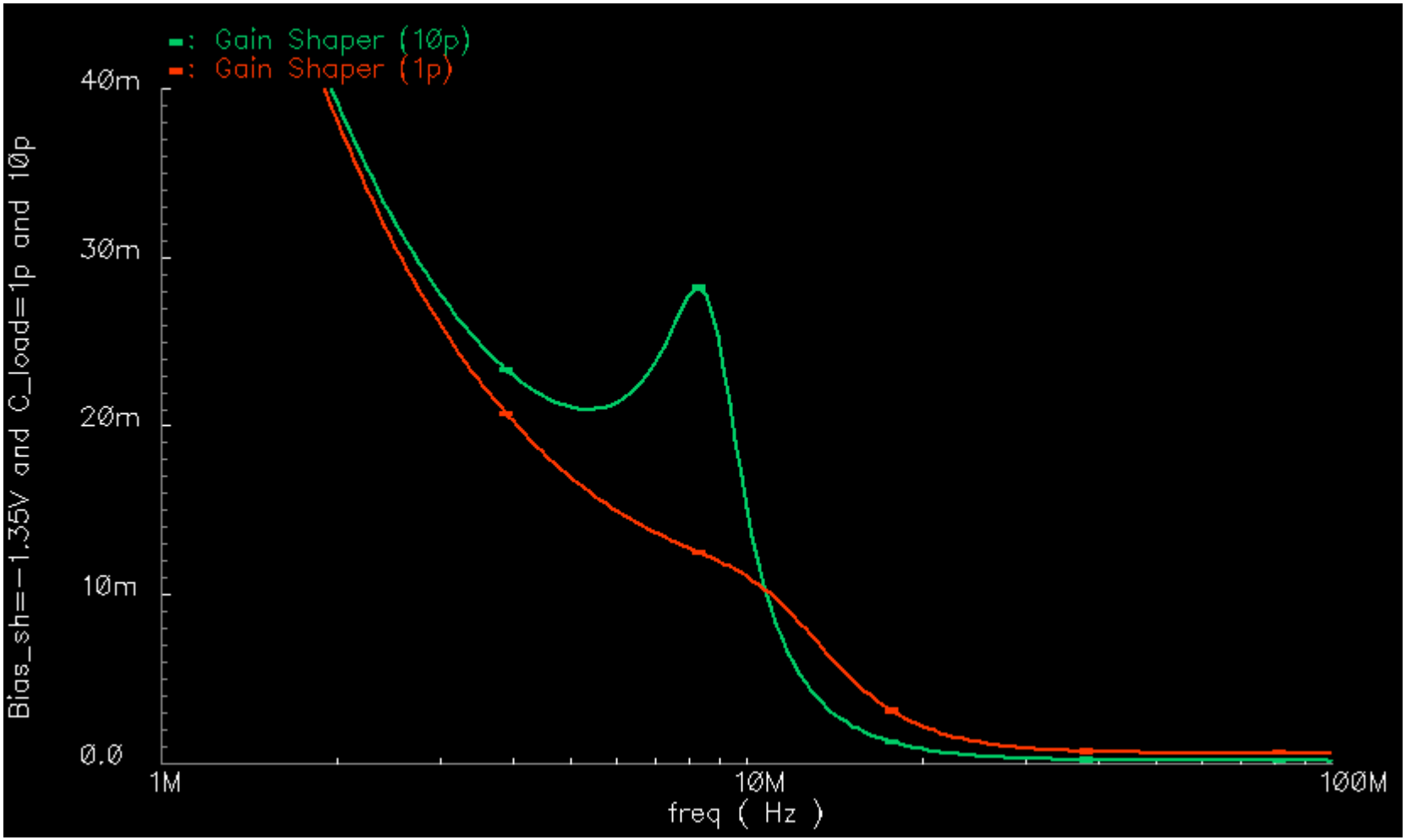
6 MHz oscillations at the shaper output

Simulated Shaper frequency response



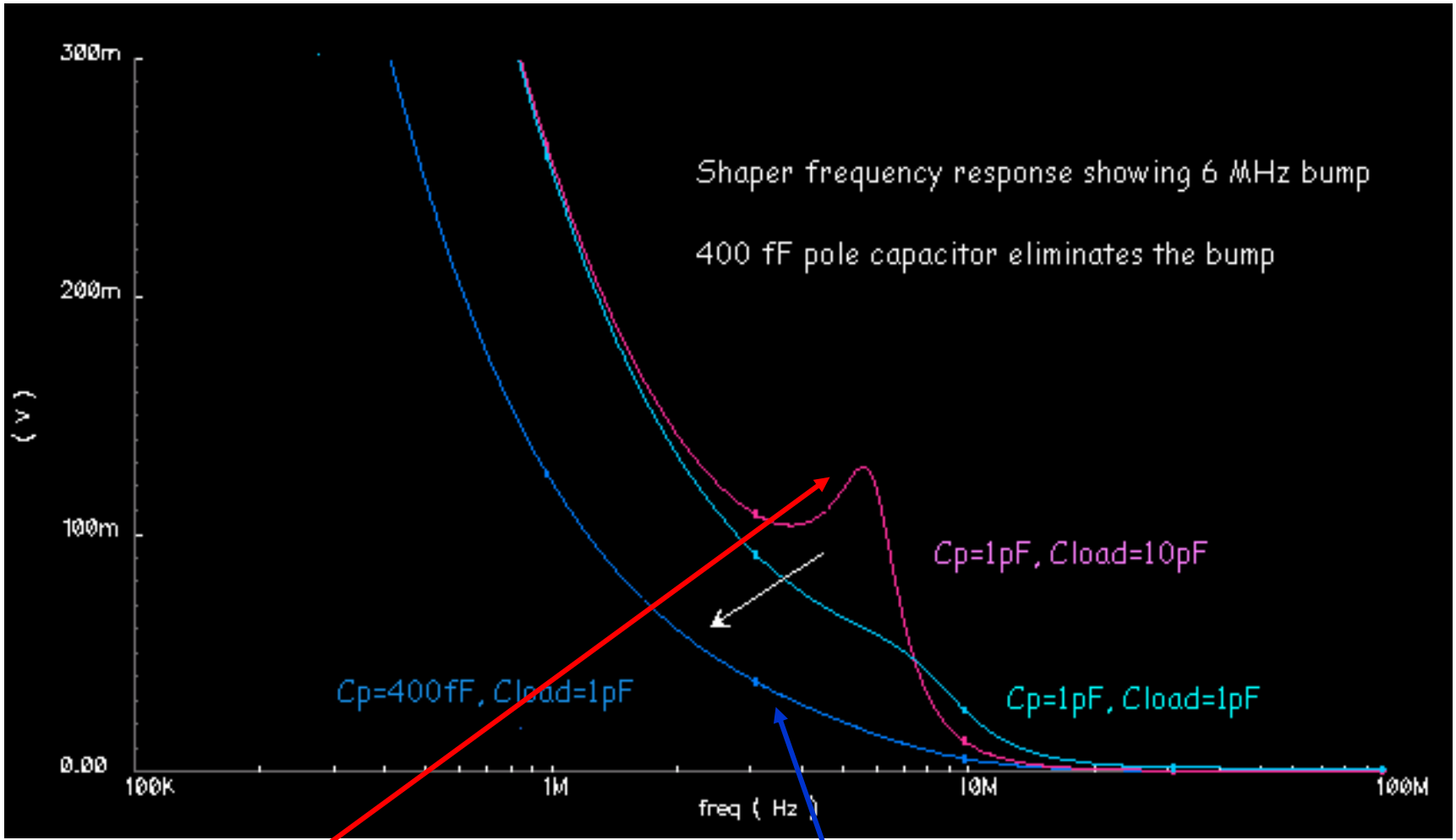
6 MHz bump at the shaper output when loaded with 10 pF

Simulated Shaper frequency response @ 10, 1 pF load



No bump with the actual Sample and Hold cap (1 pF) Parasitics ?

Simulated Shaper frequency response



Simulated bump with 10 pF load cap
Due to non extracted parasitics ?

Move C_{pole} value from 1pF to 400 fF solves the problem

Another possible issue: DSM transistors leaks ?

Two situations:

- **Gate-channel due to tunnel effect (can affect noise performances)**
- **Through channel when transistor switched-off (only affects large digital designs)**

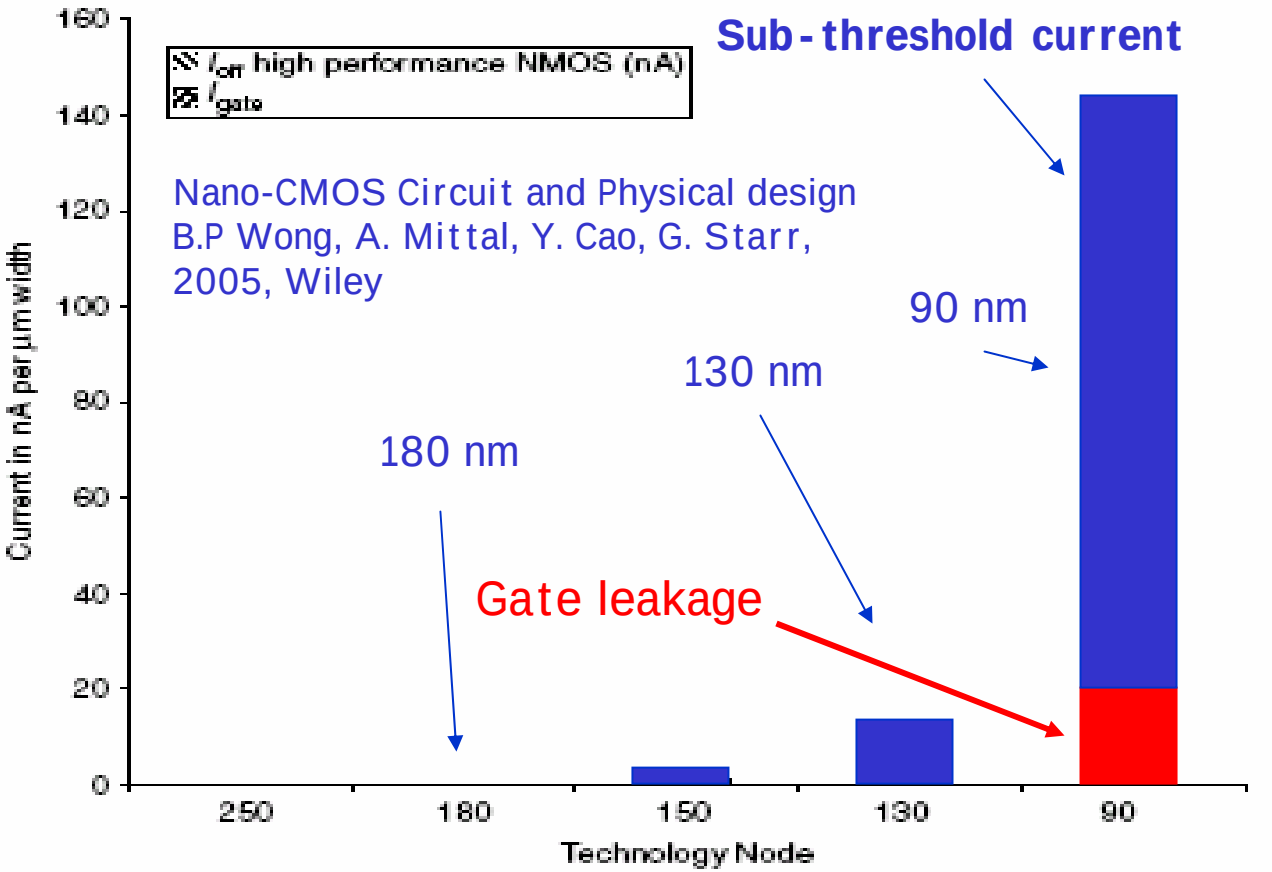


Figure 1.2 I_{gate} and subthreshold leakage versus technology.

As expected from this picture, no gate leakage noise is measured in our 180nm chip
Likewise, at 130nm, no gate leakage is expected.

To give an idea:
If there were 1 nA/µm it would give 8000 e- noise in our design !

Tests results summary

Ongoing development of thorough tests and deeper systematic understanding and characterization of the functioning of the 20 chips delivered in this first foundry.

Currently 9 chips tested over 20.

First conclusion: the process is quite reliable:

- Only one failure (not working comparator)
- Process spreads of a few %

Preamplifier works according to specs

Shaper: **waveform is as expected: OK**

Observed 6 MHz bump **(we know how to cure it)**

Linearity can be improved

Comparator to be tested

The first run delivered functional chips in a relatively new (in our field) DSM technology. The results are encouraging and we are learning a lot in the ongoing debugging task. It is instrumental for the design of the next version

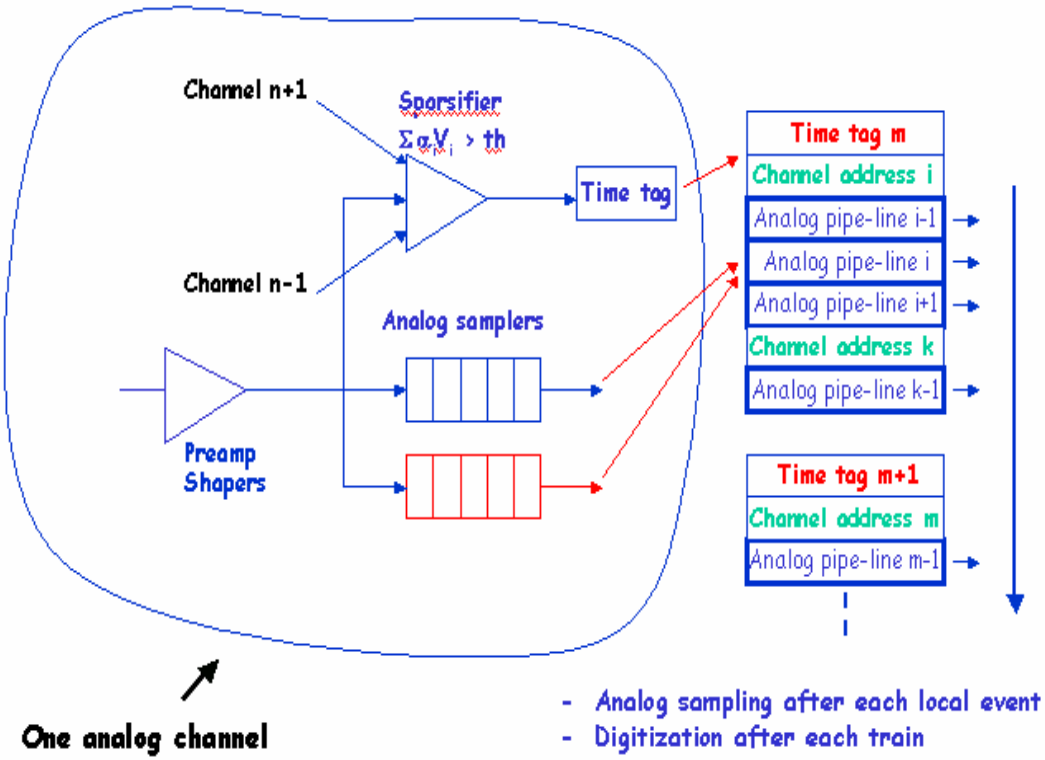
Ongoing work

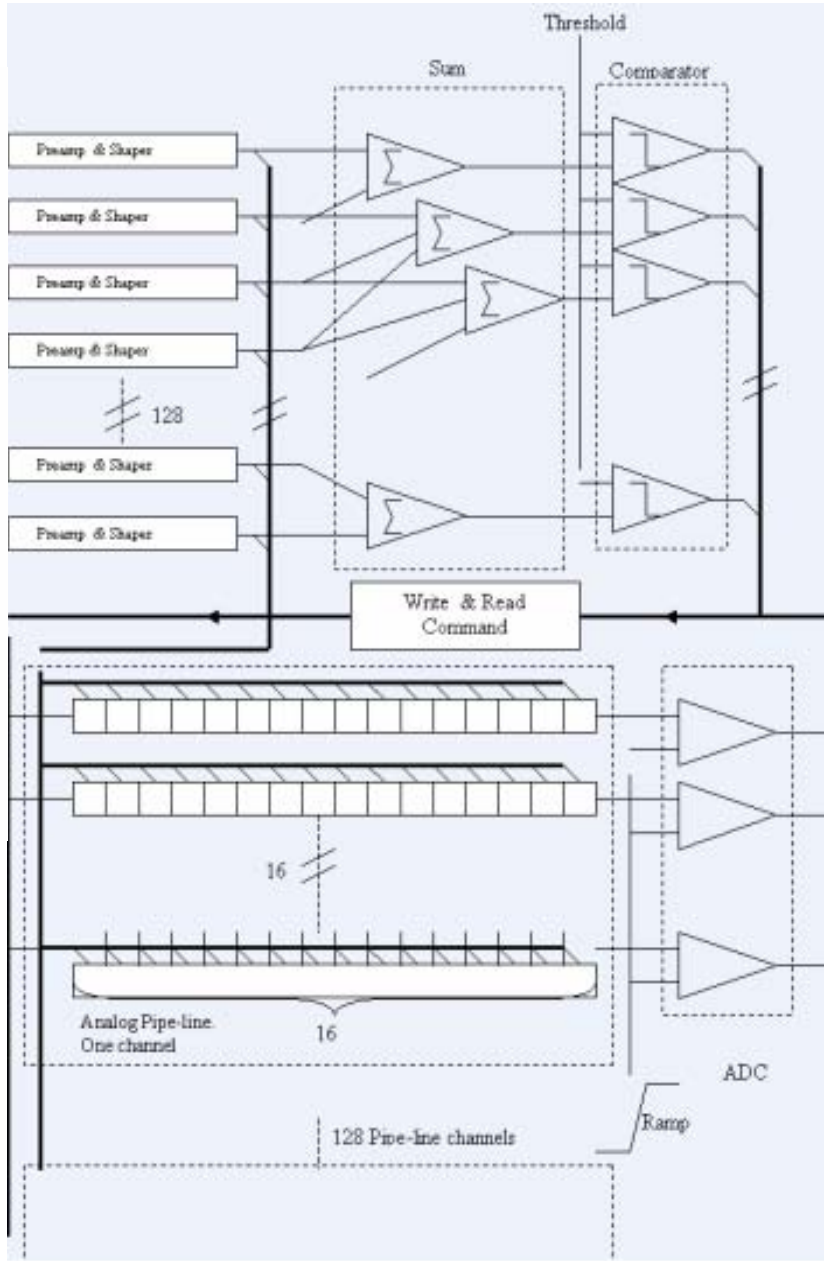
- ➔ **Complete the present tests**
- ➔ **Test test bench with actual Silicon prototype detector and with LD1060 & radioactive source.**
- ➔ **Timing studies (on test bench and simulations)**
- ➔ **Submit a 128-channel chip fall 05**

Will include:

- **Fast shaper**
- **Sparsifier**
- **Analog sampling**
- **Full ADC**
- **Power switching**

Full 128-channel underway





- Fast shaper under design
- Sparsifier under design
- ADC under design, partly laid out
- Analog samplers under layout
- Time resolution investigated

Conclusion

First experience with 180 nm CMOS DSM gives very encouraging results.

- **180 nm technology is proven to be mature and reliable**
- **Charge preamplifier works fine and will be kept as it is**
- **In the other blocks, the few encountered problems are well understood**
- **Solutions are ready to be included in the next version**

Some work still to be done:

- **Test the 11 other chips**
- **Test the comparator (offsets)**
- **Test on detector prototype at Lab test bench**

Next version underway including:

- **Fast and slow shapers,**
- **Analog samplers,**
- **Sparsifier,**
- **ADC**
- **Power cycling**

The first run delivered functional chips with very encouraging results.

This first version is thus instrumental for the design of an even better next version