Monolithic CMOS Pixel Detectors for ILC Vertex Detection

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A CMOS pixel vertex detector suited for use at the International Linear Collider (ILC) is proposed. The proposed detector consists of 50μm $\times$ 50μm macropixels, each with integrated bunch clock memory, on top of 5μm $\times$ 5μm micropixels that record amplitude information. The micropixels integrate over all bunch crossing in a train. Using the time recorded by the macropixels, the fine position measurements made in the micropixels can be associated to only a few of the 3000 bunch crossings in a bunch train.

1. INTRODUCTION

The vertex detector in a detector for the International Linear Collider (ILC) will be essential for much of the physics program. The detector must be able to efficiently separate hadronic final states with b-hadrons from light quarks and to separate jets from primary b-quarks from those containing primary c-quarks. The later is particularly challenging, but is especially important when attempting to measure the properties of Higgs bosons such as the branching ratio, $\frac{\mathcal{B}(h\to c\bar{c})}{\mathcal{B}(h\to b\bar{b})}$, that is needed to discriminate Standard Model Higgs bosons from models that extend the Standard Model such as SUSY[1].

The tracking performance of the vertex detector depends on the space point resolution of the detector, on the multiple scattering induced by the finite thickness of the detector and on the distance of the sensors from the interaction region. At the ILC there will be a large background close to the beam pipe from low energy electron-positron pairs produced in the strong electromagnetic fields of the colliding bunches. This background will depend on both machine parameters and on the strength of the detector's magnetic field which confines the low energy pairs to a cylindrical region around the beam pipe.

In this work we assume that the background in the inner most layer ($r = 1.5\,\mathrm{cm}$, $B = 3\,\mathrm{T}$) of the detector is 0.03 hit-cluster/mm^2/bunch crossing. Here one "hit-cluster" corresponds to the signal left by a charged particle crossing one of the planes of the vertex detector. Depending on detector technology, this may lead to several pixels above readout threshold. A background rate of 0.03 hit-cluster/mm^2/bunch is fairly typical for machine configuration at center-of-mass energies of 500 GeV. However, some choices of beam parameters are expected to result in higher backgrounds and most machine configurations at 1 TeV center-of-mass energy would result in higher backgrounds[2].

For bunch trains of 3000 bunches, our nominal background level corresponds to an integrated background of 90 hit-clusters/mm^2. For our nominal background, the mean number of bunches between hits in a given mm^2 is approximately 30.

2. VERTEX DETECTOR DESIGN

2.1. Detector Layout

A typically detector layout for the barrel portion of an ILC vertex detector is shown in Figure 1. The detector is designed so that there are at least 5 space points for every track, allowing stand-alone track finding to be performed in the vertex detector. In the SiD detector concept, which includes a tracker entirely based on silicon, considerable economy is obtained from having a large number of layers at relatively small radii. As can be seen in Table I the barrel

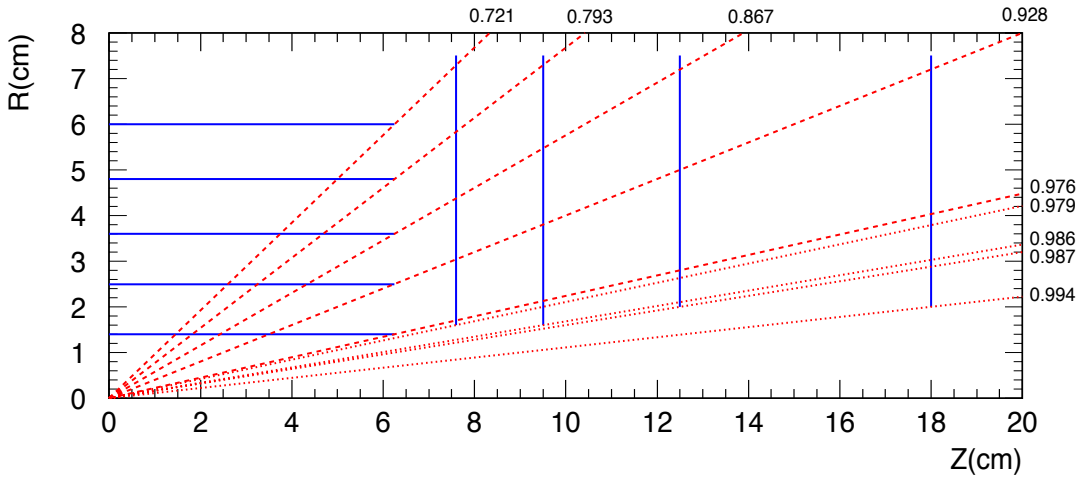

Figure 1: Example layout of the vertex detector. The dashed lines show the acceptance edges of the barrel layers. The dotted lines show the acceptance edges of the forward disks. The black numbers give the value of $\cos\theta$ associated with each acceptance edge.

Table I: CMOS Detector Barrel Configuration

Layer	**Radius** (cm)	**Total Length** (cm)	**No. of Chips**	**Chip Size** (cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

Table II: CMOS Detector Forward Disk Configuration

Annulus	**Inner Radius** (cm)	**Z** (cm)	**No. of Chips**	**Chip Size** (cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	125	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

portion of the detector comprises 100 detectors with a total sensor area of approximately 1750 cm^2. Also shown in Figure 1 are several layers of forward disks. The layout for the forward disk has not been fixed. One possible layout is to have an outer annulus formed by 24 4.4cm×2.2cm devices and an inner annulus of 24 0.9cm× ∼1.5cm devices. This gives a total of 288 overlapping sensors giving a total area of approximately 2100 cm^2.

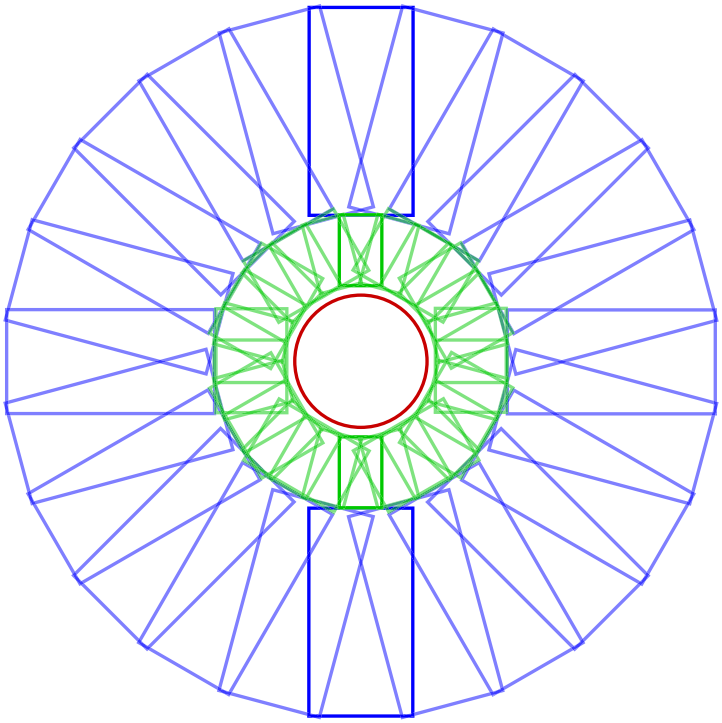

Figure 2: Example layout of the forward disk portion of the vertex detector. The sensors aligned with the vertical axis are a darker shade of green (blue) to illustrate the sensor shape in the inner (outer) annulus

2.2. Sensors

Possible sensor technologies for use at the ILC are limited by the bunch structure associated with the superconducting r-f cavities used in the accelerating structures. To make good use of the stored power in the superconducting cavities bunch trains of approximately 1 ms will be used. The spacing between bunches will probably be 330 ns, although in some configurations of the accelerator it may be necessary to accommodate bunch spacings of only 150 ns.

Given a peak occupancy of 0.03 hit-clusters/mm^2/bunch, the probability for a small inner layer 20μm $\times$ 20μm pixel to be directly hit during an entire bunch train is approximately 4%. This is probably too large to allow successful pattern recognition in designs that integrate over the entire bunch train. The situation is even worse when one considers that a typical track crossing the sensor may cause more than one pixel to be activated. The hit sharing problem becomes more acute if the pixel size is reduced in an attempt to limit the occupancy. However, in detector designs with a larger inner radius than employed here, viable designs that integrate over the entire bunch train and employ small pixels may exist [3].

In order to handle occupancies of approximately 0.03 hit-clusters/mm^2/bunch, it is necessary to either read out the detector during the bunch train, or to have some kind of buffer memory in each pixel. So far, most designs have concentrated on the former. A possible disadvantage of these schemes is that Electromagnetic Interference (EMI) may cause corruption of the pixel data if it is transfered during the bunch trains.

Here we consider 50μm $\times$50μm pixels with four buffer memories in a scheme similar to that proposed for the readout of the SiD silicon-tungsten calorimeter [4]. If the signal in the active pixel exceeds a threshold, the resulting bunch number is stored in a memory cell. Assuming that the 50μm $\times$50μm pixels are large enough that there is negligible hit sharing, 0.03 hit-clusters/mm^2/bunch corresponds to a bunch-train occupancy of 22.5%. The Poisson probability that there are four or more hits in a 50μm $\times$50μm pixel and that it becomes "dead" by the end of the bunch-train is very small, $\sim 10^{-4}$.

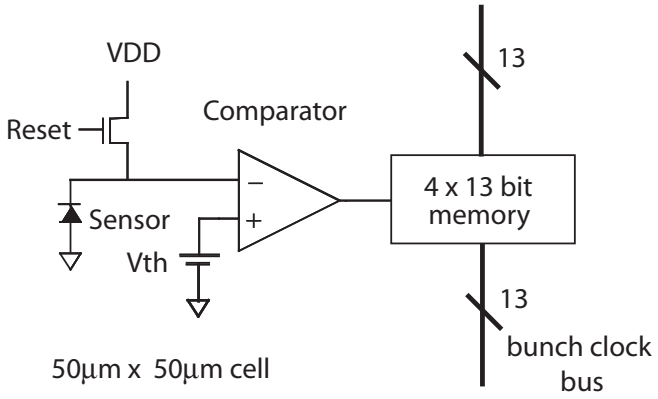

Figure 3: A conceptual diagram showing the layout for one of the single macro pixel cells.

Since the bunch number of each hit will be known, the occupancy for pattern recognition will also be very small. In any given bunch crossing, less than 10^{-4} of the 50μm $\times$50μm pixels will be hit.

In what follows we refer the 50μm $\times$ 50μm as the "macropixel" array. We expect that the macropixel array will be relatively immune to EMI because any electronics activity during the bunch train will occur largely within a single pixel. A conceptual diagram of the electronics inside of a single macro cell is shown in figure 3. The detector element is reset after each beam crossing. If the charge detected in the pixel is above threshold, the time of beam crossing is stored in the memory.

2.3. Micropixel array

The position resolution of the system can be improved by incorporating a second layer of much smaller pixels in the system. These 5μm $\times$ 5μm pixels integrate charge for the entire bunch train. After the bunch train has passed, the pixel can be randomly addressed as shown in figure 4. If the macropixels are read out first, it necessary to only read out those micropixels which are associated with hit macropixels. This can potentially reduce the readout time for the micropixels by a factor of 5, corresponding to the 20% occupancy of the macropixels.

2.4. Space point reconstruction

For the standard background of 0.03 hit-clusters/mm^2/bunch, the occupancy of the macropixels will be about 20%. For the macropixel that are hit only once, we will know the bunch crossing without ambiguity. The space point in any associated micropixel can then be associated to a single bunch crossing. This is illustrated in figure 5 which was generated using a slightly higher than nominal occupancy (30%) and corresponds to the hits from an entire bunch train. In pixels that are hit more than once, there will be an ambiguity in the beam crossing time from the multiple hits during the bunch train.

During pattern recognition for events with the standard background conditions, the occupancy in the inner layer of the macropixels will be less than 10^{-4}. The first step in the pattern recognition, will likely be to find tracks using the macropixel array. Because the occupancy is so low, this should not be difficult. Using the associated micropixel, the trajectories of the charged tracks can be refined. In the outer layers, the vast majority of macropixels will only have a single micropixel associated. In the inner most layer, approximately 80% of macropixels will have a single micropixel associated. In the remaining 20% of cases, it will be necessary to try all combinations of associated micropixels to find the one that yields the best track fit.

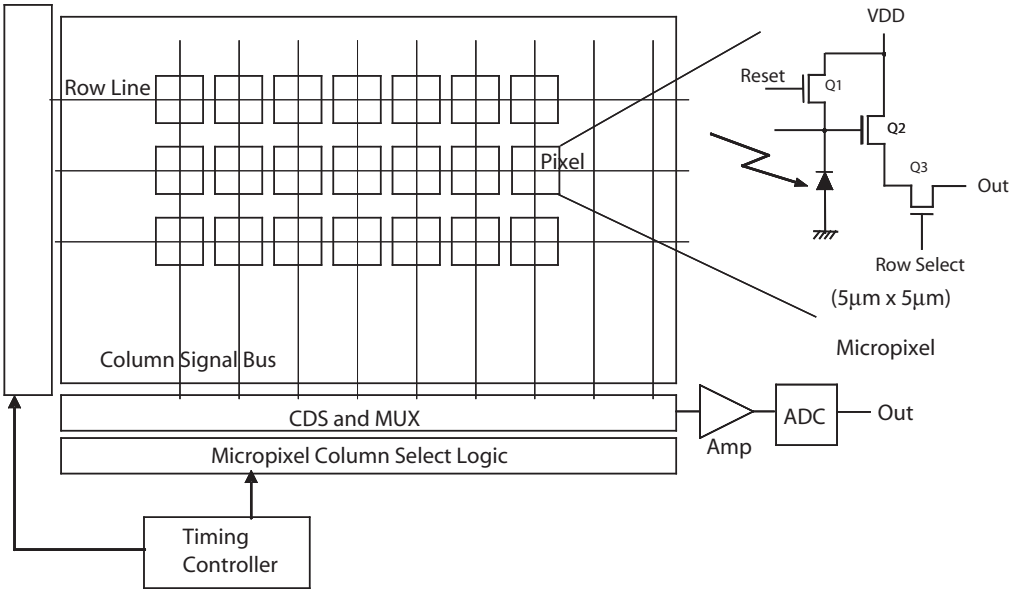

Figure 4: A conceptual diagram showing the layout of the micropixel array and a single micropixel cell.

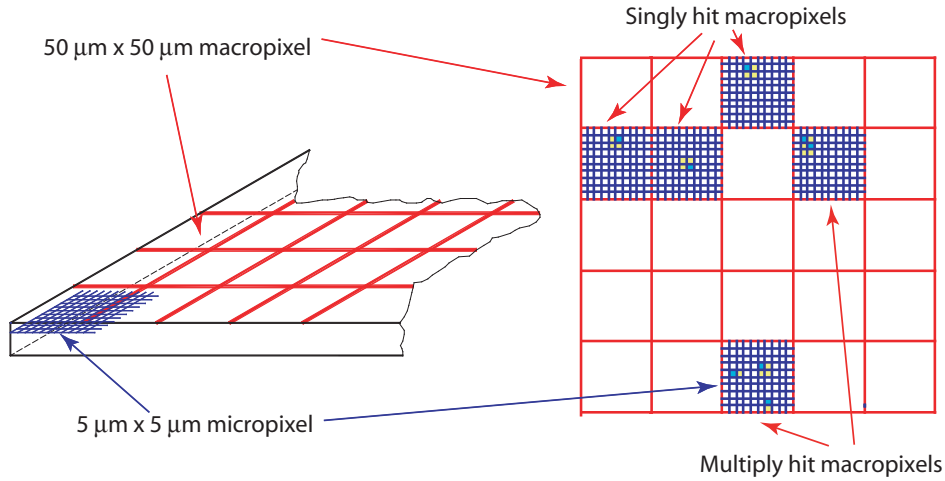

Figure 5: A conceptual diagram showing the association between macro- and micropixels. The diagram on the right shows a perspective drawing of the two layers. The diagram on the right shows a plan view and a simulation of the pixels that were hit during an entire bunch train. The simulated background conditions were somewhat worse than the standard ones. Because the macropixel records the bunch times of the hits, when individual bunch crossings are considered the macropixel occupancy drops by a factor of roughly 3000 over what is shown here.

3. FUTURE PLANS

In the course of the ALCPG 2005 Snowmass workshop it became clear that several machine configurations could produce background several times higher than the 0.03 hit-clusters/mm^2/bunch initially assumed. If this is the case, the probability for a noise hit to occur in the same macropixel as a true hit could rise above 50% making it difficult to associate the tracks with the correct micropixel cluster. We are presently working with Sarnoff Corporation[5] to define a roadmap to reduce the size of the macropixel array pixel to below 10μm $\times$10μm. This can be achieved by using a semiconductor process with a smaller feature size. If the pixel size can be reduced enough, it may be that the

micropixel array will become superfluous. Therefore we plan to give first priority to the development of macropixels and plan to produce small-scale prototypes of the macropixel array as a first step.

Acknowledgments

We wish to thank organizers of the vertex-detector session at Snowmass 2005 for organizing useful and stimulating sessions. This work is partially supported by the U.S. Department of Energy.

References

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