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Front-end chip for H-Cal SiPM readout

S. Blin, J. Fleury, C. de La Taille,
G. Martin-Chassard, L. Raux

IN2P3/LAL Orsay

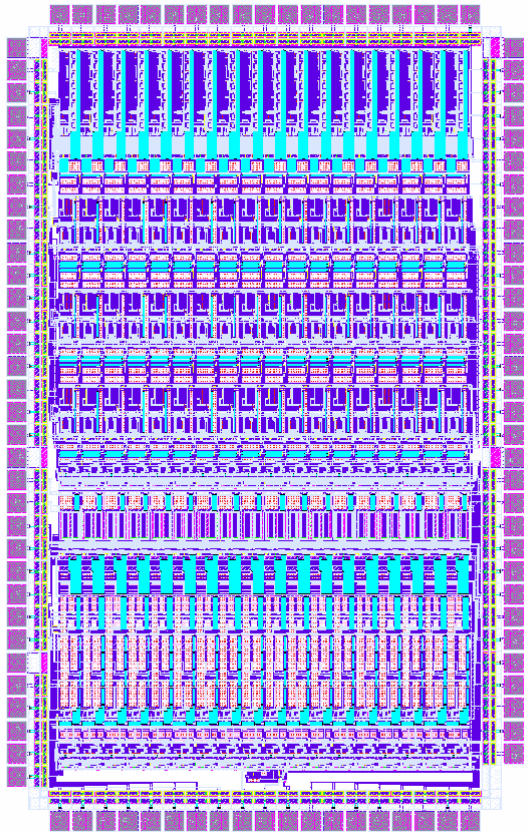
http::/www.lal.in2p3.fr/technique/se/flc

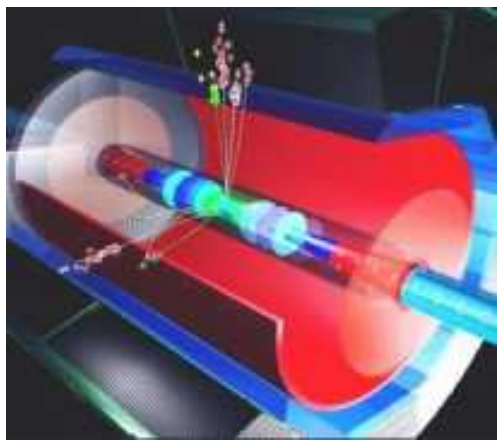
FLCALICE Calorimeter

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Contents

- SiPM presentation and connection
- Chip description
- Measurement results
- Schedule and cost
- Conclusion

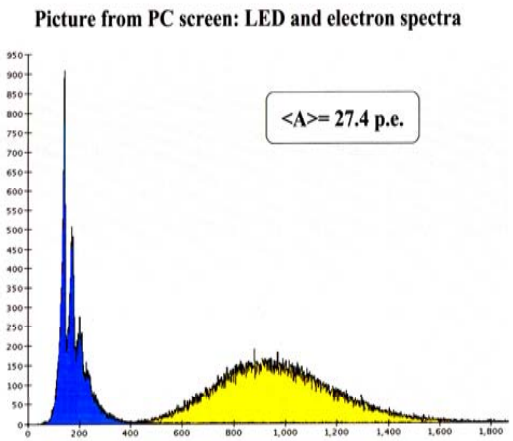




SiPM : electronic characterisation

➢ SiPM signal :

gain 10^6 (1 p.e.=160fC) and MIP ~ 16 p.e.
Dyn. range ~ 120MIPs (400pC)
Fast signal : few ns rise time
measurement compatible with ECAL readout
→ Slow shaping for physics mode



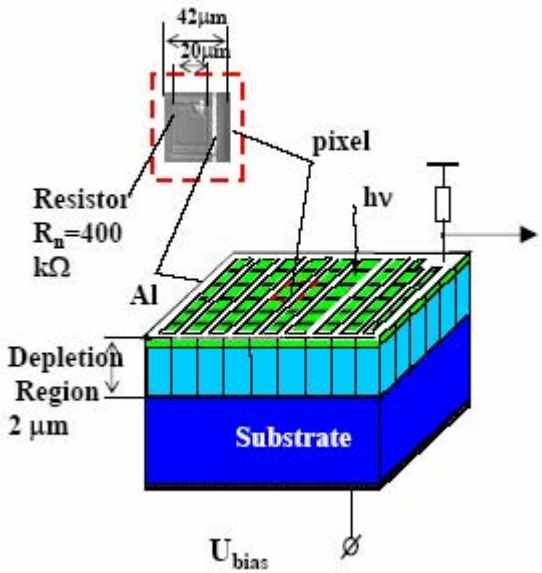
From Felix Sefkow, DESY

➢ SiPM noise:

2MHz noise rate (1 p.e. every 500ns)
→ calibration on SPE necessary at fast shaping to avoid pile up

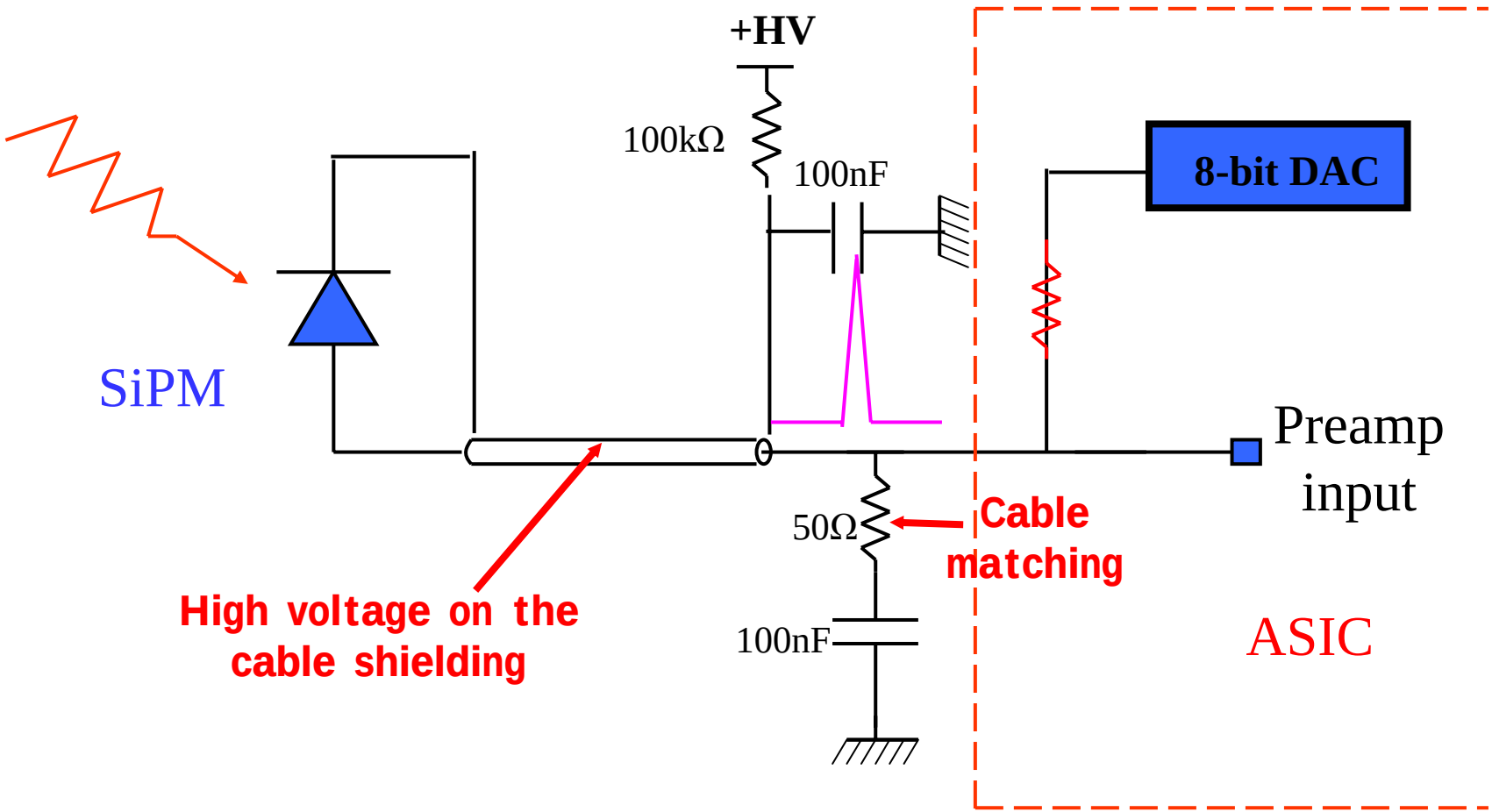
➢ SiPM gain varies with high voltage:

3-7% / 100mV
→ DAC on chip to ajust gain



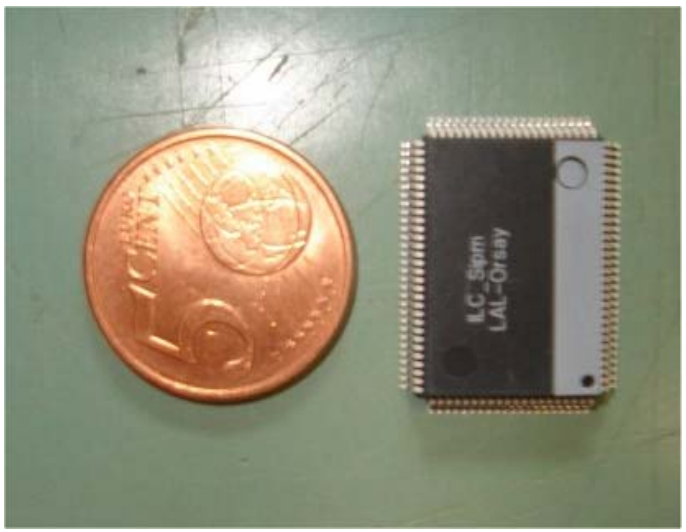
SiPM Connection

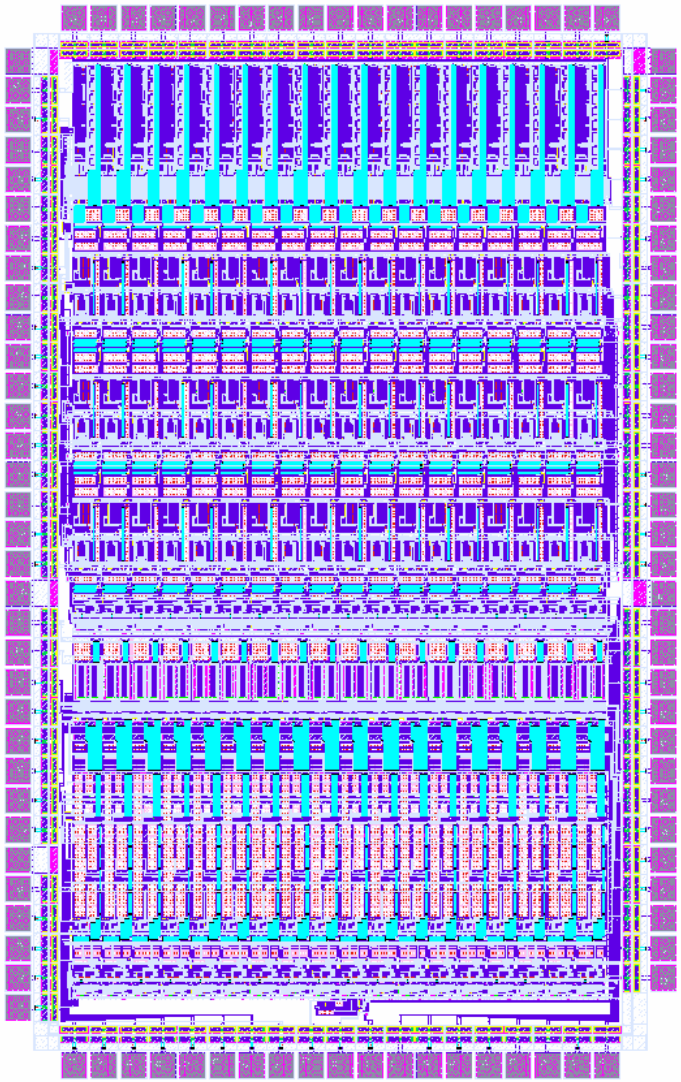
- **SiPM connected with followed biasing scheme :**
  - **HV = 45 V**
  - **No external circuitry around SiPM**



Chip description

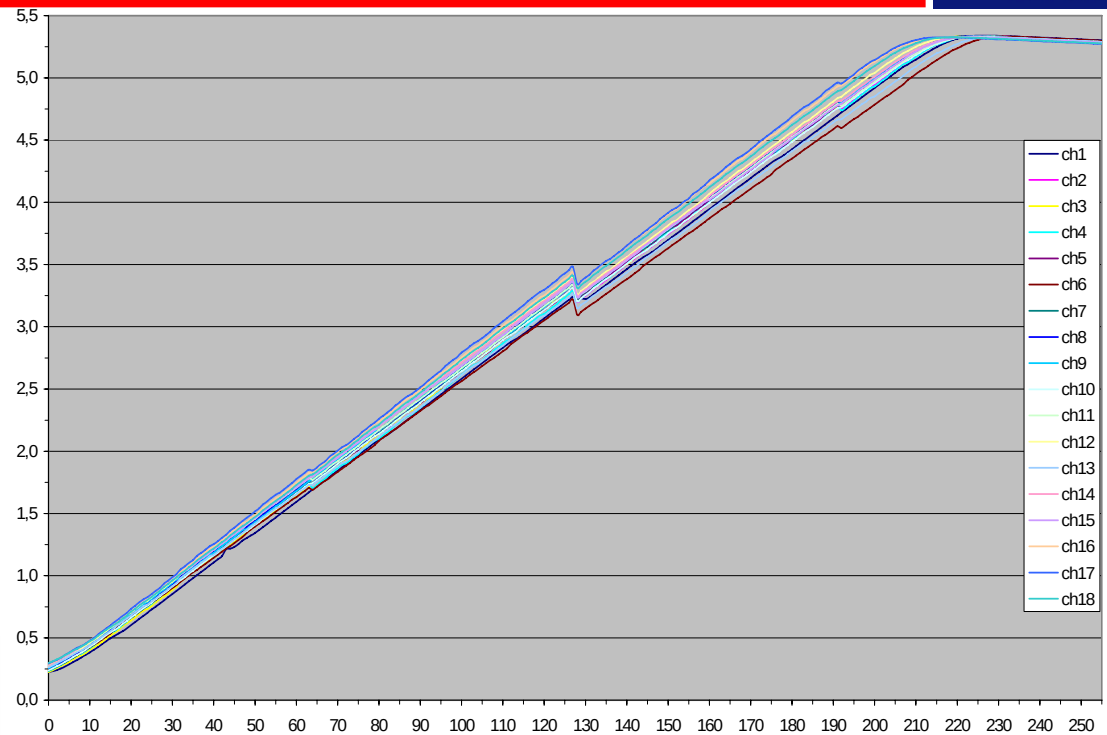
- **18-channel 8-bit DAC (0-5V)**
- **18-channel front-end readout :**
  - Variable gain charge preamplifier (0.67 to 10 V/pC)
  - Variable shaping time CRRC^2 shaper (12 to 180 ns)
- **Track and hold → 1 multiplexed output**
- **Power consumption :** ~200mW (supply : 0-5V)
- **Technology :** AMS 0.8 µm CMOS
- **Chip area :** ~10mm²
- **Package :** QFP-100



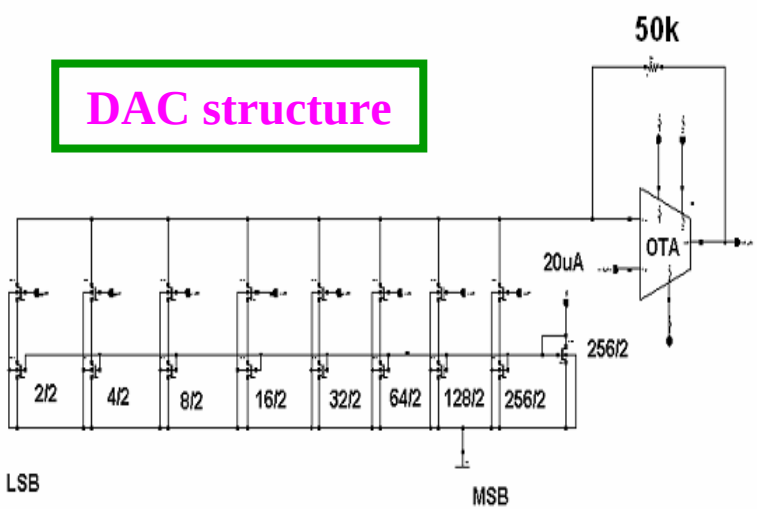


DAC description and measurements

- 18 channels
- 8 bits
- Excursion : 0-5V
- Structure based on scaled mirrors
- Non linearity (~2%) due to mismatch in the current mirrors

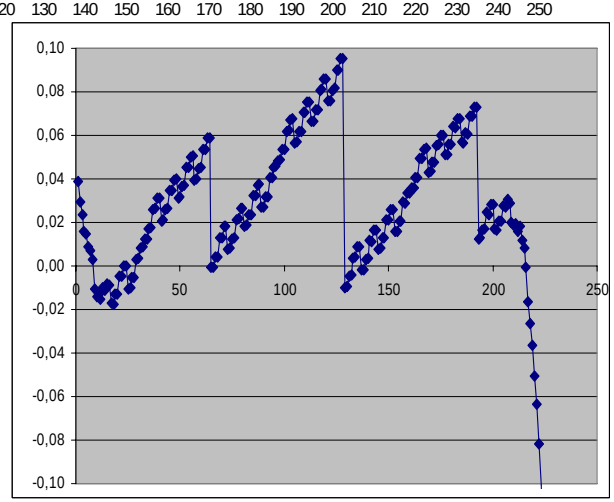


DAC structure

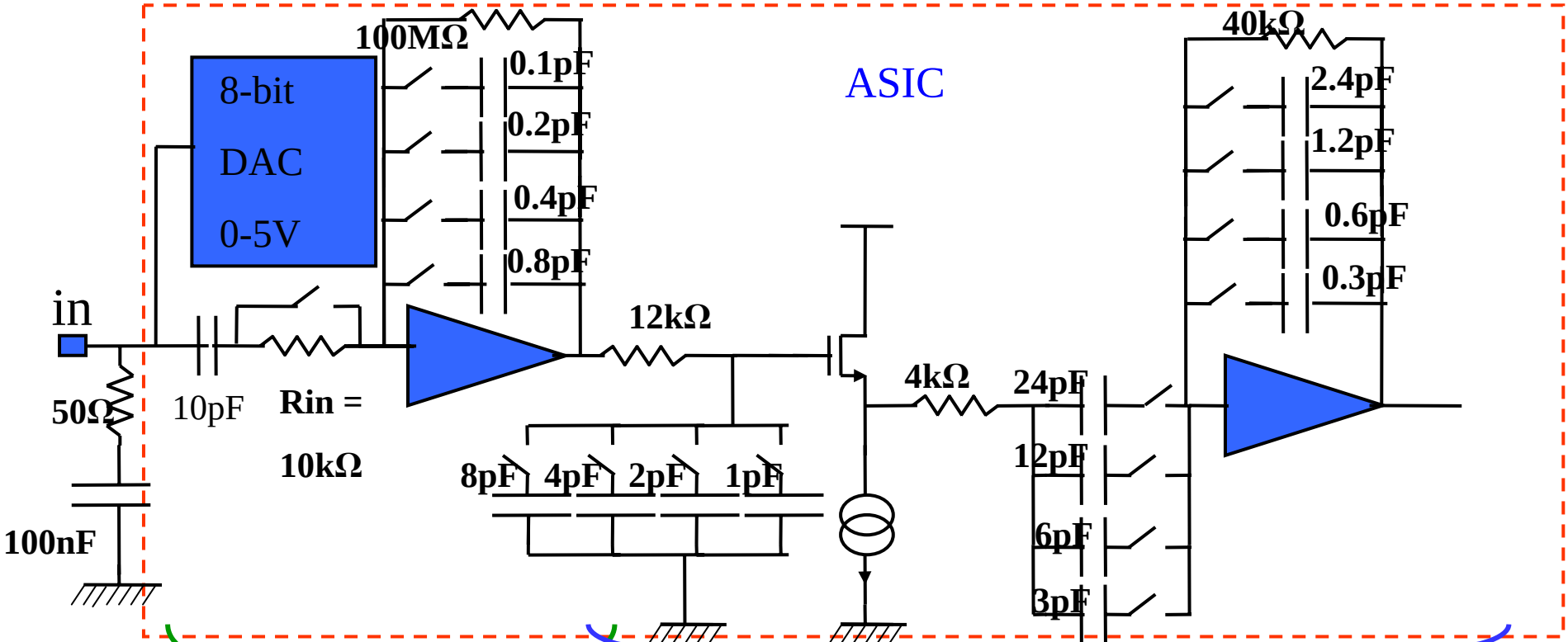


18 channel linearity

Residuals in Volts



Channel architecture for SiPM readout



Charge Preamplifier :

- Low noise : 1300e- @40ns
- Variable gain :

  4bits : 0.67 to 10 V/pC

CR-RC² Shaper :

Variable time constant : 4 bits (12 to 180ns)

12ns → photoelectron measurement (calibration mode)

180ns → Mip measurement (physics mode)

compatibility with ECAL read-out

MIP and photo-electron responses

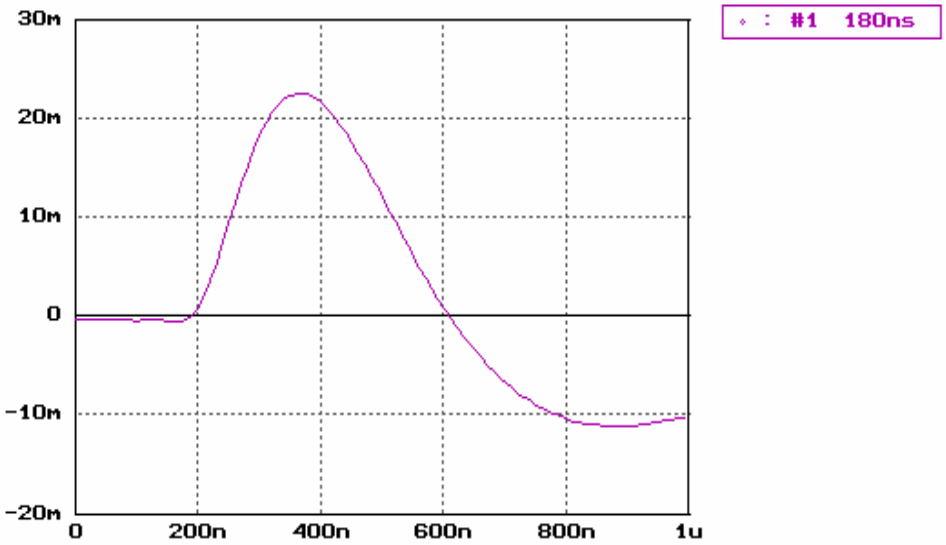
Physics mode :

Cf=0.4pF- τ=180ns - Rin ON

1 MIP (16 p.e) →

Vout = 23 mV @ tp = 160 ns

Noise = 1mV RMS



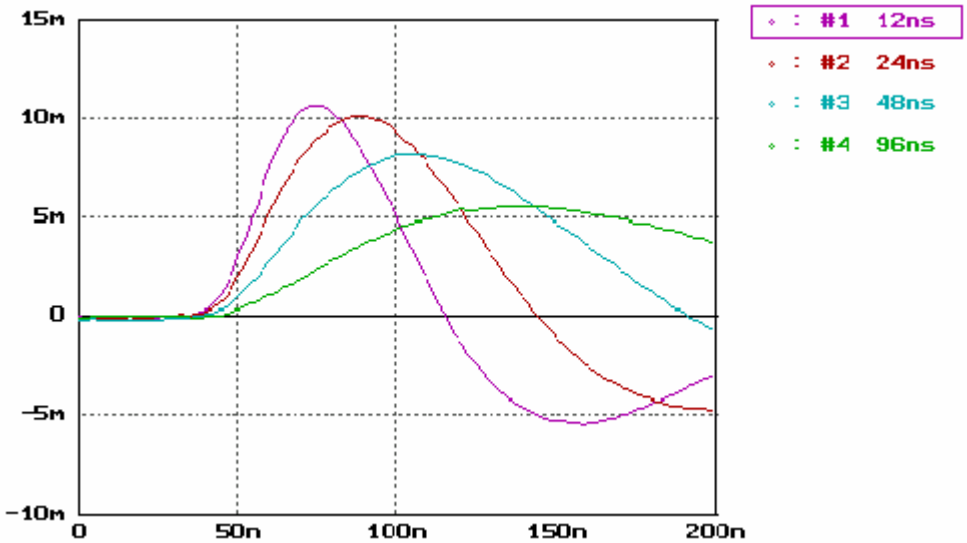
Calibration mode :

Cf=0.2pF - τ=12ns - Rin OFF

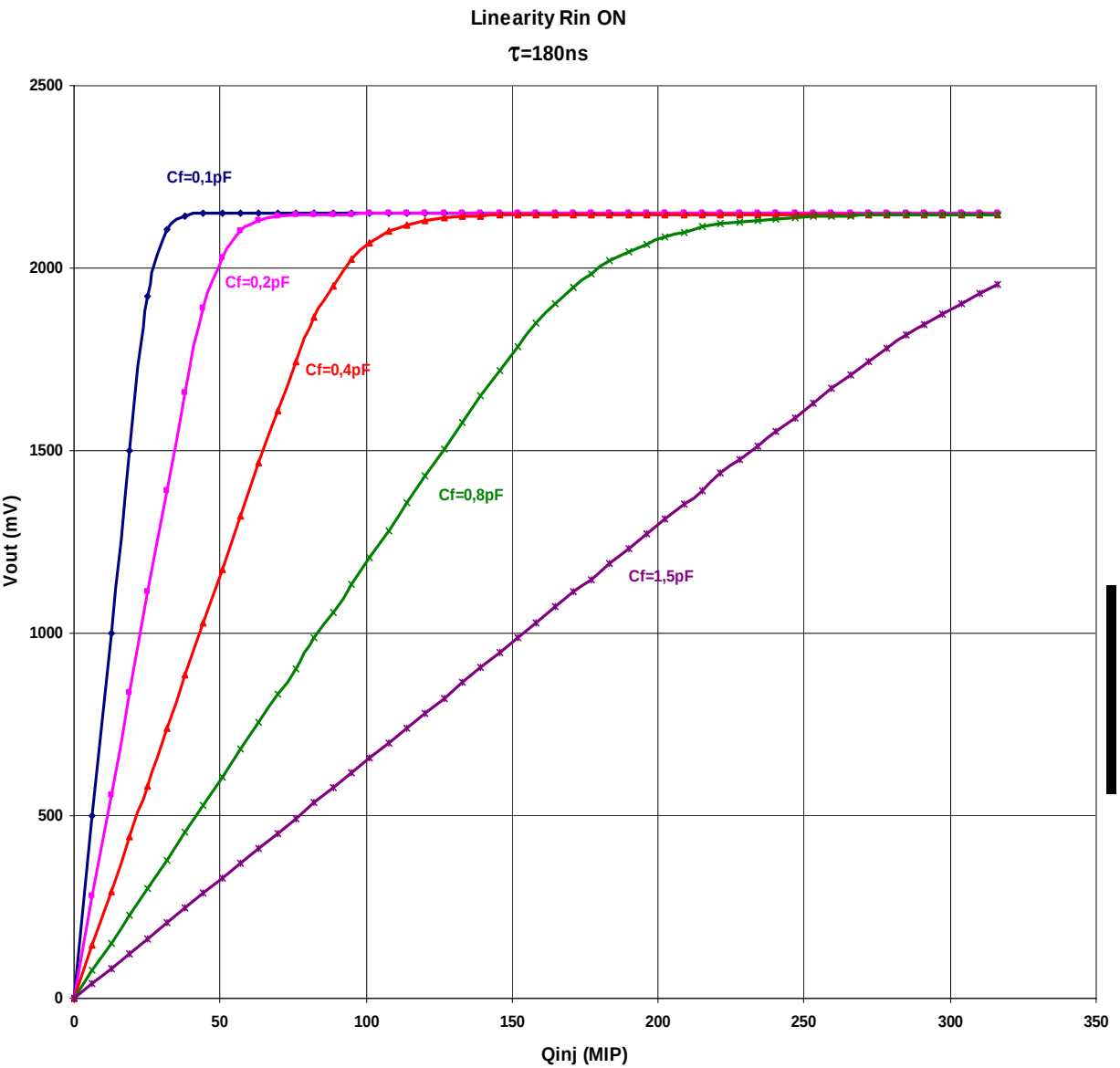
1 SPE →

Vout = 11 mV @ tp = 35 ns

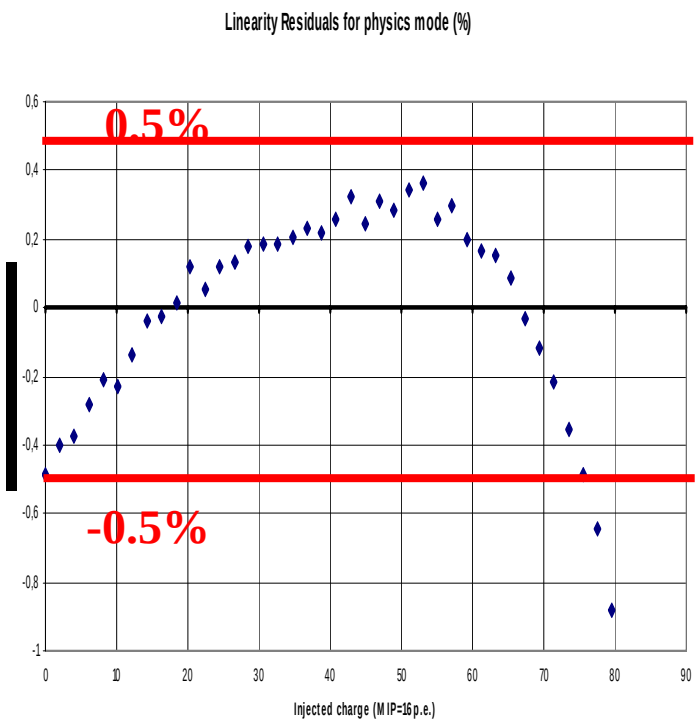
Noise = 1.25mV RMS



Linearity measurement (physic mode)



- Voltage swing : ~2.1V
- Dynamic Range: 80 MIPs
- Linearity: <1%

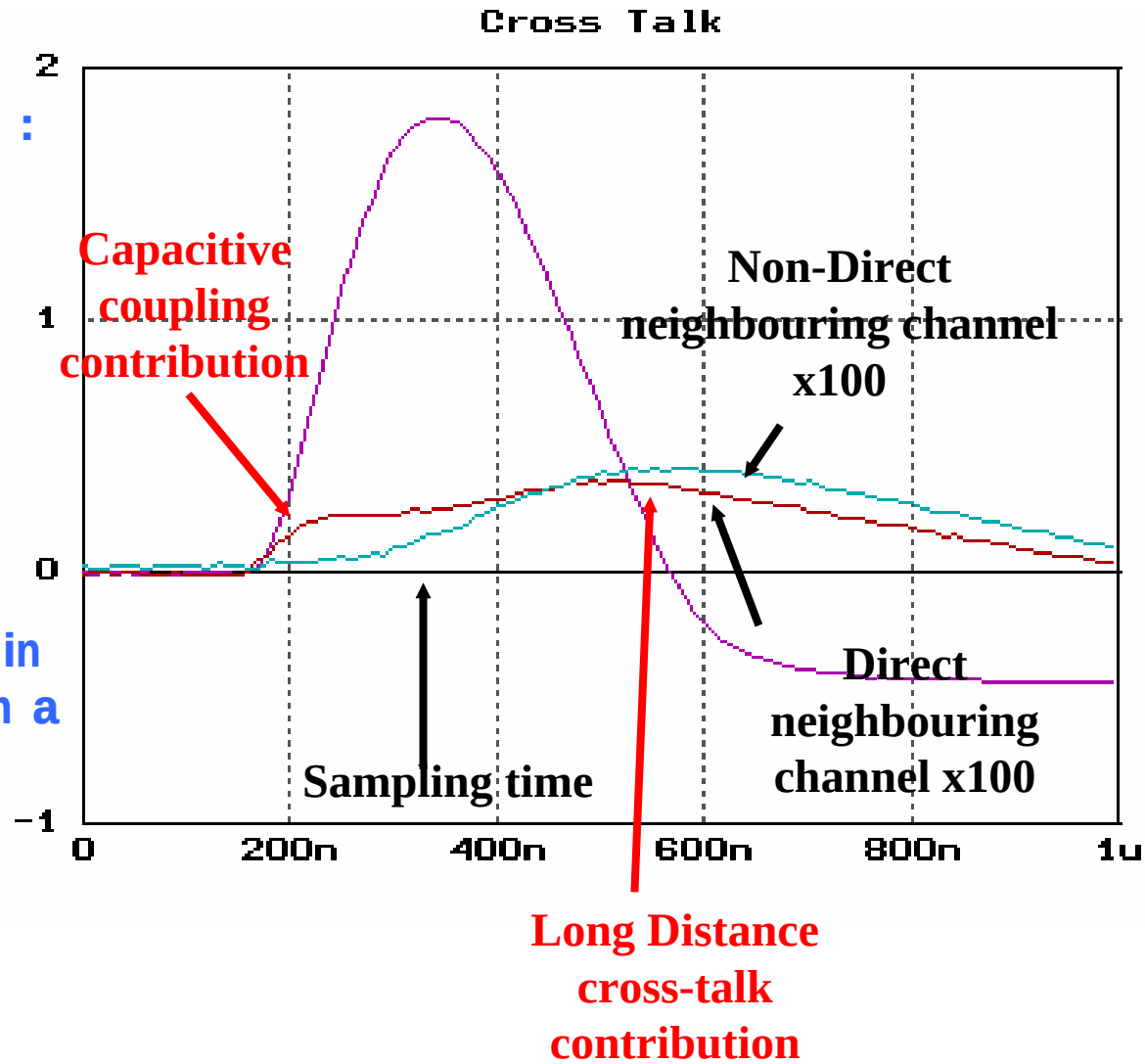


Cross-talk measurement

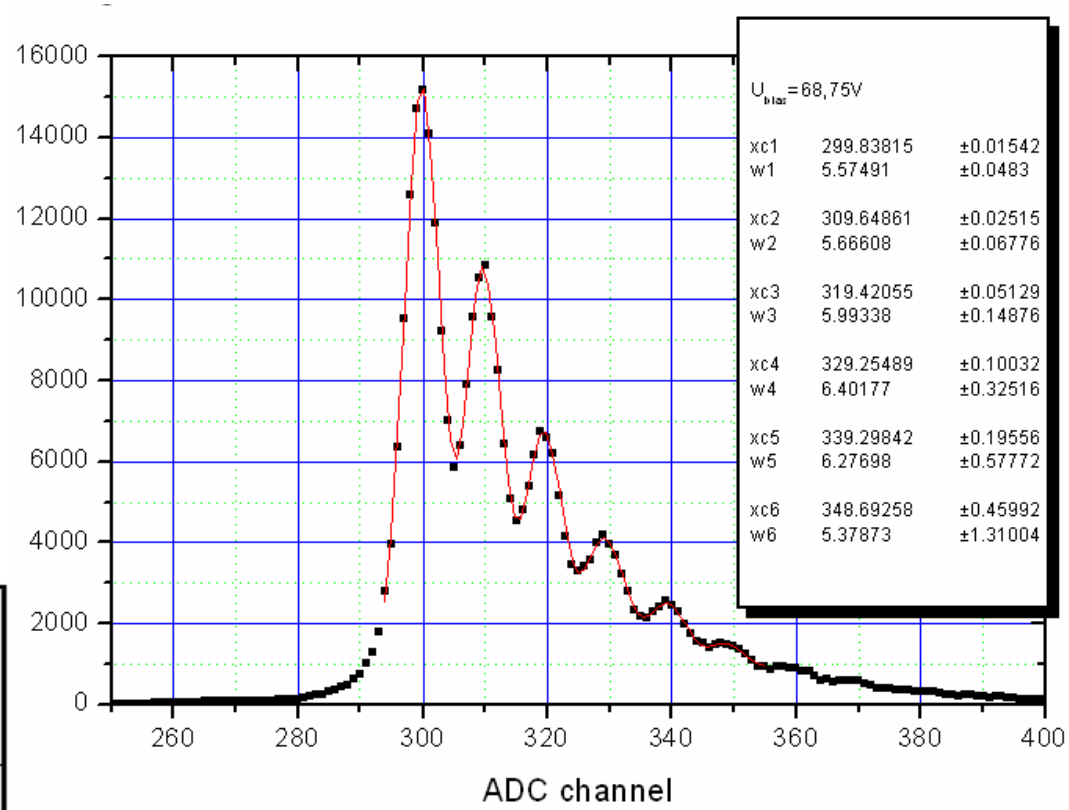
Channel-to-Channel cross-talk :

- ~ 1-2‰ :negligible
- 2 contributions :
  - **Capacitive coupling between neighboring channels**
  - **Long distance crosstalk in all channels (comes from a reference voltage)**

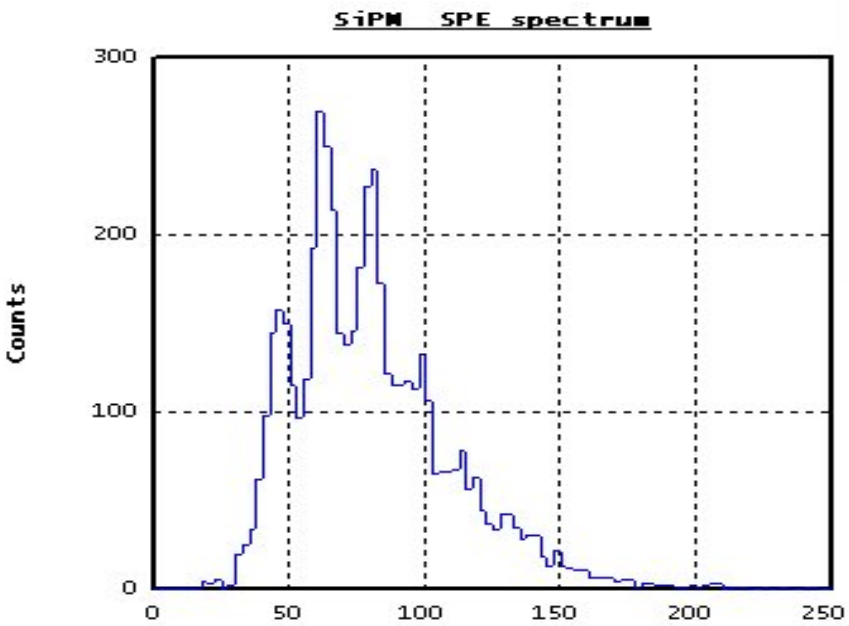
Set-up: Cf=0.4pF, τ=180ns



SPE spectra



Measured by LAL group at Orsay



M.Groll and A. Karakash

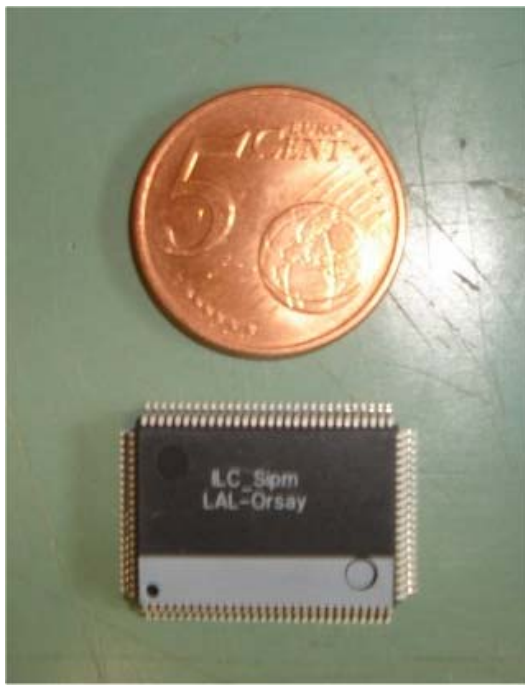
DESY / MEPhI

Schedule and cost

- **Schedule :**
  - Prototype study began in April 2004
  - Prototype Submission in June 2004
  - Prototype Delivery in September 2004
  - Test and validation with SiPM in October 2004
  - Production of 1000 chips in November 2004
  - Production Delivery in January 2005
  - Systematic chips test in March 2005
  - All chips available by April 2005

  → Chip development less than 1 year
- **Cost :**
  - Silicon : 1000 dies → 21.4 k Euros
  - Package : PQFP-100 →4.1 k Euros

  →Total : 25.5 k Euros



Summary

- **1000 Chips produced in less 1 year**

- **Very versatile chip :**
  - **Variable gain from (from 0.67 to 10 V/pC)**
  - **Variable shaping time (from 12ns to 180ns)**

- **DAC on chip provide up to 5V high voltage change**
  → adjust SiPM gain : 7%/100mV

- **In calibration mode : fast shaping clearly separated SPE peaks**

- **In physics mode : dynamic range from 1mV to 2V (11bits)**
  → Matches detector