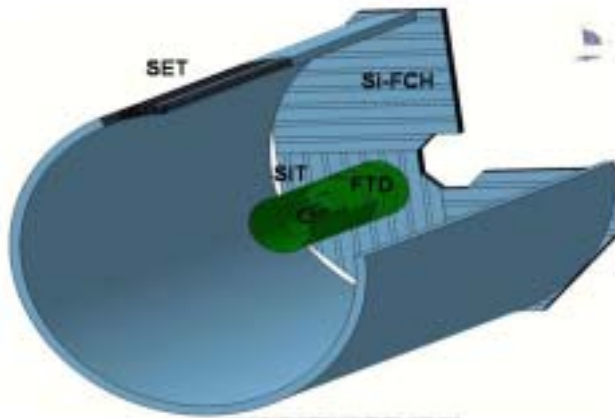


# Large Silicon Tracking Systems for ILC

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LPNHE, Universite Pierre & Marie Curie/CNRS-IN2P3



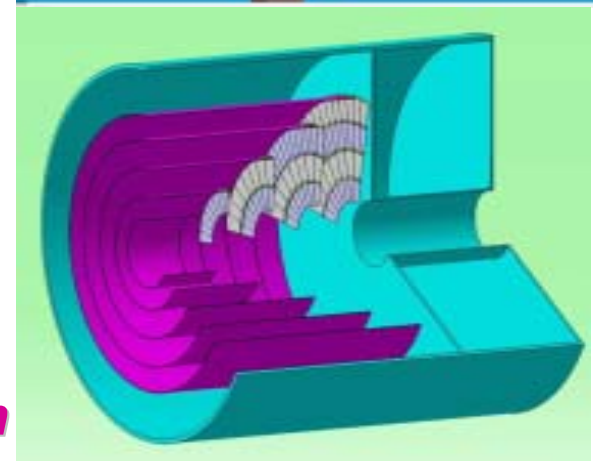
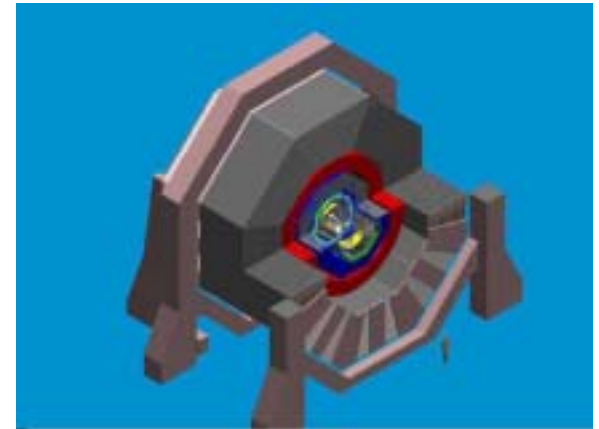
★ Roles

★ Designs

★ Main Issues

★ Current status

*R&D work within  
SiLC R&D Collaboration*

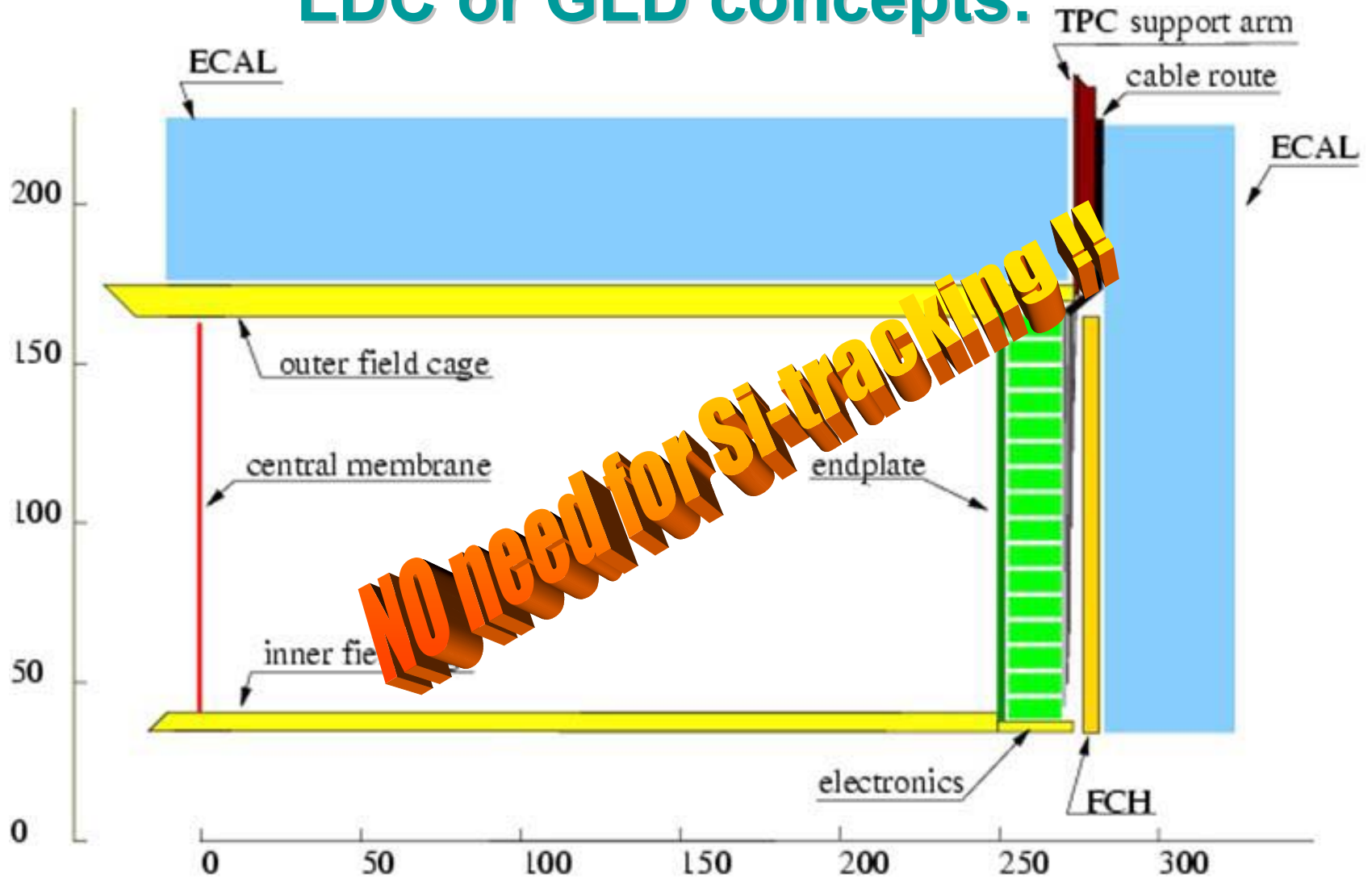


*Tracking Session at LCWS'05, Stanford, March 18-23, 2005*

Two detector concepts:

Mainly differing by the  
tracking strategy

# LDC or GLD concepts:



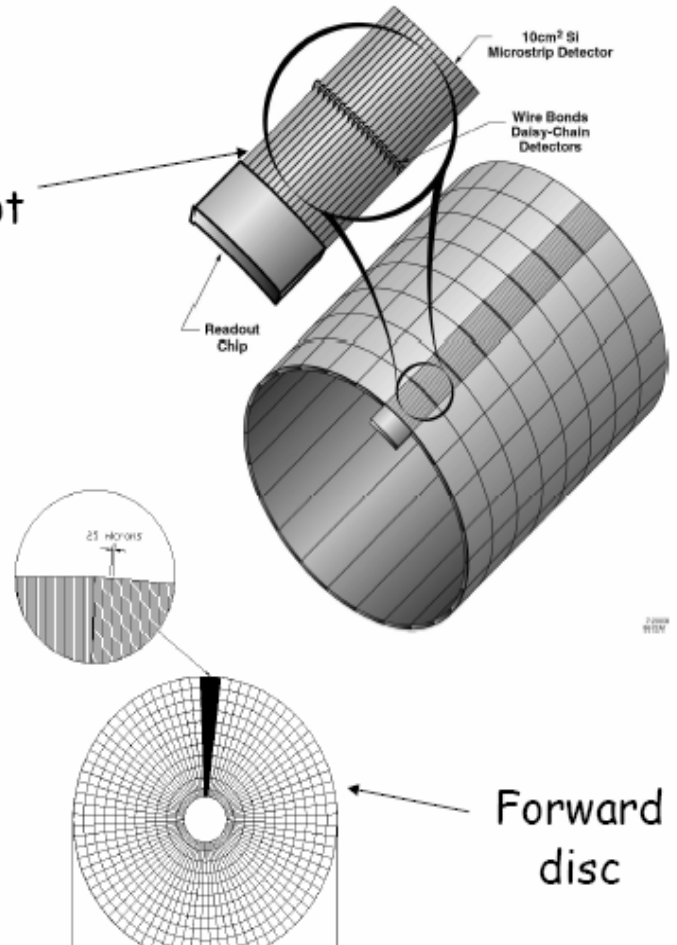
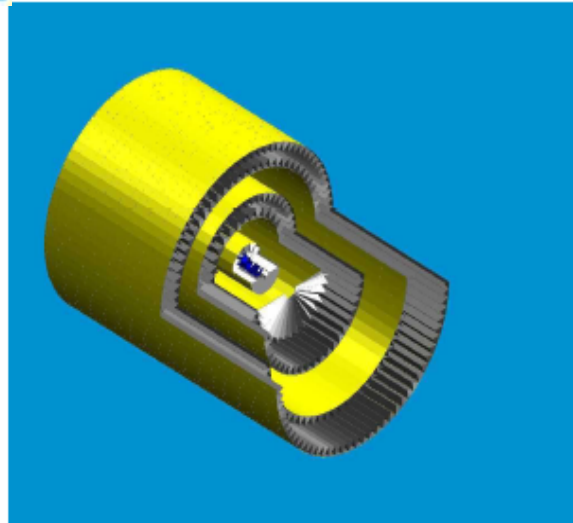
The tracking is mainly achieved by TPC and microvertex



SiD Tracker

All we need is silicon !!

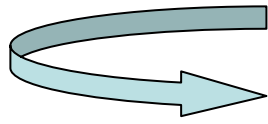
"Tiled" concept



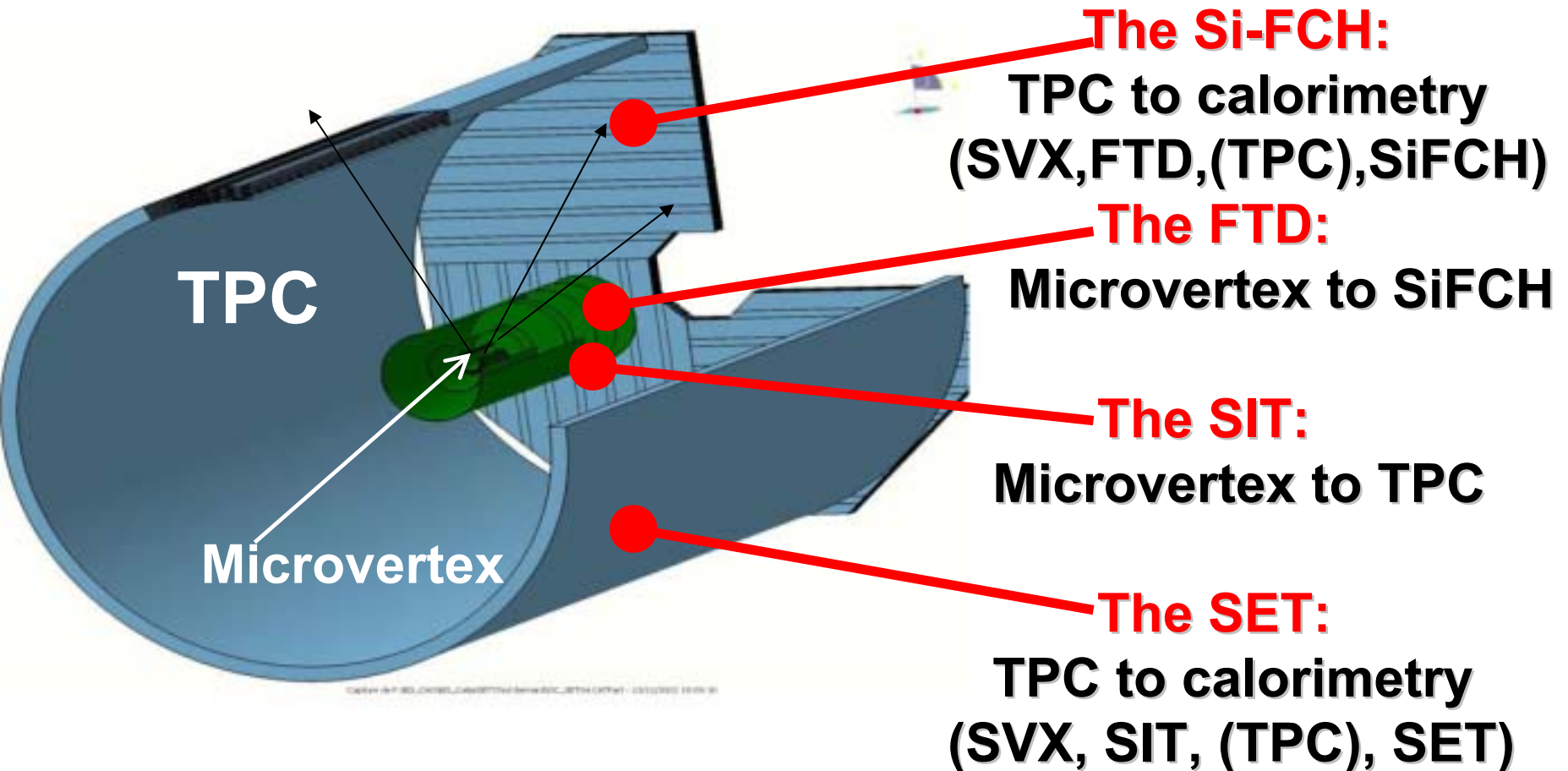
Basic SiD concept:

Si tracking acts as a "sagitter" linking microvertex and Si-W calorimetry. **Question: do we need more?**

# Silicon Tracking System with a central gaseous detector

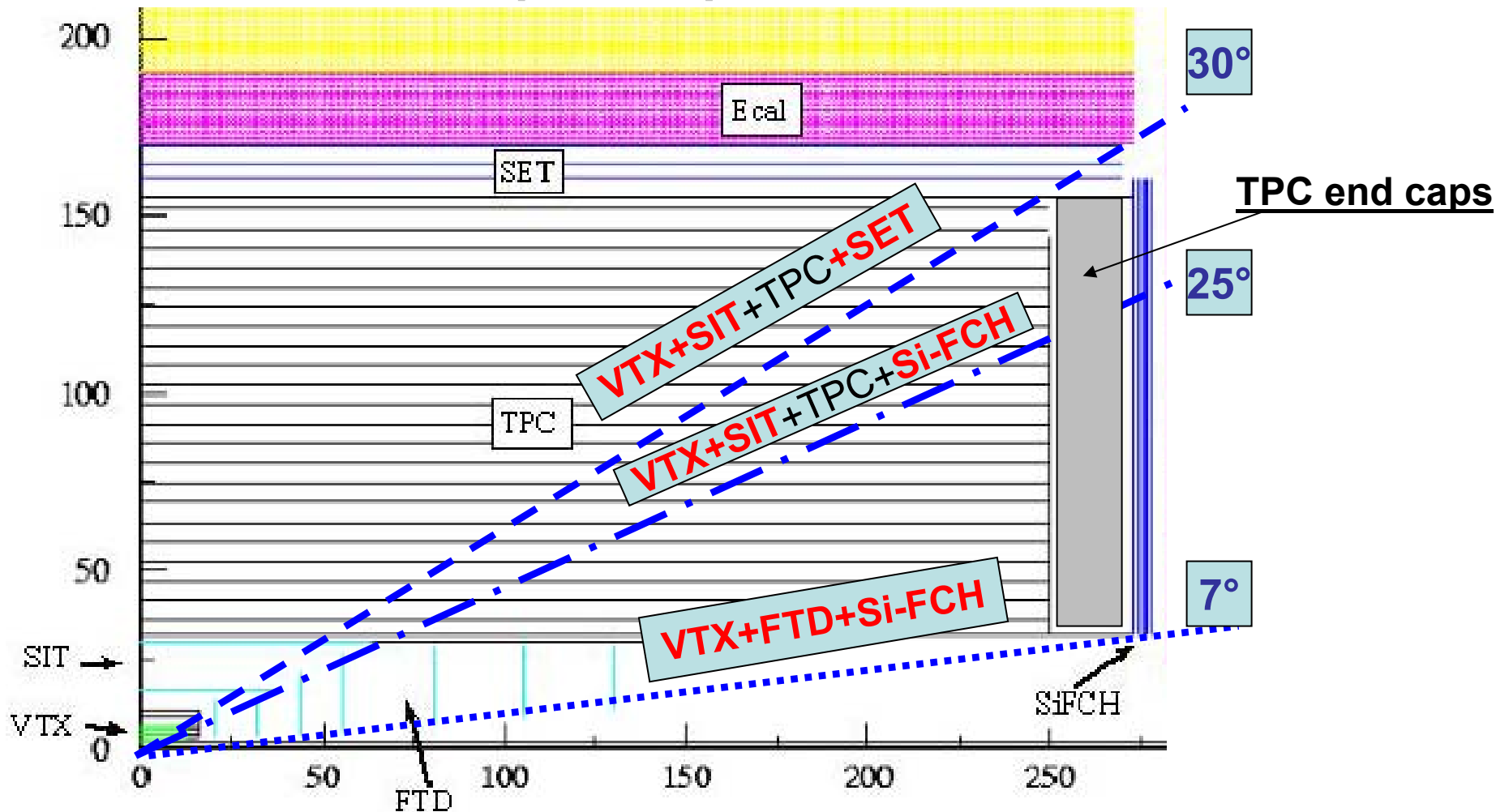


**The Silicon Envelope concept =  
ensemble of Si-trackers surrounding the TPC (LC-DET-2003-013)**



## Crucial Keywords:

- ✓ Robustness
- ✓ Full coverage
- ✓ Improved performances

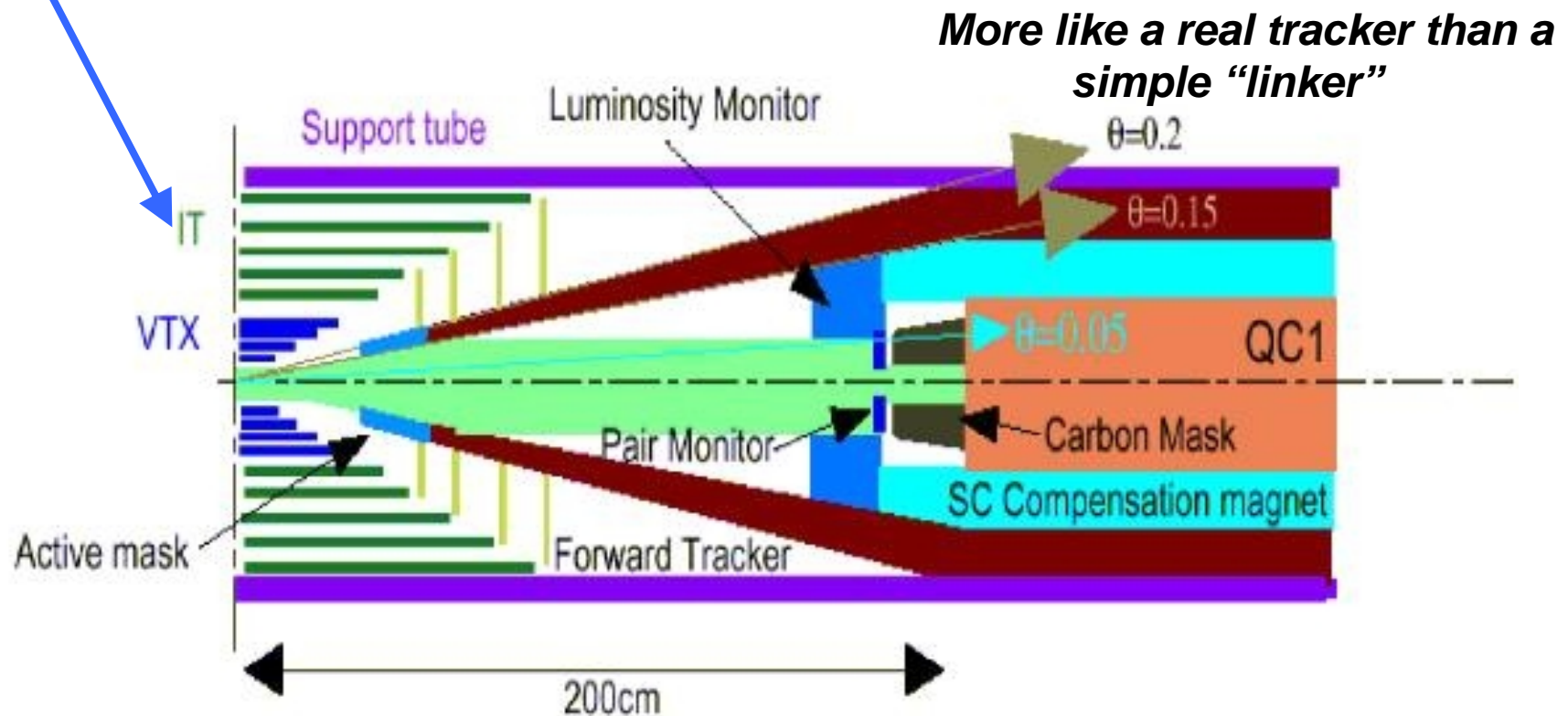


# Si tracking components in the central barrel:

## 1) The innermost layers:

If a TPC: 2 alternative designs:

- SIT (*Silicon Internal Tracker*) (LC-DET-2001-036) and TESLA TDR, similar to the ISL in CDF
- IT (*Intermediate Tracker*), in the GLD design, with 5 Si layers, similar to the SCT in ATLAS.



*(N.B. Same conceptual design can be used for innermost central layers in SiD)*

***SIT links microvertex (2 to 3  $\mu\text{m}$ ) to TPC (50-80  $\mu\text{m}$ ).***

***It is made of two double-sided Si-microstrips layers, 50  $\mu\text{m}$  readout pitch,  
200  $\mu\text{m}$  thickness, 7 to 8  $\mu\text{m}$  spatial resolution***

***It improves the momentum resolution by about 30%.***

***It gives the possibility to detect secondary vertices of long lived particles  
It covers the tracking down to 25° wrt beam axis.***

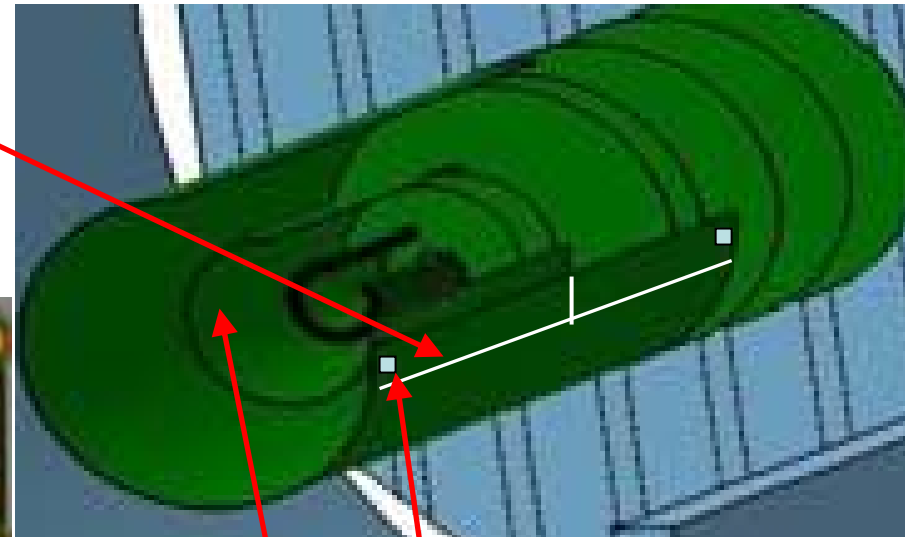
Based on 30cm long strips for SIT1 and  
eventually 60cm long strips for SIT2.

Total of about 200K to 300K channels

**Electronics on both ends**



28 cm long Si strips prototype  
tested with VA front-end

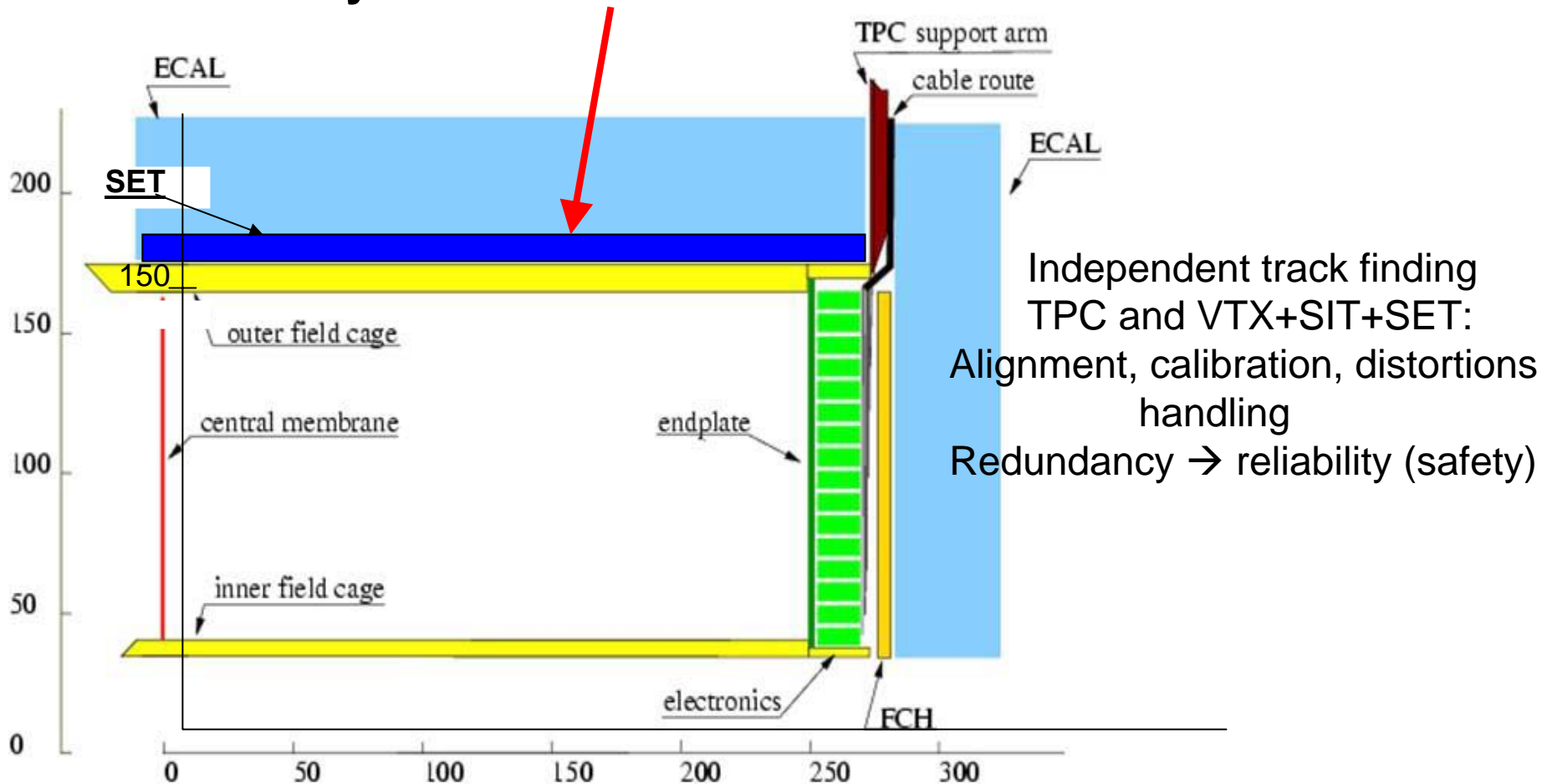


1st layer  
( $R=16\text{ cm}$ )

2nd layer ( $R=30\text{cm}$ ).

## 2) Central Outer Si layers

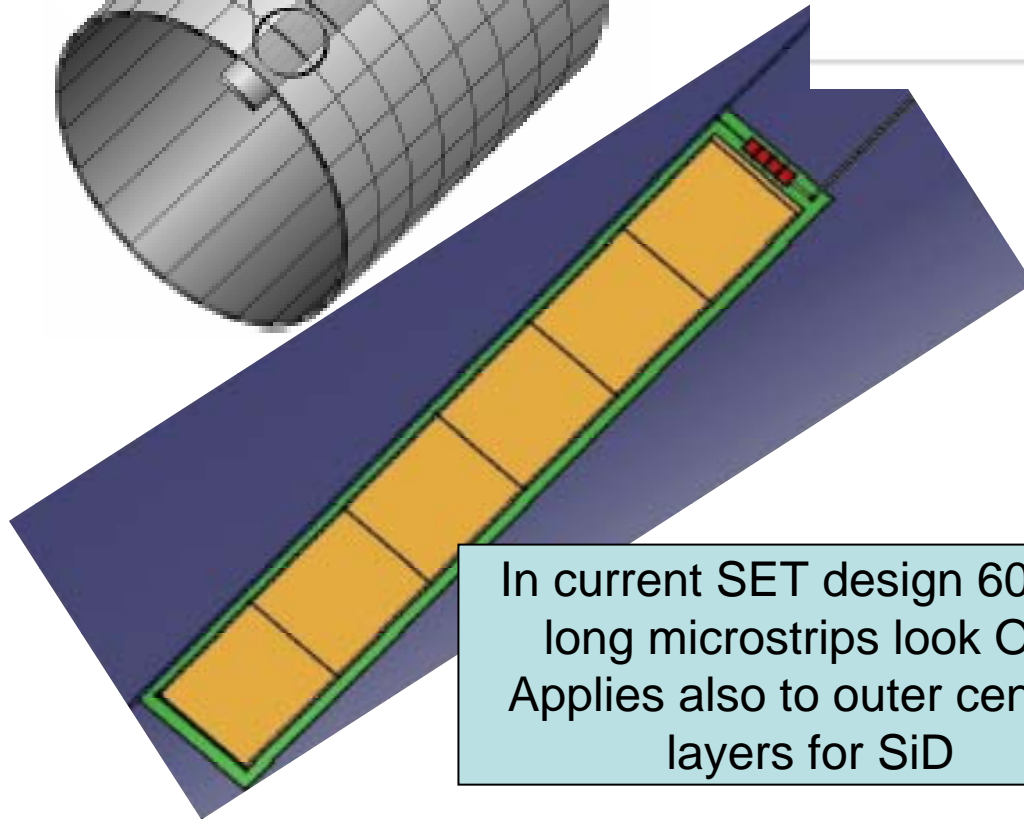
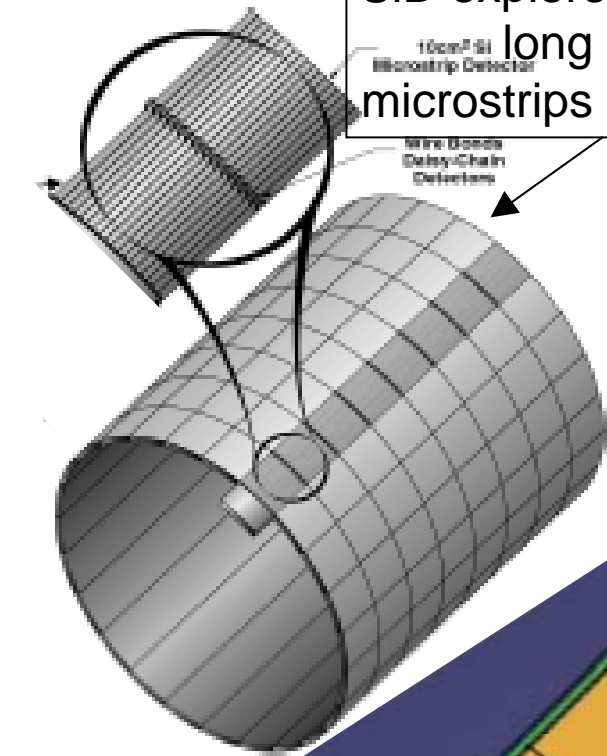
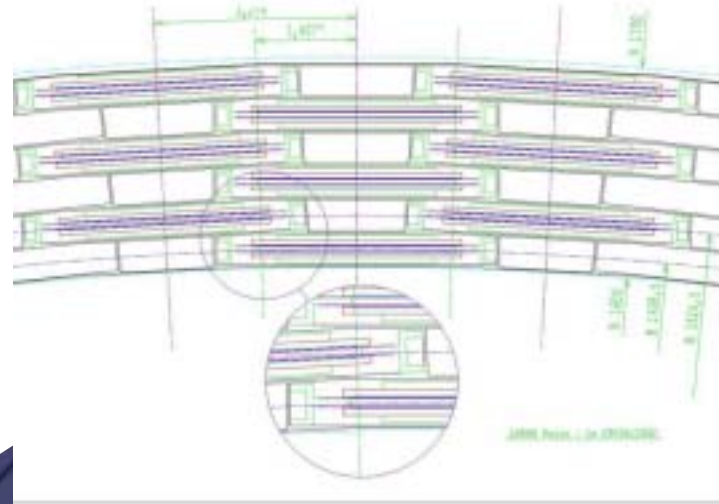
- If a TPC: SET (Silicon External Tracker) proposed in LC-DET-2001-075. Located between TPC and e.m. calorimeter
- Optimized with 3 layers, two single sided external layers, one d.s. intermediate layer and overall structure based on alveoli.



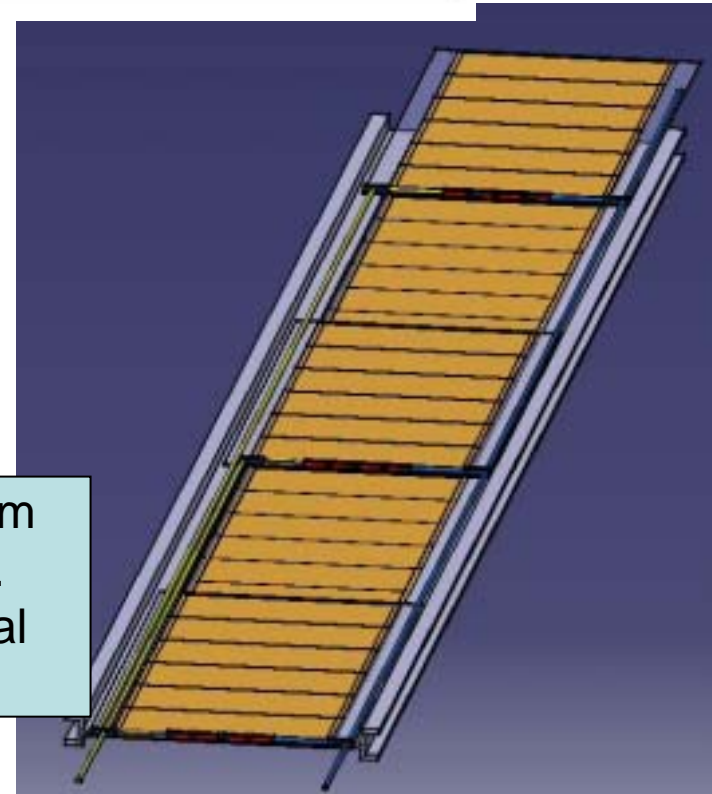
## Central Outer Si layers: current design

SiD explores very long microstrips or tiles

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In current SET design 60 cm  
long microstrips look OK.  
Applies also to outer central  
layers for SiD

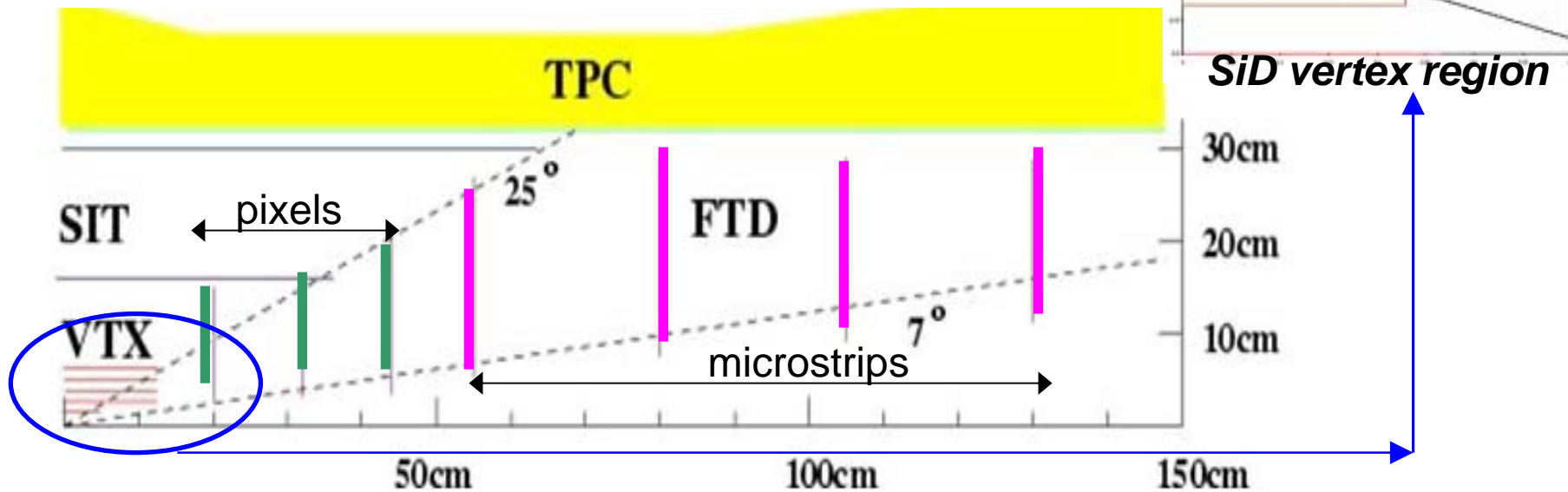


# Si tracking components in Forward region

*The forward region is a key-region for Physics at the ILC c.m. To have highly performing tracking system at large angle is therefore mandatory  
The overlap between central & forward tracking must be taken care of.*

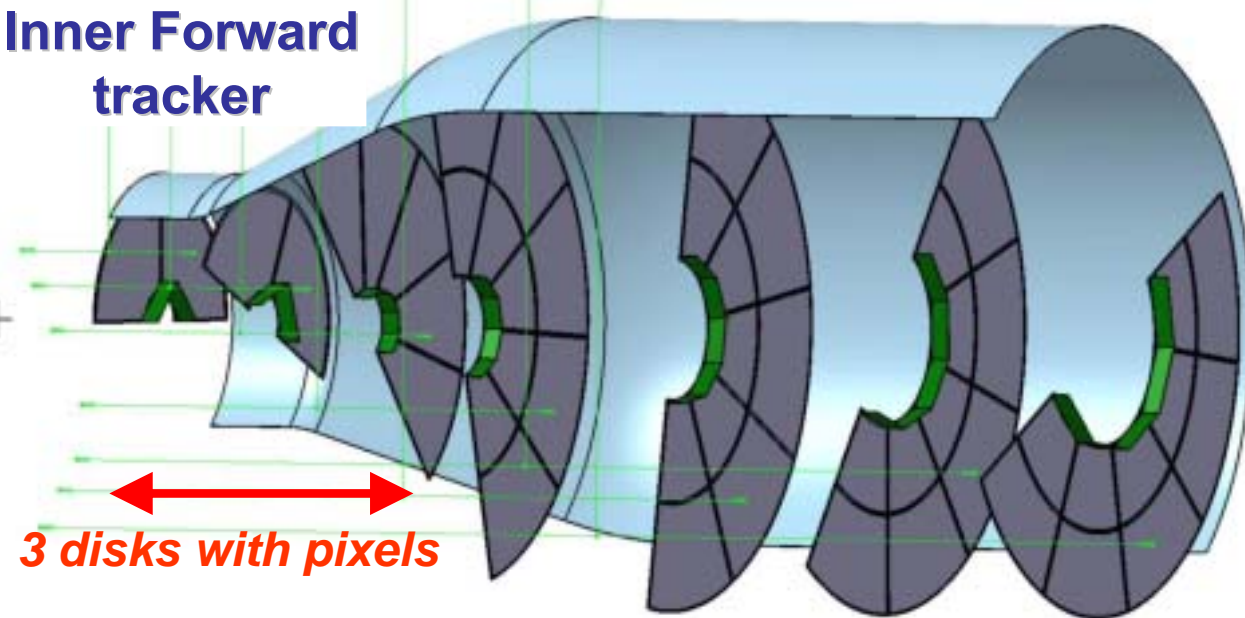
## 3) The inner forward Si tracking component:

covers between  $25^\circ$  to  $7^\circ$  wrt beam axis. No TPC. Links VTX to tracker with TPC end cap in between.



3 first disks: pixels ( $50\mu \times 300\mu$ ), the 4 next ones: microstrips

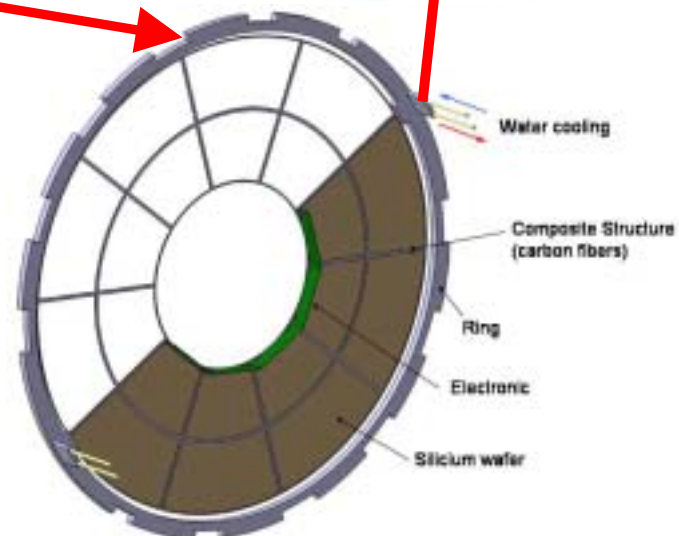
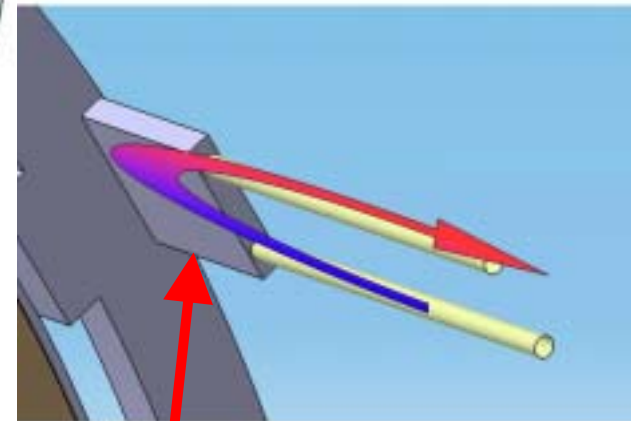
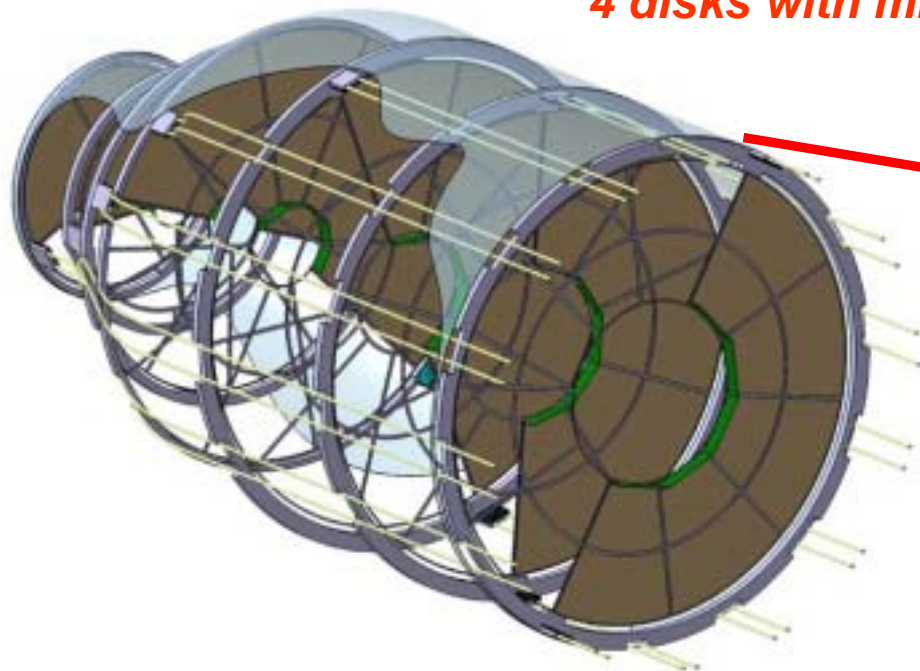
# Inner Forward tracker



*Cooling under study:  
based on water cooling  
with water  $T < 10^{\circ}\text{C}$ , flowing  
through the rings  
(to be checked on  
mechanical prototype)*

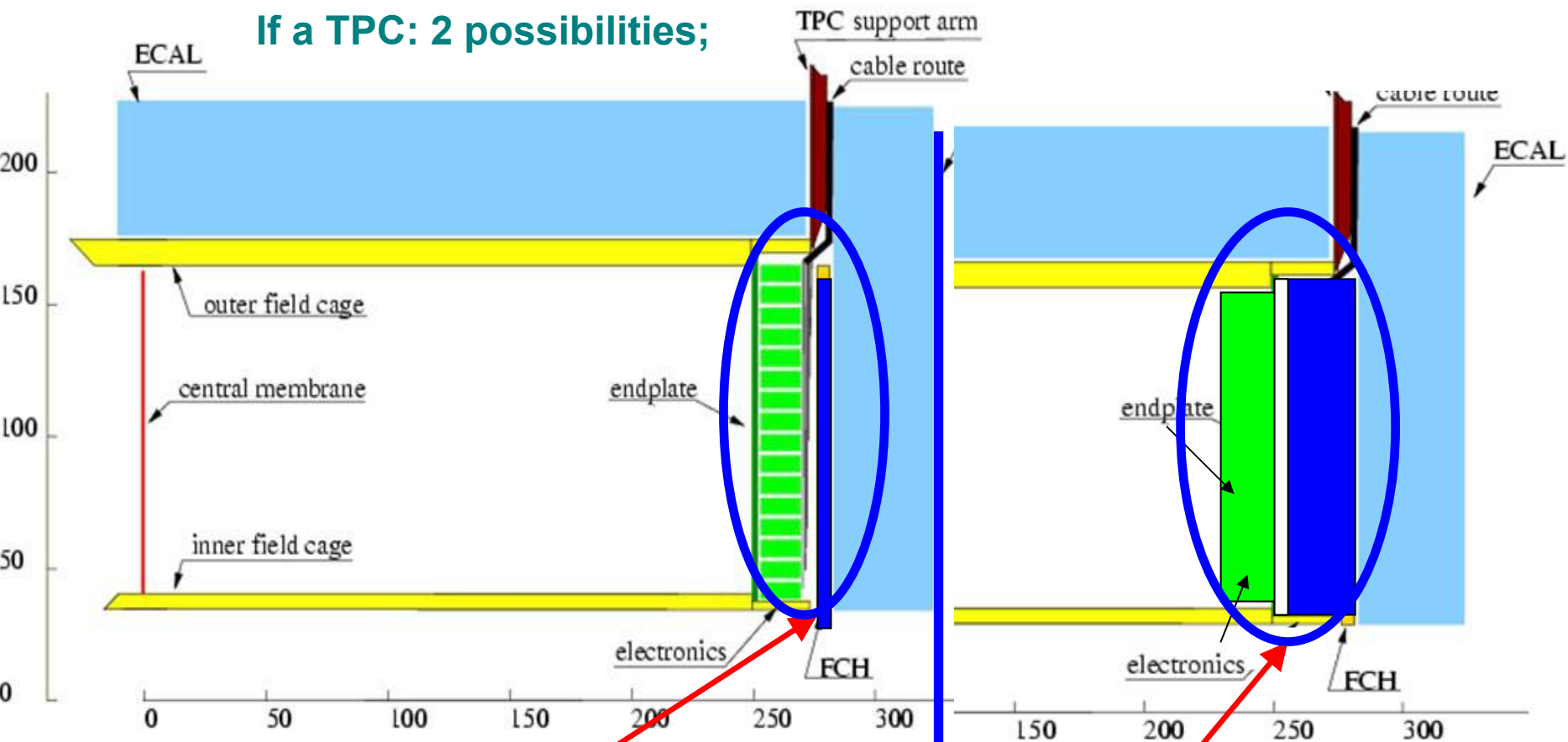
*3 disks with pixels*

*4 disks with microstrips*



## 4) The Forward Outer Si component:

If a TPC: 2 possibilities;

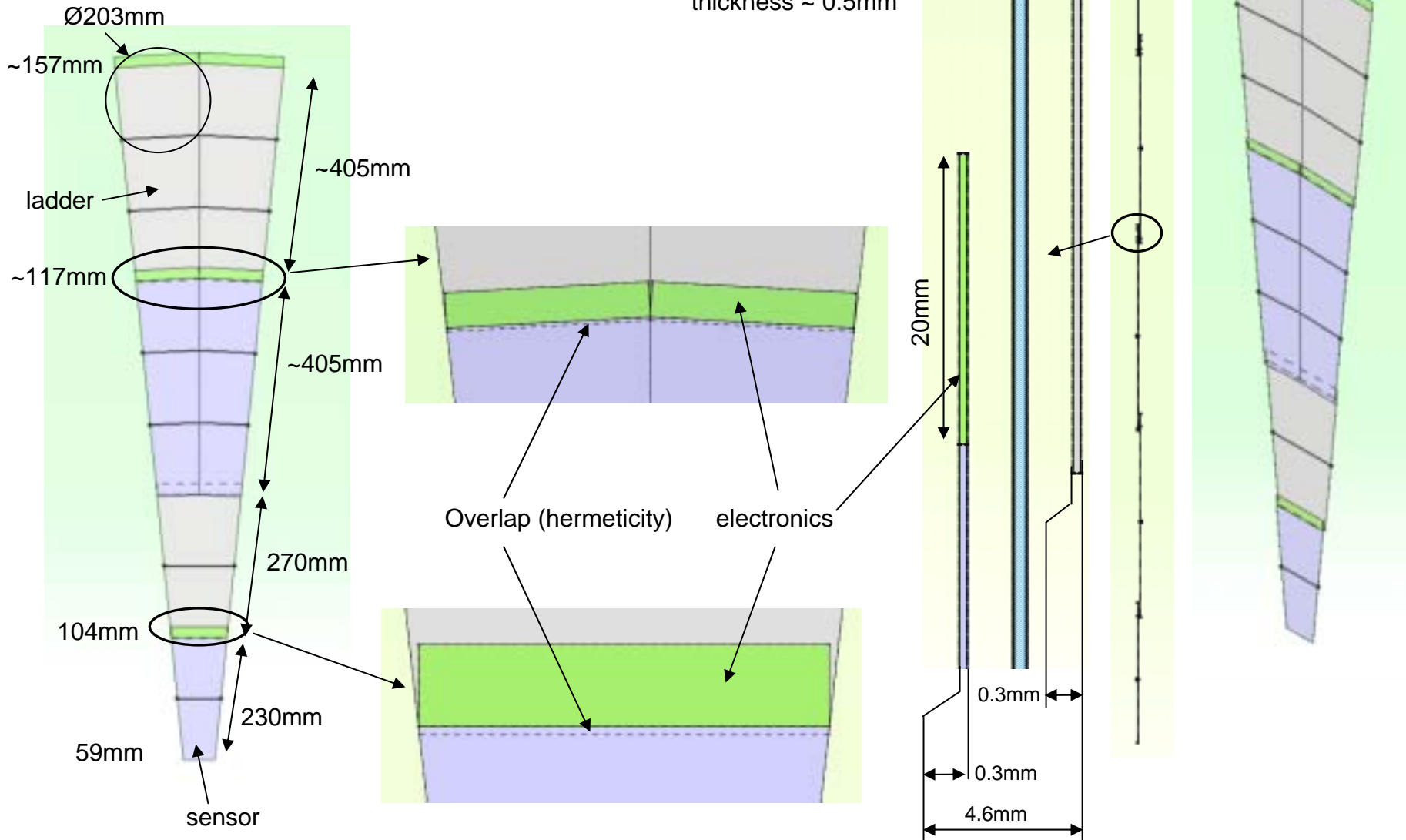


The external forward Si-tracker is compressed between TPC endplate and the calorimetry. Thus it is more a linker than a real tracker.

The external Si-tracker is extended over about 40 cm thus it provides a real tracking (level-arm) (this means a shorter TPC)

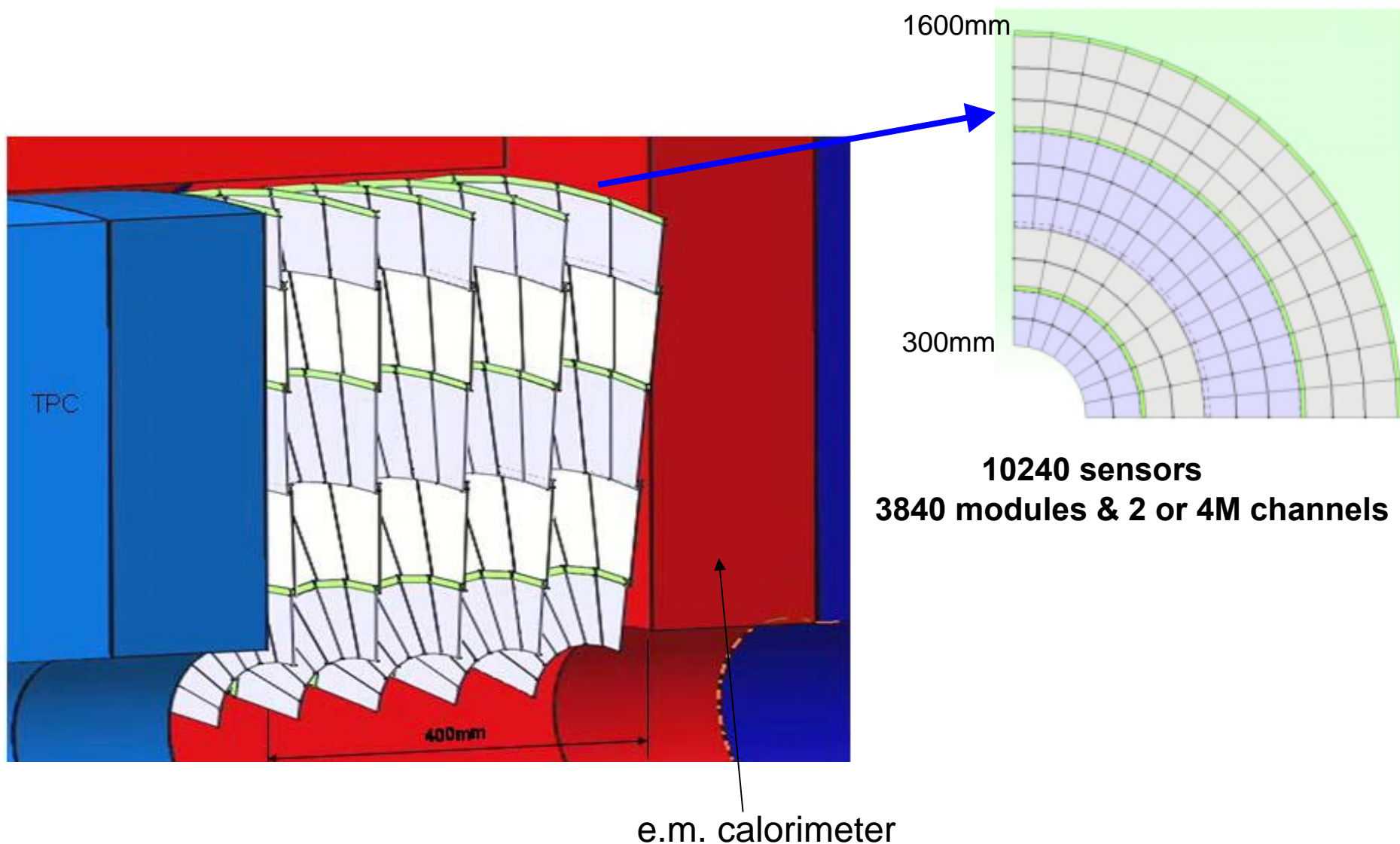
***Simulation studies needed !!***

# FORWARD SECTOR



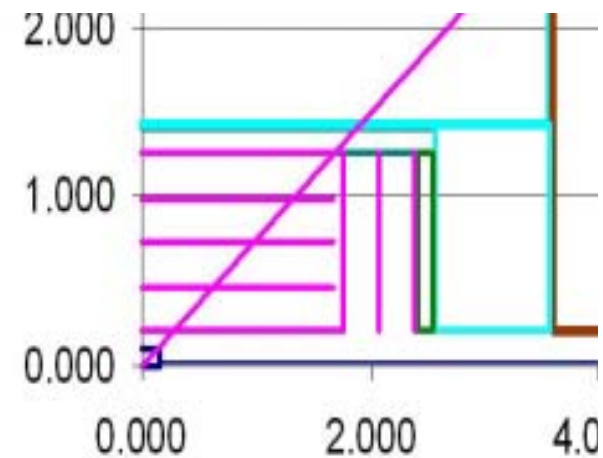
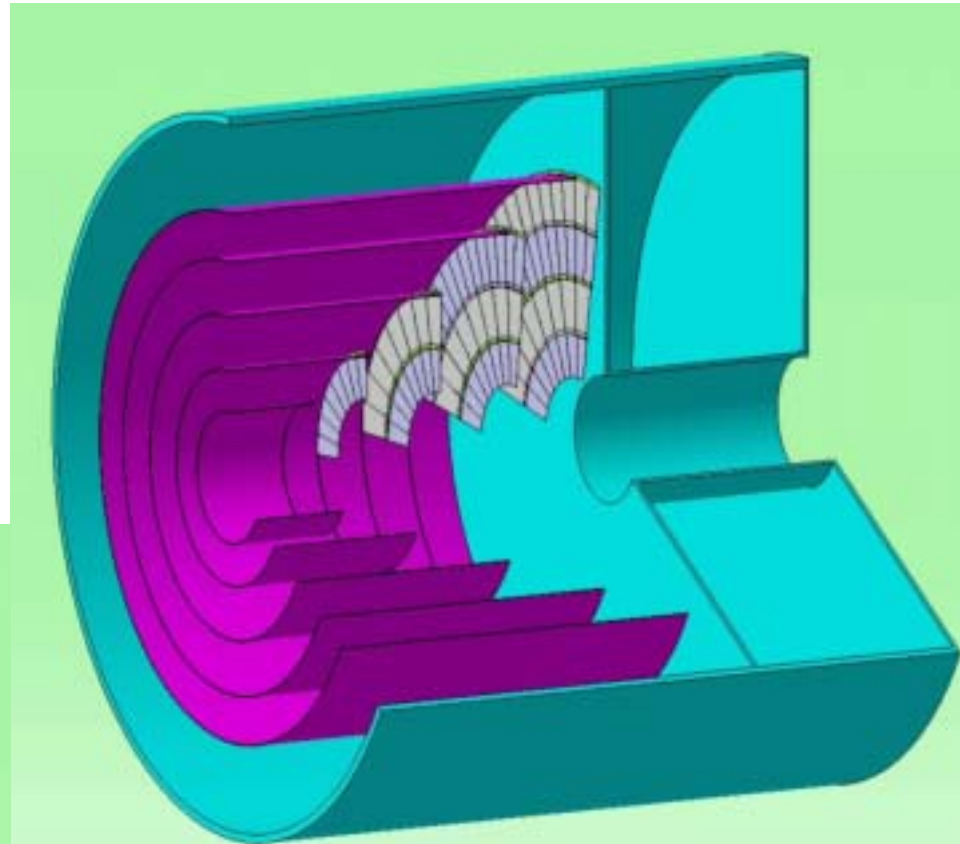
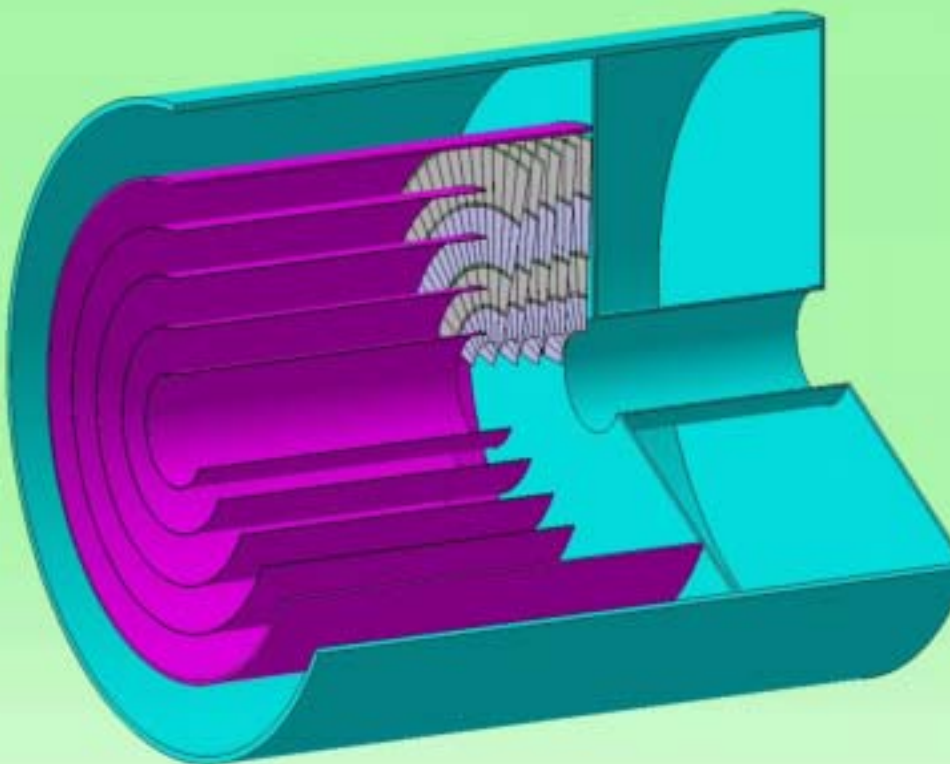
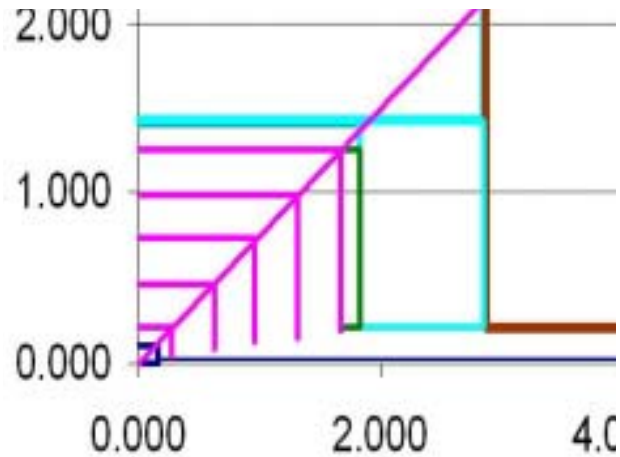
Si-FCH - ILC

## Forward external tracker: overall integrated view



***This CAD design can be included in the geometry DB for the G4 simulation studies in this region***

***How it compares with the SiD Forward tracking ? Important key issue to evaluate the two detector concepts***



# Some common issues to achieve these roles & goals

- Detector modules and sensors: R&D and study of performances
- Cooling: thermo-mechanical studies
- Front-end and readout electronics
- Integration
- Detailed simulations

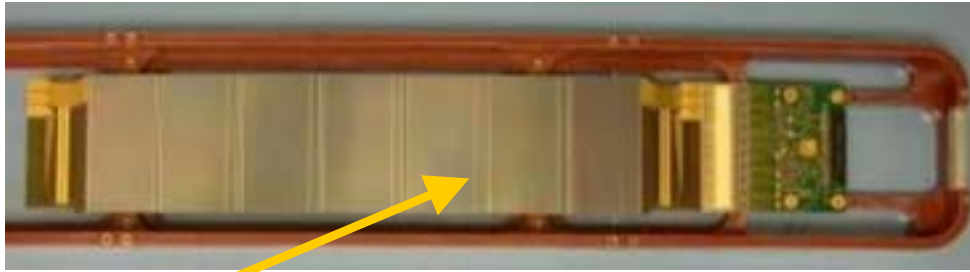
**Basic element of the Si-tracking  
architecture:**

**the detector module**

**Main issue: to have larger wafers  
( $\geq 8''$ ) and thinner.**

**Present Hamamatsu Monopoly**

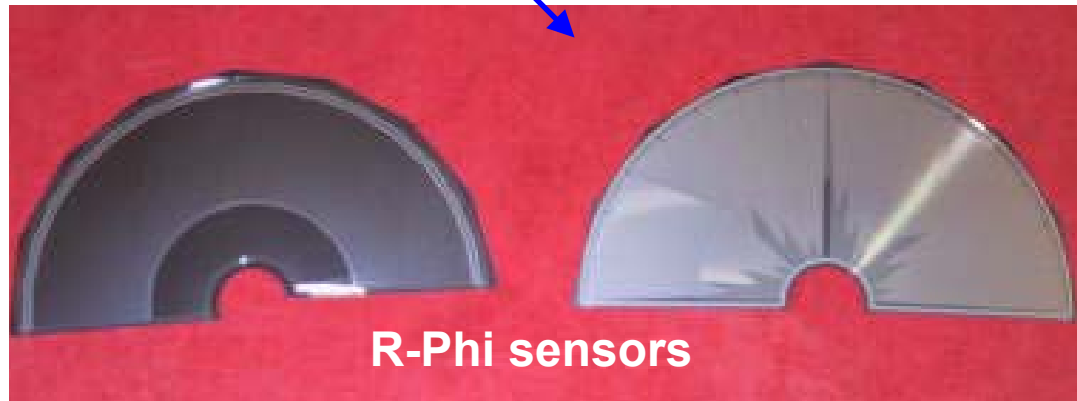
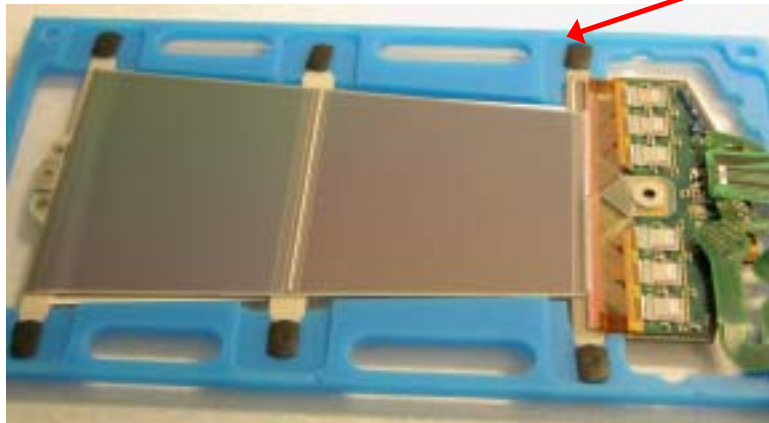
# Various types of modules are considered depending the location of the Si-tracker and the requested performances



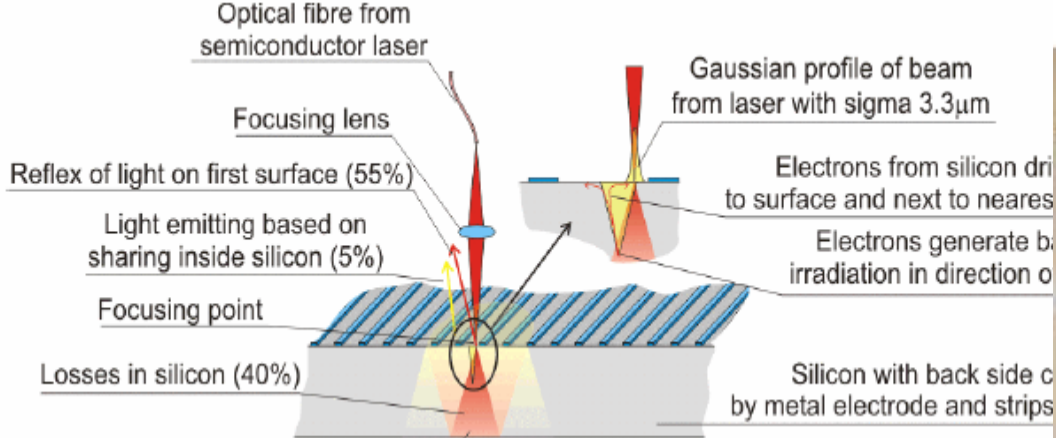
Ladders with  $n=1$  to  $N$  sensors

Inner and outer Si-trackers in Barrel made of microstrips of different length, depending the detector location (occupancy). ILC allows relatively long microstrips  
Two typical lengths: 30 and 60 cm

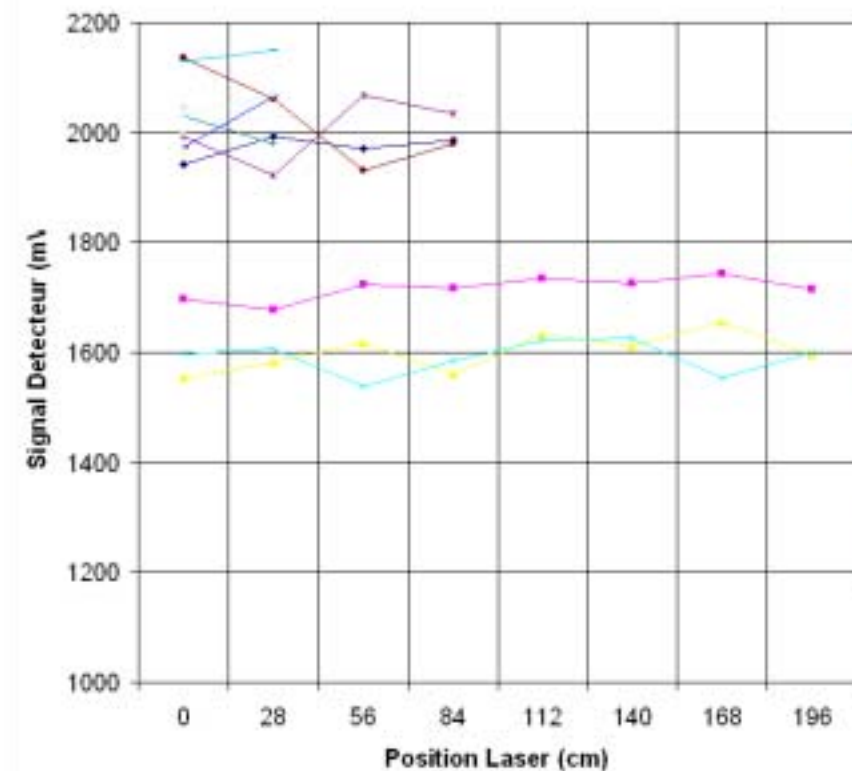
In the FWD region due to the local geometry (disks or octagons), various sensor shapes are under considerations. Mainly based on present experience from LHC experiments.



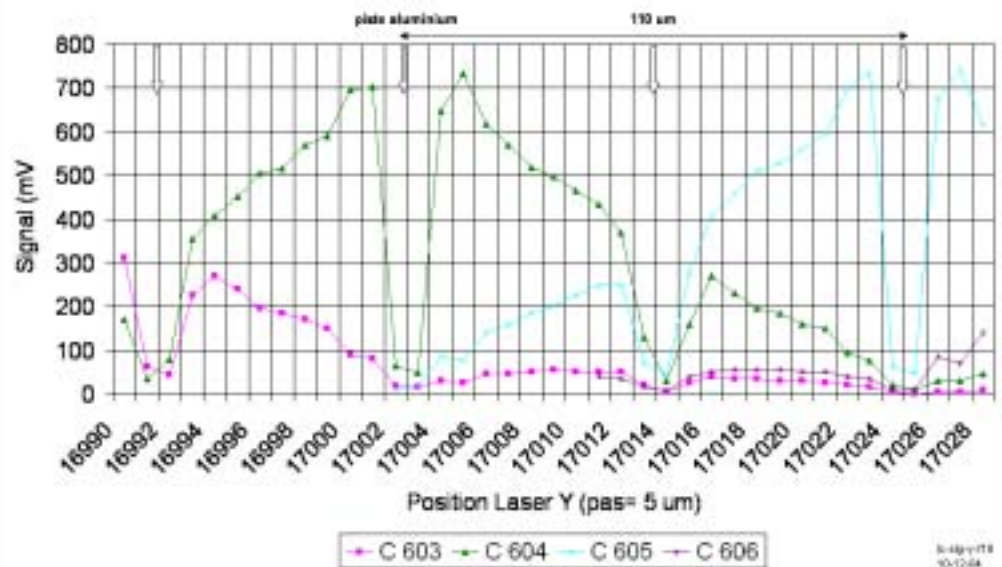
R-Phi sensors



**SIGNAL DETECTEUR / POSITION LASER**  
(Pulse 4,8 ns 1300 mV)

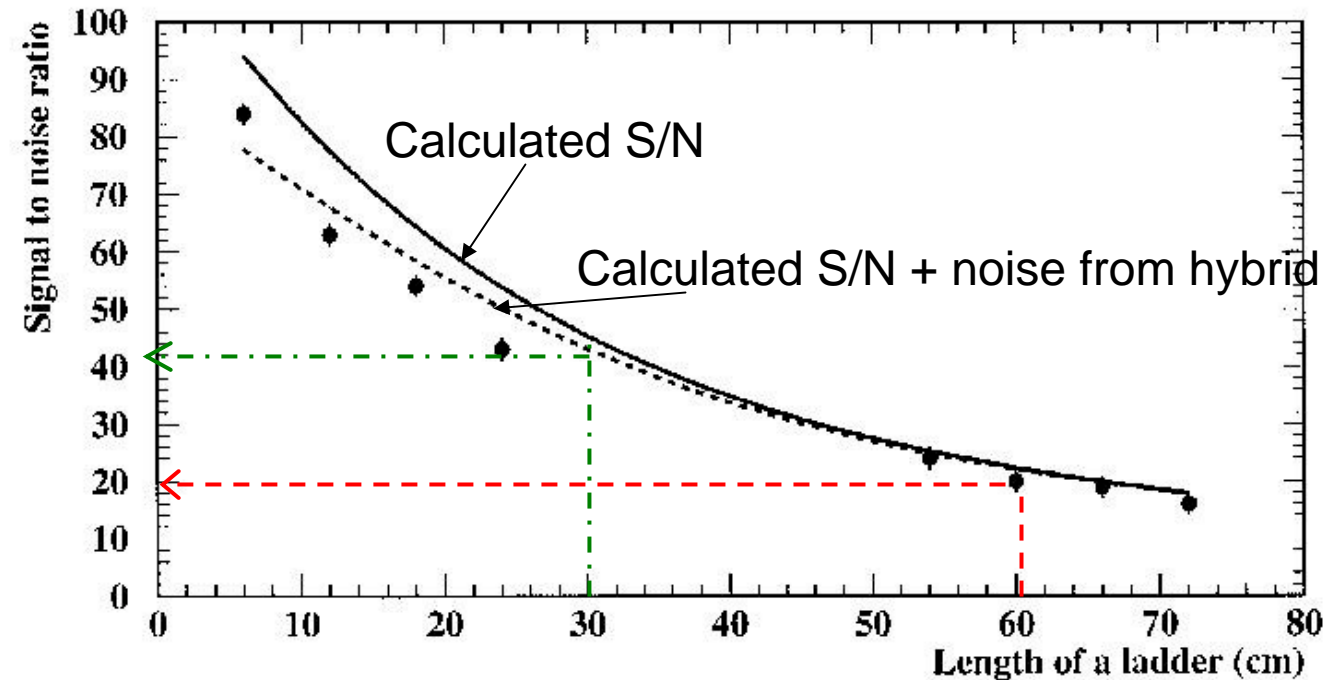
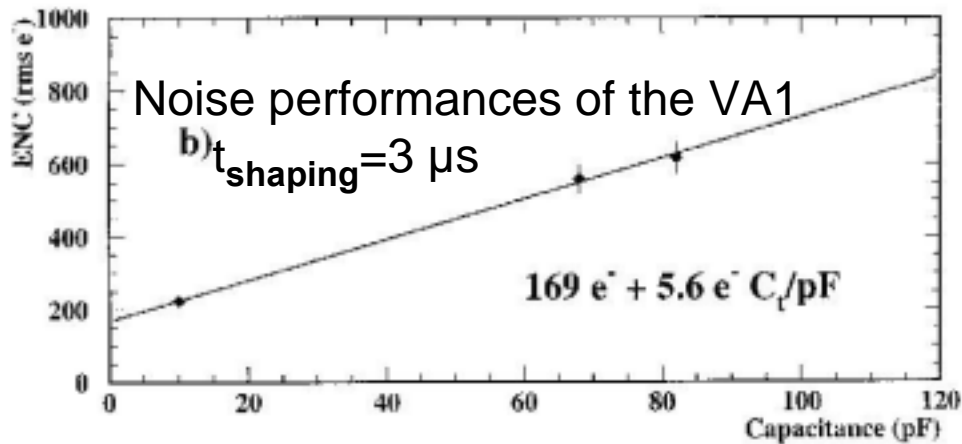


**SIGNAL / POSITION LASER**  
laser LD1060 avec collimateur F = 18 mm T = 50 ns



## Performances of silicon microstrips vs length

NOMAD vertex detector: NIM A 413(1998)  
sensors and VA readout: similar to  
present set-up



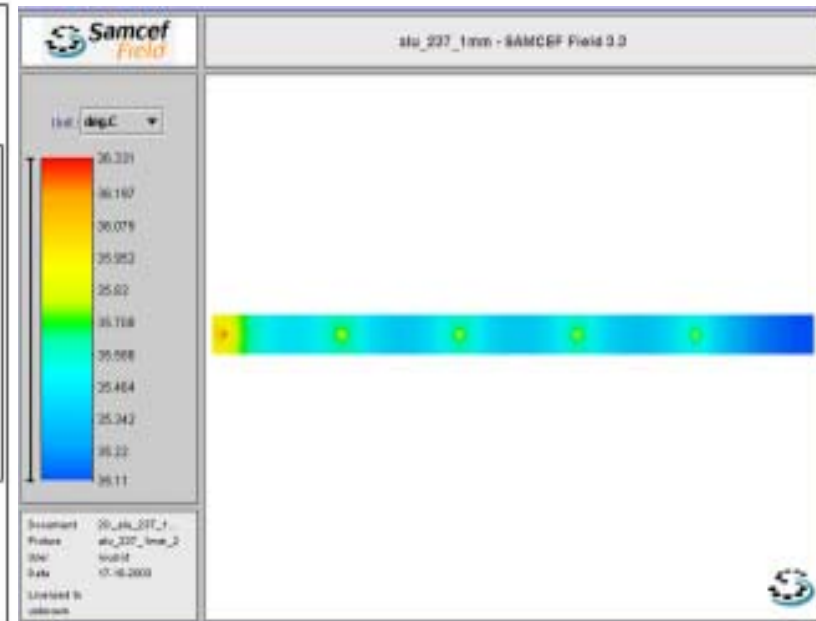
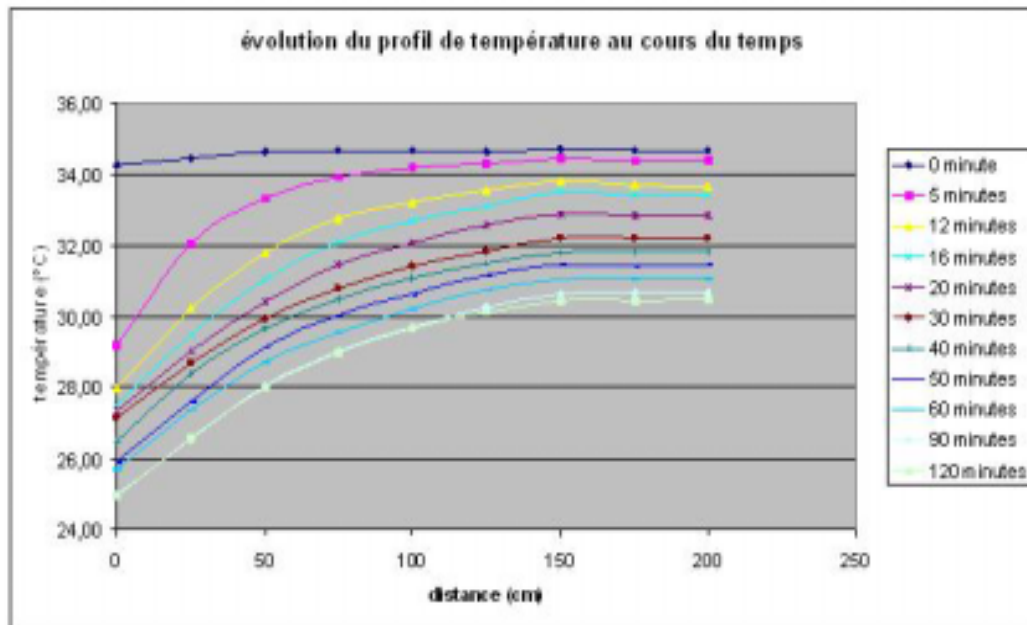
**S/N for 30 cm long  
microstrips: 40;**  
**For 60 cm long  
microstrips: 20**

**Underway:**

**Measuring S/N for longer strips & other sensors (new Hamamatsu) & new  
readout chips**

# Thermo-mechanical studies: essential in the quest for low material budget

- Detailed study on prototype for the external Si tracker: Air convection is good enough to ensure the proper cooling in this detector location

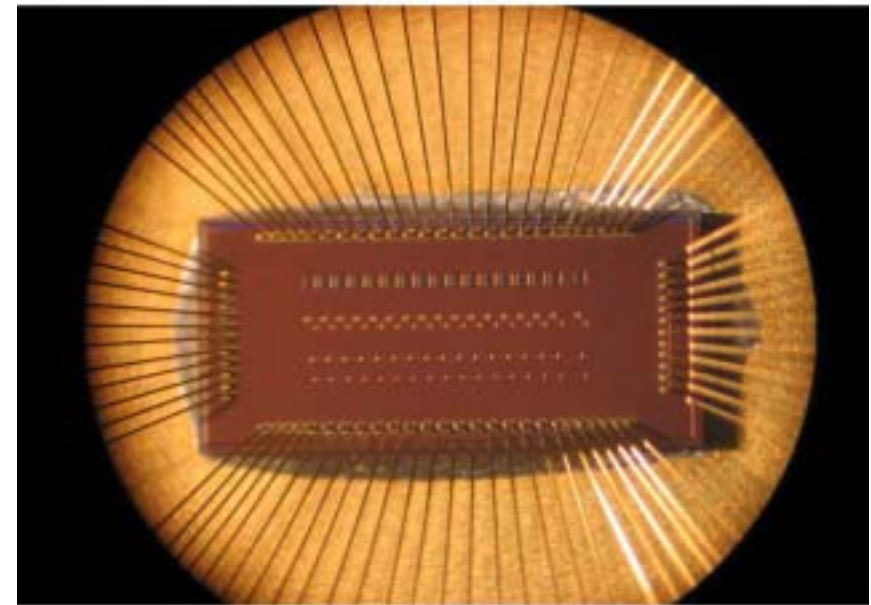
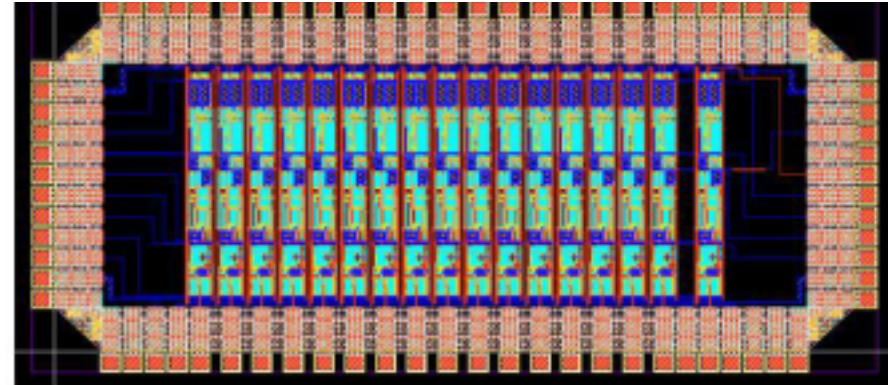


- Studies are just starting for the internal Si-tracker and for the forward tracker. Need informations about environmental conditions in those regions.

# FE readout electronics

## Goals:

- Low noise preamplifiers
- Shaping time (0.5 to 5  $\mu$ s)
- Very low power dissipation
- Highly shared ADC
- Digitization @ sparsification
- Power cycling
- Compact and transparent
- Choice of DS $\mu$ E



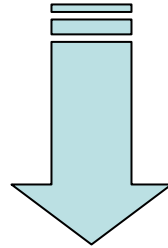
3 mm

Chip received Feb 28

*Very preliminary first results: very promising (see J.F. Genat's talk)*

# Material budget or Slimness

**The material budget is an issue we are confident we will overcome**



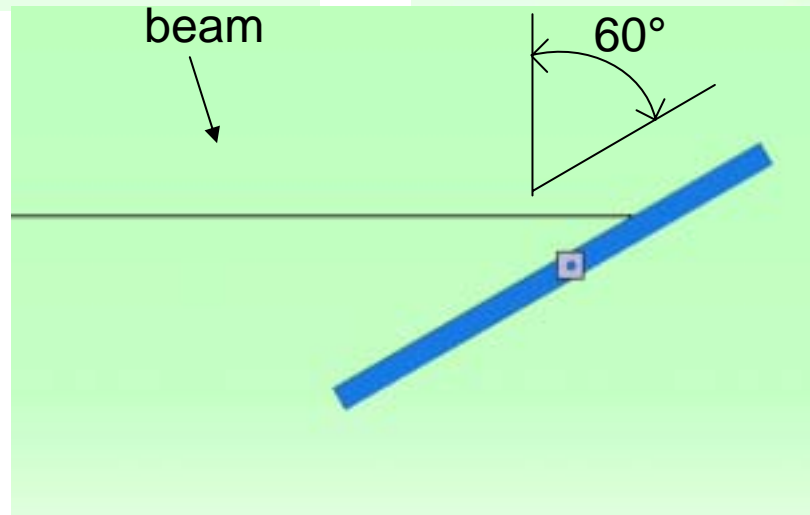
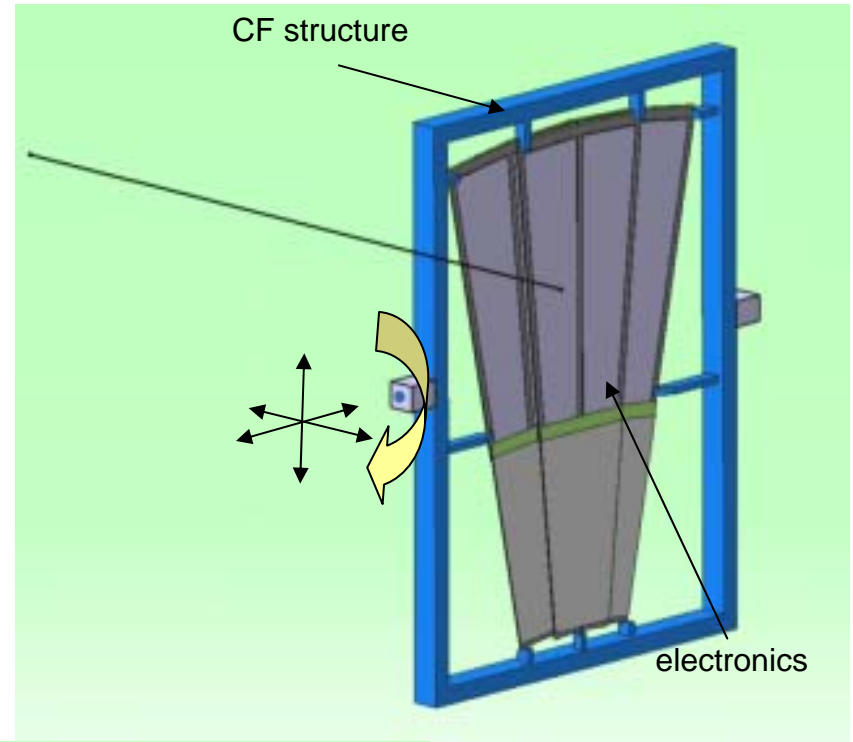
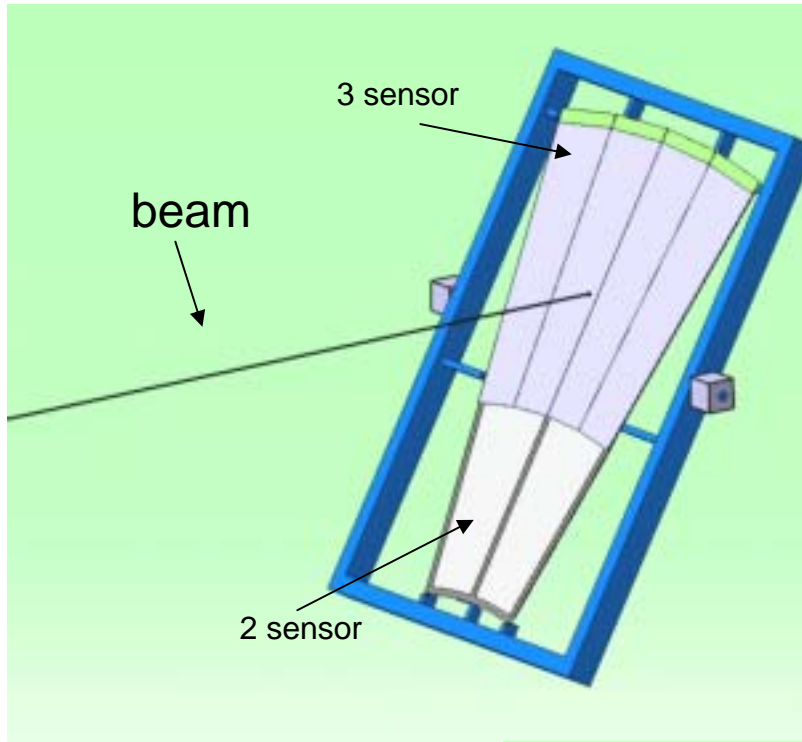
**Exploring and developing several ways to improve it both on mechanics and electronics**

**(optimization of support structure, choice of materials, detector architecture (integration), cooling (passive), electronics on detector (dsm), cabling and connectics).**

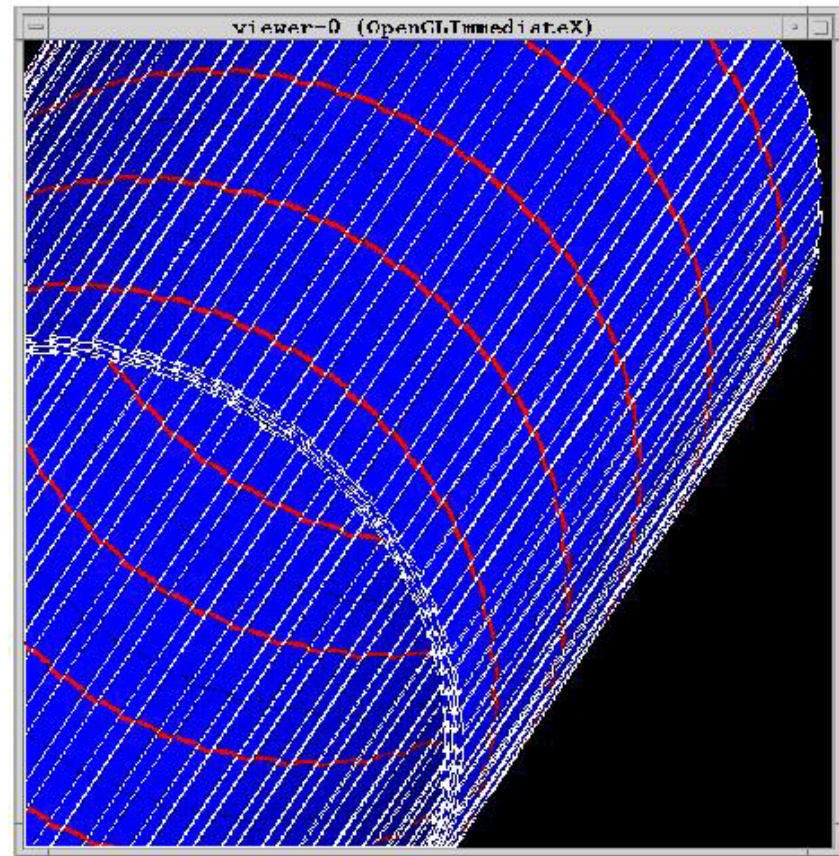
- ▶ **Taking advantage of the technological advances and**
- ▶ **Benefiting from all the R&D work for Tevatron II, for LHC and of the SiLC framework.**

# Test beam: next important step (fall 2006)

## Design of a forward detector prototype has just started



# SIMULATIONS



Silicon Tracker Envelope in Mokka (G4) framework (V. Saveliev)

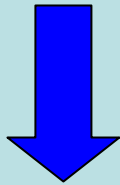
**Dramatic need for a task force on simulation studies for optimising/comparing detector designs & performances**

# Concluding remarks

**Detector with TPC: LDC or GLC**

**Need for Silicon tracking:  
At least 2 crucial reasons:**

**Robustness  
Overall angular coverage**



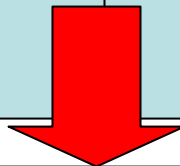
**Much better with Si tracking**

**All Si tracking: SiD**

**Need for a real tracking system  
and not only a simple  
“track linker”  
between microvertex and Si-W**



**Better have a highly performant  
Si tracker**



**Both detector concepts need highly performing Silicon trackers  
with very similar conceptual designs.**

**Most of the R&D issues are common to both detector cases  
All the related R&D aspects are addressed by the SILC Collaboration:  
Just join us**