A Swift and Slim Flavour Tagger exploiting the CMOS Sensor Technology

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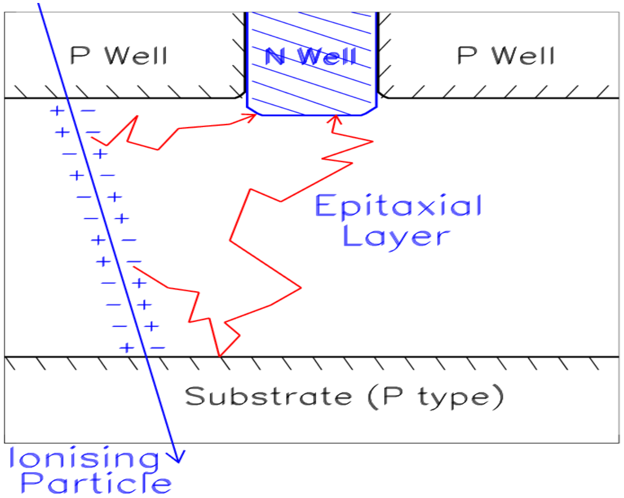
- Reminder: main features and advantages of CMOS sensors
- Demonstrated performances and fabrication processes explored
- Specific aspects of a VD based on CMOS sensors
- Status of the main R&D directions:
  - spatial resolution and ADC design
  - thinning procedure
  - radiation tolerance
  - read-out speed
- Summary and Outlook

Main features and advantages of CMOS Sensors

- Basic detection features:
  - Signal charge ∝ epitaxial thickness
    (~ 80 e^-/h pairs / μm)
  - N wells bound to be charge collectors
  - Sensitive volume mostly unbiased
    (low resistivity Si)

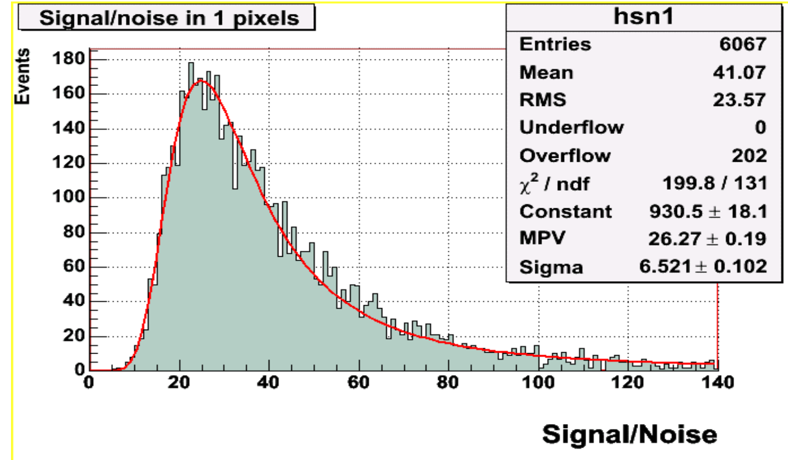


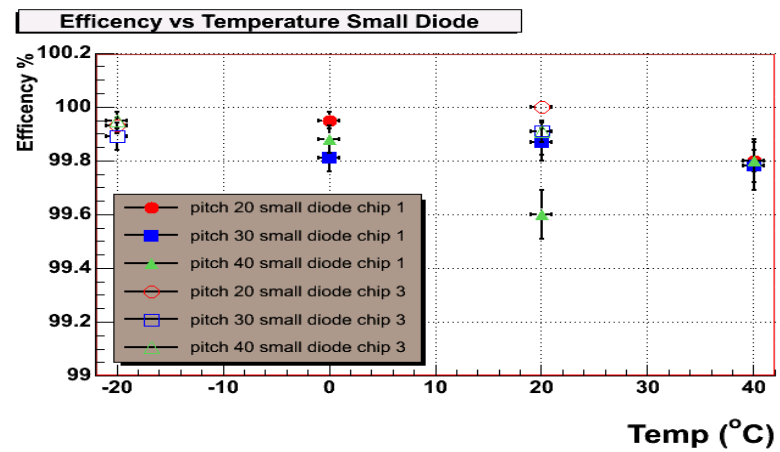
- Main advantages w.r.t. other technologies:
  - Signal processing μcircuits integrated on sensor substrate: inside pixels (NMOS transistors, capacitors) & on chip periphery
    - ➢ System-on-Chip (SoC)
  - Sensitive volume (~ epitaxial layer) is ~ 10 μm thick
    - ➢ sensors may be thinned down to < 20 μm)
  - Standard, massive production, fabrication technology
    - ➢ cheap, fast turn-over

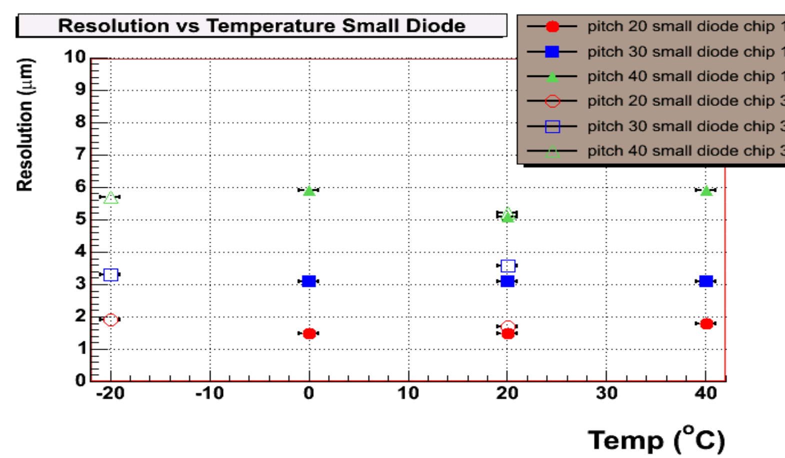
➢ Attractive trade off between granularity (σ_{sp},σ_{2hits}), material budget, read-out speed and radiation tolerance

Performances Achieved with MIMOSA chips

- 11 MIMOSA prototypes designed and fabricated since 1999
- 6 fabrication processes explored:
  AMS-0.6μm, AMI-0.35μm, AMS-0.35μm (opto and ordinary), IBM-0.25μm, TSMC-0.25μm
- Most chips tested with ~10^2 GeV/c π^- **(CERN-SPS)**
  - S/N ~ 20-30 (MPV) ⇨ ε_{det} ~ 99-99.9 %
  - σ_{sp} = 1.5-2.5 μm (20 μm pitch) ; σ_{2hits} ≥~ 30 μm
  - Rad. Tol. For ILC conditions checked with neutrons and X-Rays
  - Reticle size chip fabricated and working well (e.g. imager)
  - Assessment of 50 μm thinning under way
- Application to STAR, CBM, etc.

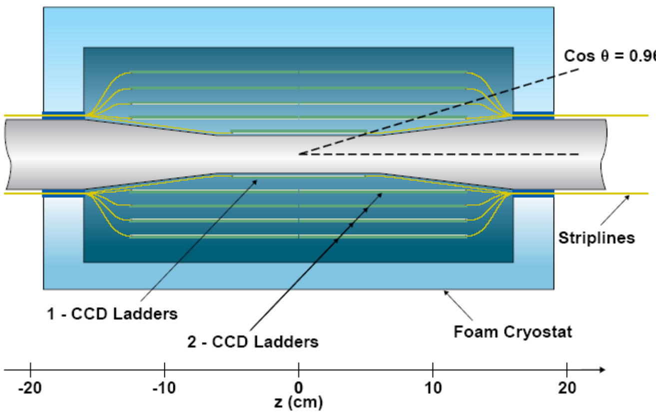






Specific aspects of the CMOS VD concept

- Overall design a priori very similar to TESLA TDR concept (CCD):
  - 5 cylindrical layer
  - R = 15 – 60 mm
  - surface ~ 3000 cm^2



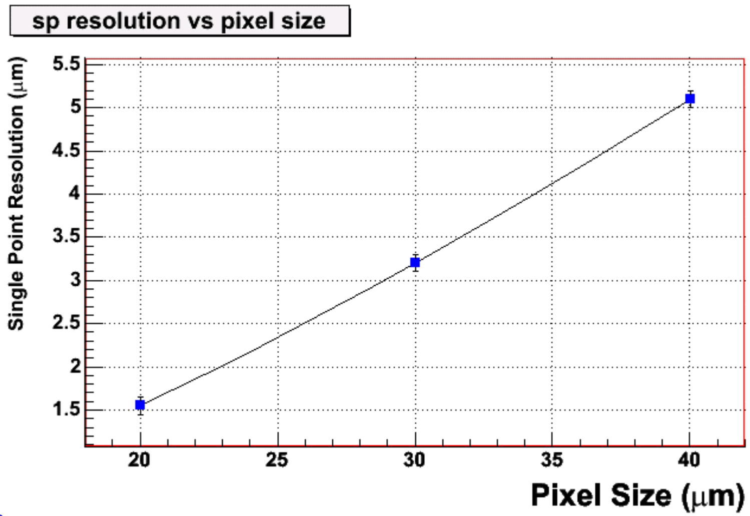
- Basic characteristics:
  - sensor thickness ~ 25-50 μm
  - total number of pixels ~ 300 millions
  - P_{diss}^{mean} ~≤ 25 W **(full detector; 1/20 duty cycle)**
  - operating T < 0° ?

Layer	Pitch	$t_{r.o.}$	N_{lad}	N_{pix}	P_{inst}^{diss}	P_{diss}^{mean}
L0	20 μm	25 μs	24	30M	< 120 W	< 6 W
L1	25 μm	≤ 100 μs	16	70M	< 80 W	< 4 W
L2	30 μm	200 μs	24	70M	< 100 W	< 5 W
L3	35 μm	200 μs	32	70M	< 110 W	< 5 W
L4	40 μm	200 μs	40	70M	< 125 W	< 6 W

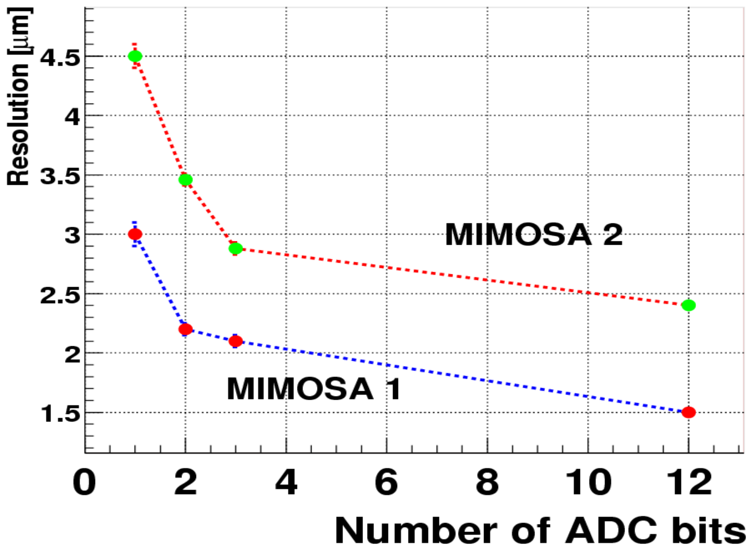
- Main R&D effort concentrated on achieving fast CMOS sensors:
  large data flow ⇨ signal processing (sparsification) integrated/chip

Spatial resolution vs digitisation

- Single point resolution of MIMOSA-9 as a function of pitch ($\sim 10^2$ GeV/c π^- at CERN-SPS)
  - $\sigma_{sp} \sim 1.5\ \mu m$ (L0)
    $\sim 4\ \mu m$ (L4)
    with 12 bit ADC encoding



- Effect of digitising MIMOSA-1 & -2 charges on 1,2 or 3 bits
  - $\sigma_{sp} \sim 2.5\ \mu m$ achievable
    after compact digitisation (3-5 bits)



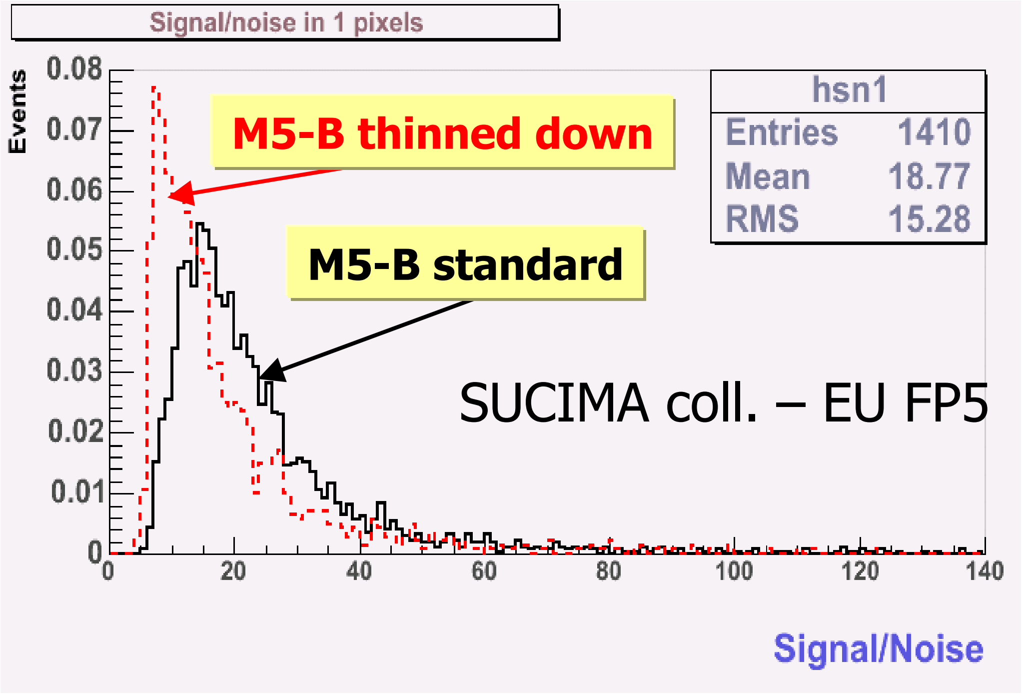
- Design studies of fast ADC integrated at end of each column starting:
  – Baseline: 4 bits
  – Requirements:
    20-40 μm x 1 mm; > 10 MHz; < 500 μW

The issue of thinning

- 120 μm sensor thickness repeatedly achieved on MIMOSA-5 wafers
  ⇨no performance loss observed
  (several chips tested)

- Goal: chip thickness ~ 25-50 μm (mounted on extra-light support)

- MIMOSA-5 chips thinned to 50 μm, outcome assessment under way via LBNL for STAR VD upgrade

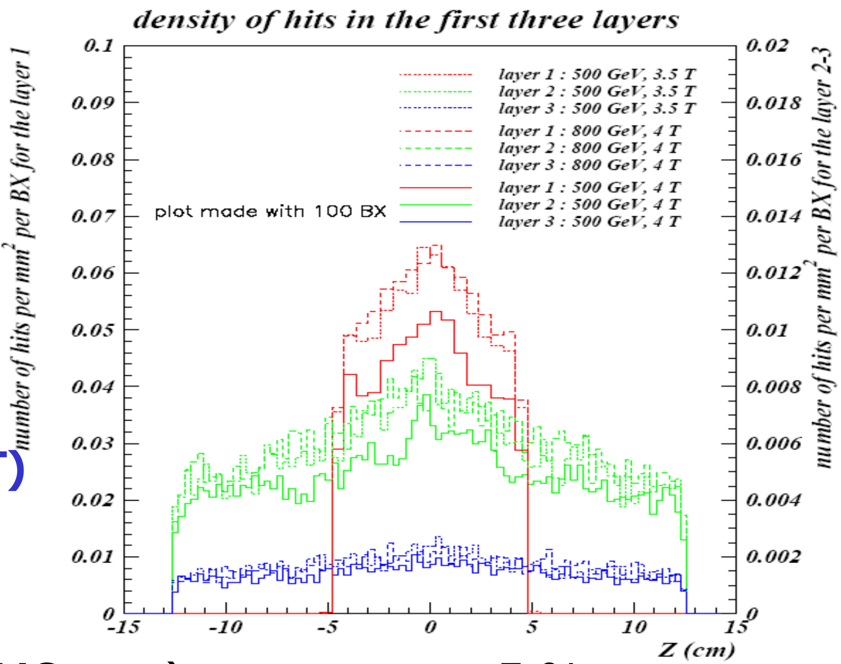


- Substrate removal achieved with MIMOSA-5 (≥~ 15 μm thickness) for O(10 keV) electron detection (EB-CMOS) ⇨detection efficiency drop observed (due to Q loss)

- Substrate removal is not (yet) the solution: optimal solution would be an etch stopper buried in the substrate at 25 μm depth
  - BUT: commercially not available today ⇨ under investigation

Constraints from beamstrahlung background

- Characteristics (from Monte-Carlo !!!)
- $e^{\pm}_{BS}$ have essentially low momentum
  ⇨ very sensitive to B_{exp}=4T
  ➢ Only $e^{\pm}$ with p ≥~ 9 MeV/c (resp. 16 MeV/c) reach L0 (resp. L1)
- ~≤ 5 hits/cm²/BX at 90° **(R = 15 mm, 4T)**



1) Impact on read-out speed:
   ➢ 0.15 % hit occupancy in 25 μs
   ➢ Cluster mult. (5-10), uncertainties (MC, etc.) ⇨ occup. ~≤ 5 %
   ⇨ ~≤ 25 μs needed in L0 and ~≤ 100 (50?) μs in L1
2) Impact on radiation tolerance w.r.t. non-ionising damage:
   ⇨ 6.10^{11} e_{BS}/cm²/yr ⇨ 2.10^{10} n_{eq}/cm²/yr **(NIEL factor ~ 1/30)**
   ⇨ Uncertainties (MC, NIEL, etc.): ~≤ 1.10^{11} n_{eq}/cm²/yr
   (Ionising damage less worrying: ~ 15-50 kRad/yr)

The issue of radiation tolerance

- Non ionising damage:
  1) Neutron gas:
     - **M.C. prediction ~ 10^9 $n_{eq}/cm^2/yr$**
     - **MIMOSA-1/-2 tests (DUBNA): ~≤ $10^{12} n_{eq}/cm^2$ acceptable**
     - **Required tolerance should account for uncertainties (safety factor of 10) and ≥~ 3 years of running: ~ $3.10^{10} n_{eq}/cm^2$**
  2) Beamstrahlung e±:
     - **M.C. prediction ~ 6.10^{11} $e_{BS}/cm^2/yr$ ($2.10^{10} n_{eq}/cm^2/yr$) in L0**
     - **Accounting for uncertainties (M.C.,etc.)**

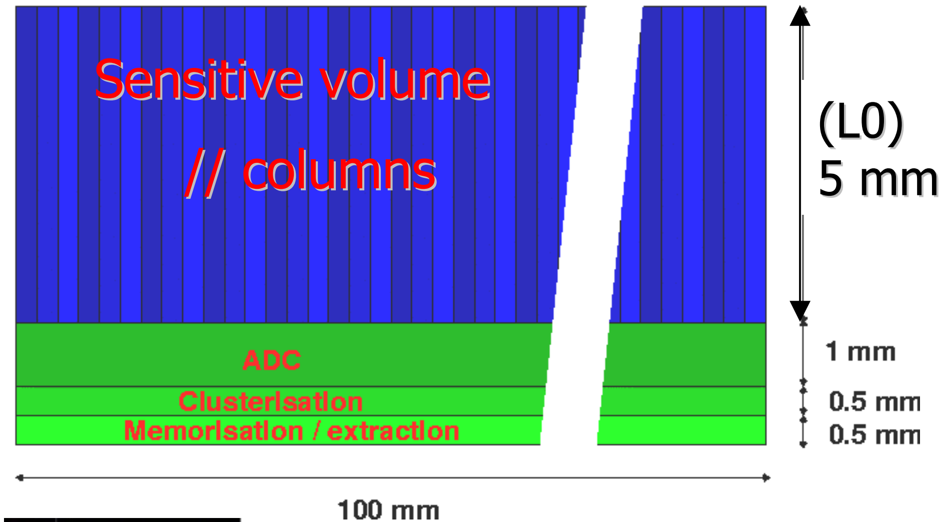
     ⇨ Aim for tolerance to ~≤ 10^{13} e_{BS}/cm^2 (~$3.10^{11} n_{eq}/cm^2$)

     2 MIMOSA-9 chips exposed to 3.10^{12} and 10^{13} e^-/cm^2: analysis under way

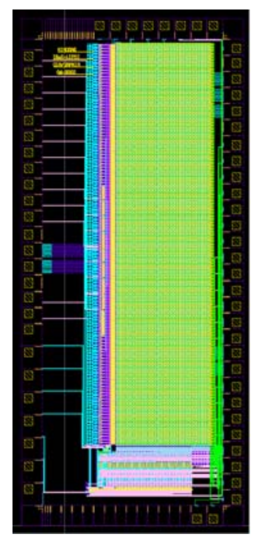
- Ionising damage:
  - **e_{BS}: M.C. prediction ~ 15 kRad/yr**
  - **Aim for tolerance to 150 kRad (3 years, including uncertainties)**
  - **MIMOSA chips exposed to 10 keV X-Rays: no perfo. loss for several 100 kRad**
  - **Proto. designed for bio-medical imaging (SUCIMA – FP5), with dedicated features against rad. damage, stands 1 MRad (X-Rays) without significant loss**
  - **New prototype being fabricated (MIMOSA-11), equipped with various pixel architectures exploring sources of ionising radiation sensitivity**

Achieving high read-out speed

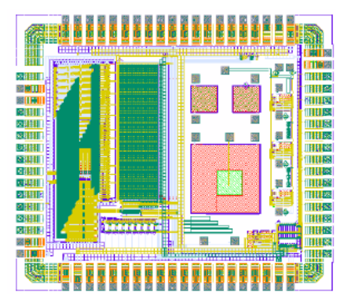
- Fast read-out required in L0 (and L1) ⇨massively // processing
  - ➢ Ladder subdivided in short columns (⊥ to beam) processed in // (serial treatment of pixels inside each col.)
  - ➢ Large data flow
    ⇨ data sparsification integ. on chip



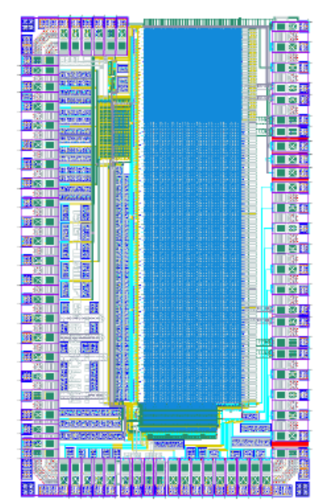
- Develop progressively full r.o. chain on col. par. prototypes:
  - ➢ Inside each pixel: CDS with preAMP (cf MIMOSA-6, -7, -8)
  - ➢ End of each column: ADC + cluster finding + sel. info extraction



MIMOSA-6



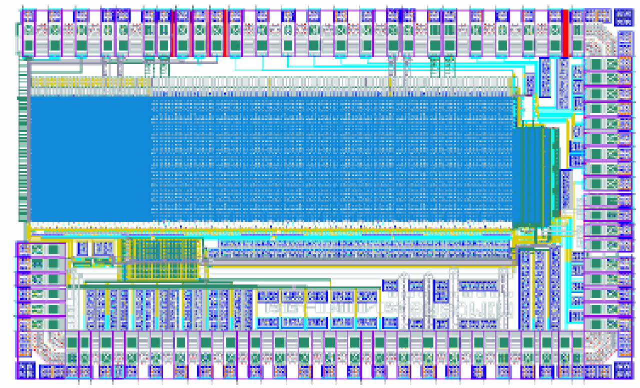
MIMOSA-7



MIMOSA-8

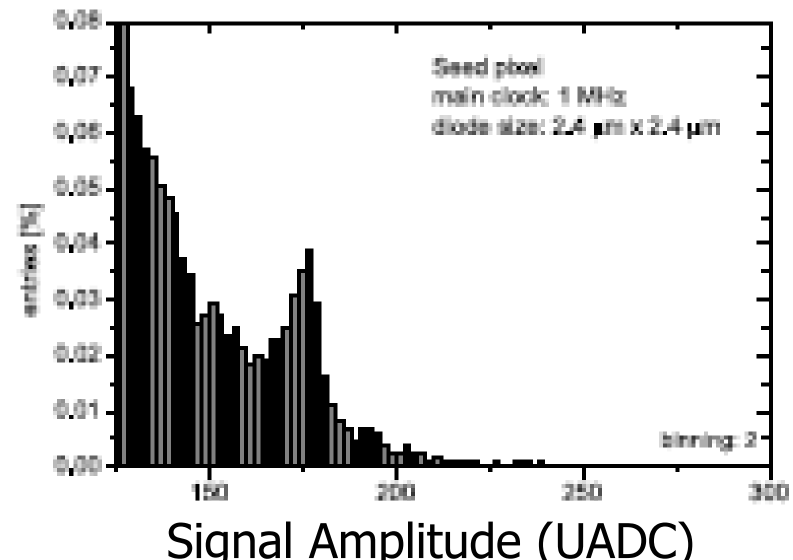
Achieving high read-out speed (2)

- MIMOSA-8 (designed in 2003 with DAPNIA)
  - TSMC 0.25 μm digital fab. process with 8 μm epitaxial layer
  - 32 // columns of 128 pixels
  - Pixel pitch: 25 μm
  - 4 sub-arrays featuring AC and DC coupled on-pixel voltage amplification
  - On-pixel CDS
  - Discriminator at end of each column



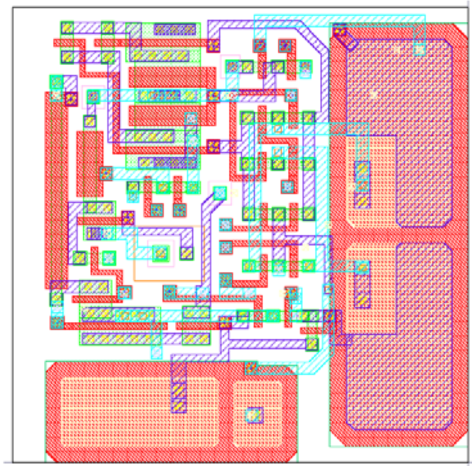
- Test with ^{55}Fe source:
  - ➢ Very encouraging results
  - ▪ Conversion factor: 50-110 μV/e-
  - ▪ Pixel noise (including CDS) ~ 13-18 e^- ENC !
  - ▪ Low pixel-to-pixel dispersion

➢ Architecture seems worth extending with integrated ADC, a.s.o.



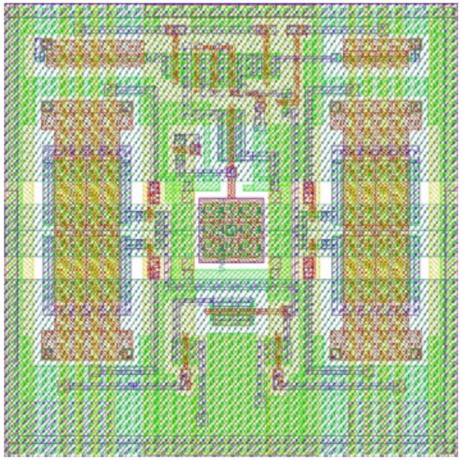
Achieving high read-out speed (3)

- $e^{\pm}_{BS}$ rate is ~ 25 times lower in L2 than in L0
  ⇨ $t_{r.o.}$ ~ 200 μs ⇨ ~ 5 frames / train



- 2 phase micro-circuit architecture, reducing the data flux:
  1) Charge sampled and stored inside pixel during train
     ⇨ 5 capacitors integrated in each pixel
  2) Signal processed in between trains

- 1st multi-capa. pixel: MIMOSA-6 **(design with DAPNIA in 02)**
  Test results: ⇨Large pixel-to-pixel dispersion



- MIMOSA-12: new prototype exploring various types & dimensions of memory cells (scheduled for fab. 25 March)
  - AMS-0.35 μm techno.
  - 4 capacitors/pixel (35 μm pitch)
  - 6 sub-arrays, exploring various MOS capa.: 50, 100, 200 fF
  ⇨ Aim for minimal size capacitors providing satisfactory precision, depending on pitch - i.e. layer - (~ 4.6 fF/μm²)

Summary and Outlook

- Concept of vertex detector using features of CMOS sensors progressing, based on requirements accounting for uncertainties (e_{BS} !)
- Well established performances:
  - **S/N, ε_{det}, σ_{sp}**
  - **Rad. Tolerance to neutrons and X-Rays**
  - **120 μm thinning of Megapixel sensors**
- Most recent achievements
  - **Fast col. // pixel architecture (integrated CDS) found, with low noise (< 20 e^- ENC) and small pixel-to-pixel dispersion**
  - **Assessment of a well performing R&D fabrication process: AMS-035 μm (opto and epi-free) ⇨ very good perfo. even with 40 μm pitch (L4)**
  - **Checks of tolerance to 10-20 MeV electrons under way**
  - **Outcome of thinning to 50 μm under study (≥~ 15 μm not yet OK)**
- Next important steps:
  1) **Fast column // sensor with digital output, adapted to L0-1 (integrated low power, fast and compact 4-bit ADC)**
  2) **New multi-memory cell sensor adapted to L2-4**
  - **Complete study of MIMOSA-5 thinning to ~ 50 μm with LBL**
  - **Investigate characteristics of new fab. processes (e.g. IBM-0.13 μm, UMC-0.18 μm)**
    - **Thinning no-epi sensors is very appealing: any possibility ?**
    - **Privileged contact with a foundry would be very valuable...**

➢ Aim for a fast col. // megapixel proto providing digital output in 2007