Towards a Detector Control System for the ATLAS Pixel Detector

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1 Abstract

The innermost part of the ATLAS experiment at the LHC, CERN, will be a pixel detector consisting of about 1750 individual detector modules. The high power density of the electronics, the harsh radiation environment, and the inaccessibility over long terms are the specific constraints for the design of the pixel detector control system (DCS). Selection and development of adequate hardware components as well as efficient software strategies are required to guarantee the safety of the detector and to support a reliable operation during data taking. The various building blocks of the pixel DCS will be described. Following the recommendations for the LHC experiments we have started to build software units using the Supervisory Control And Data Acquisition (SCADA) PVSS, a commercial software product (Prozessvisualisierungs- u. Steuerungssytem: ETM Co., Austria). We report about the status of our software development and how the complexity of the various detector components can be mapped onto the SCADA system.

2 Overview of the Pixel Detector Control System

As a subdetector of ATLAS, the pixel detector control system must fit in the ATLAS wide system which is organized in three levels. The highest is given by the central DCS station, from where the subdetectors local control stations receive commands and where they return status information to. The local control station, forming the intermediate layer, monitors and regulates the detector hardware. From a logical point of view these two layers are called the 'back-end' system. The hardware, the IO-units and sensors, which are distributed in the detector cavern and in the detector sensitive volume, are representing the lowest level in the DCS hierarchy and are refered to as the 'front-end' system. Figure 1 shows the different levels and gives also an overview of the various building blocks of the front-end, as they will be required for the pixel detector. In the following section we will concentrate on the most important ones. (As there are several contributions to this workshop about the ATLAS pixel tracker, we skip a description of the detector itself.)



Figure 1: Overview of the Pixel Detector Control System

3 The Front-End System

For the operation of the detector and its related electronics several voltages are required: the depletion voltage for the sensors, two low voltages for the front-end chips and the module controller chip and three low voltages for the operation of the optical link. Because of grounding and redundancy considerations a high granularity is aimed for, giving in total about 4000 individual channels. For such a complex power supply system we foresee a system with a high level of local intelligence, which is for example able to react to overcurrent conditions by its own. This helps to enhance the safety of the detector and in parallel reduces the network traffic. Additionally the operation of channel groups is foreseen and the support of our interlock system, see later in this section, must be given.

Due to the high power density of 0.7 W/cm^2 , giving a total power consumption of about 20 kW, an efficient cooling system is required. For this task a system based on evaporative cooling using C_3F_8 was chosen and its successful operation has been proven by several prototypes [1]. A silicon operation temperature of -6 °C was achieved. Such a system helps to reduce the extra material in the tracker sensitive volume; other advantages are that the refrigerant is non-flammable, non-conductive and radiation resistant. Up to 26 detector modules will be cooled by one Parallel Cooling Circuit (PCC). This is the smallest cooling unit, which can be controlled separately.

Another important building block of the front-end system is the Embedded Local Monitor Board (ELMB), a standardized, general purpose front end IO-device developed by the ATLAS DCS group [2]. It owns a 16 bit ADC with 64 channels, 34 digital IO-lines and is radiation tolerant. The connection to the outer world is realized by a CAN-bus interface (Control Area Network [3]). This fieldbus is specially suitable for widely spread applications. For the various monitoring tasks of the pixel system, see fig. 1, we are going to have in total about 250 ELMBs distributed around the surface of ATLAS on a CAN-bus system of up to 150 m length.



Figure 2: Scheme of the Interlock Box

As in particular our irradiated detectors are very sensitive to heat-ups, a special safety circuit is necessary: the thermal interlock system. It protects the sensors against risks associated with de-lamination, latch ups or failures in the cooling system. For this purpose each detector module is equipped with a NTC-thermistor. Its signal is split into two paths. One is sent to the ELMB, where the information is via the CAN-bus lead further to the local control station. This is the standard monitoring chain. The other one is going to the Interlock Box, which will become active, if the standard procedure fails for any reason. As can be seen from fig. 2 the NTC-signal is compared to given thresholds. In case of excessive deviations, logical signals are created which are hardwired to the power supply system and will switch off the related power supply channel. The two bit logic of the output indicates additionally a broken cable or a short circuit. Additionally logic unit offers the possibility to combine signals, see fig. 1. Several prototypes were successfully tested. The overall maximal error of 1 K includes tolerances of the NTCs, which are not individually calibrated, tolerances due to the electrical components of the interlock circuit and effects caused by varying cable properties. Because of the Interlock Box' location in the ATLAS cavern, the radiation tolerances of all components were investigated. A full set of compatible components is now established; further details can be found in [4].

4 The Back-End System



Figure 3: The geographical approach

As the mapping between the hardware components and the software determines the overall project structure, this should be defined first. The aim is to mirror the hardware (thousands of channels) in a clear way, which supports the shifter in understanding the behaviour of the detector. Problems must be made evident and an easy problem tracing is required. Therefore we do not foresee a grouping of channels according to their functionality, in contrary a geographically oriented tree structure is aimed [4]. As can be seen in fig. 3, the top level is built by the pixel detector. The first sublevel is defined by the mechanical structure: the disks and the shells or the half shells respectively. The next level is given by the segmentation of the cooling system, the PCCs. The lowest level is formed by the base detector units (BDU). As the distribution for our power supply system foresees two detector part like temperature, high and low voltages of a detector module, status of the optical link etc. are shown. Having this information a shifter can easily check whether different upcoming error messages are related to the same detector element.

The core of the back-end system is given by PVSS, the SCADA system which is chosen for the LHC detectors. It will be running on the local control station. PVSS' advantages are that it can be distributed over many stations and its flexible and open architecture. Furthermore it offers basic functions for automatisation, standardized interfaces to the hardware and application programming interfaces.



Figure 4: The test beam DCS setup

The basic properties are defined by 'data point types' (ELMB for example), while the logical related process variables are the 'data points' (ELMB-nr.nn for example), which inherit the structure defined by the data point types. Each data point consists of dp-elements (a single channel in ELMB-nr.nn), these elements can be further divided into sub dp-elements and so on. In this way a tree structure is built up. Configuration, reaction to error conditions, and graphical user interfaces are created via control scripts, which are correlated to the data points and its elements.

The data points are filled with physical data via the OPC server (OLE for Process Control), which handles the connection between PVSS and the CAN-nodes. The advantage of this industrial standard interface is the fact that no specific driver for each client is necessary.

5 Test Beam 2002

In summer 2002 the control system participated in test beam campaigns, where the performance of the pixel modules was studied at the H8 beam of the SPS at CERN. Concerning the DCS several questions were studied. Besides the task of supporting the shifter with information, the properties of the thermal interlock system were investigated. As it was the first time that the selected DCS components of the front-end and the back-end system were operated together under data taking conditions, it was a good possibility to explore whether PVSS covers the pixel detector's needs. First experience with the thermal behaviour of the detector modules was gathered. Additionally we aimed to build a system which can easily be expanded for future, larger applications. Fig. 4 shows the hardware setup.

One part is a replication of the final thermal interlock system. ELMB1 builds the standard monitoring path, while IBox (Interlock Box) 1 to 4 and the logic unit are forming the interlock system itself. ELMB2 monitors its output pattern. As the effects of the cables — up to 150 m length will be required in ATLAS — are not negligable, this part of the setup was installed with original cable length for the analog and digital signals, the powering and the CAN-bus. Just a few detector modules were studied in the test beam. Therefore the rest of the inputs to ELMB1 and the Interlock Boxes were equipped with dummy resistors to simulate different temperatures. ELMB3 was responsible for the temperature monitroing of a cooling box, which was used to deliver an adaquate environmental temperature for the detectors. All information was collected by PVSS running on the local control station.

The PVSS program consists of three parts. While the first two of them are mainly handled by the DCS operator, the third part is foreseen for the shifters. During start up the internal project structure is defined. It is checked whether all data point types are available and the data points are created. Some of their attributes like alert settings can be modified. The number of ELMBs actually in use is determined here, the correlation between physical channels and their logical names used in the program is defined.



Figure 5: Synchronisation interval and noise for different ADC ranges

It follows the configuration of the hardware. Operation parameters for the ADCs and the CAN-bus must be set. Therefore the noise of the ADC as a function of its conversion rate was studied, see fig. 5. At a conversion rate of 60 Hz, the maximal error was found to be 2 mV, corresponding to 0.1 K which is a sufficient value for our application. Further on the conversion rate limits the minimal synchronisation interval, which on the other side is correlated to the bus speed. As an operation not close to the limits is always considered to be saver, finally a synchronisation interval of 5 sec for the ADC and 125 kBit/sec for the CAN-bus speed were chosen.

The last part of the program then supplies the shifter with the actual information. On the upper part of fig. 6 the panel for the monitoring of the cooling box can be seen. The temperatures of the sensors are given, in parallel their position in the box is displayed, this makes temperature gradients visible. The trending shows the development over time. A panel for all base detector units belonging to one PCC is shown in the lower part of fig. 6.



Figure 6: PVSS panels for the test beam setup 2002

More PCCs can be easily added here. Further information like values for the high and low voltage can be added to each BDU.

Alltogether the behaviour of the program was very satisfactory. PVSS offers useful tools to design clear panels for the shifters. Data taking and storage were reliable. The only problems observerd so far are instabilities in the 'visualization manager' and the 'trending' tools, which turned out to be quite limited. Transfering the ADC test results to the channel numbers of the final system, 2000 channels, the maximum number in one CAN-bus branch, can be read out in 5 sec with a precision of 2 mV correpsonding to 0.1 K. As no fast reaction of the standard monitoring path is expected, these values should be sufficient. The thermal interlock system did not show any malfunction; signals were set and reset as expected. A deterioration of the system due to the large cable length was not observed. For the first time the temperature of a detector module under data taking conditions was measured. No cross talk between the data acquisition system and DCS was observed. Depending on the meachnical structure an increase of the temperature — due to the power dissipation of the read-out electronics — of 8 to 10 K was measured.

6 Summary and Outlook

The integrated setup of the DCS front- and back-end passed its first test successfully. The complete chain of the thermal interlock system did not show any problems. The performance of the SCADA system, PVSS, was studied, which covers the pixel detector's needs. Besides that PVSS offers good possibilites to build a geographically oriented tree structure as it is planned for the pixel DCS. As the basic building blocks are defined, the system is easily expandable. Our next steps will include more quantities for monitoring and in parallel increase the number of detector units under control. More studies — closer to the final setup — have to follow concerning the thermal behaviour of the detector modules. Furthermore we have started to develop a separate histogramming tool based on 'root'.

References

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