A Low Mass, Low Profile Interconnect for the ATLAS Pixel Detector Modules

(OK ... so it's a flex circuit)

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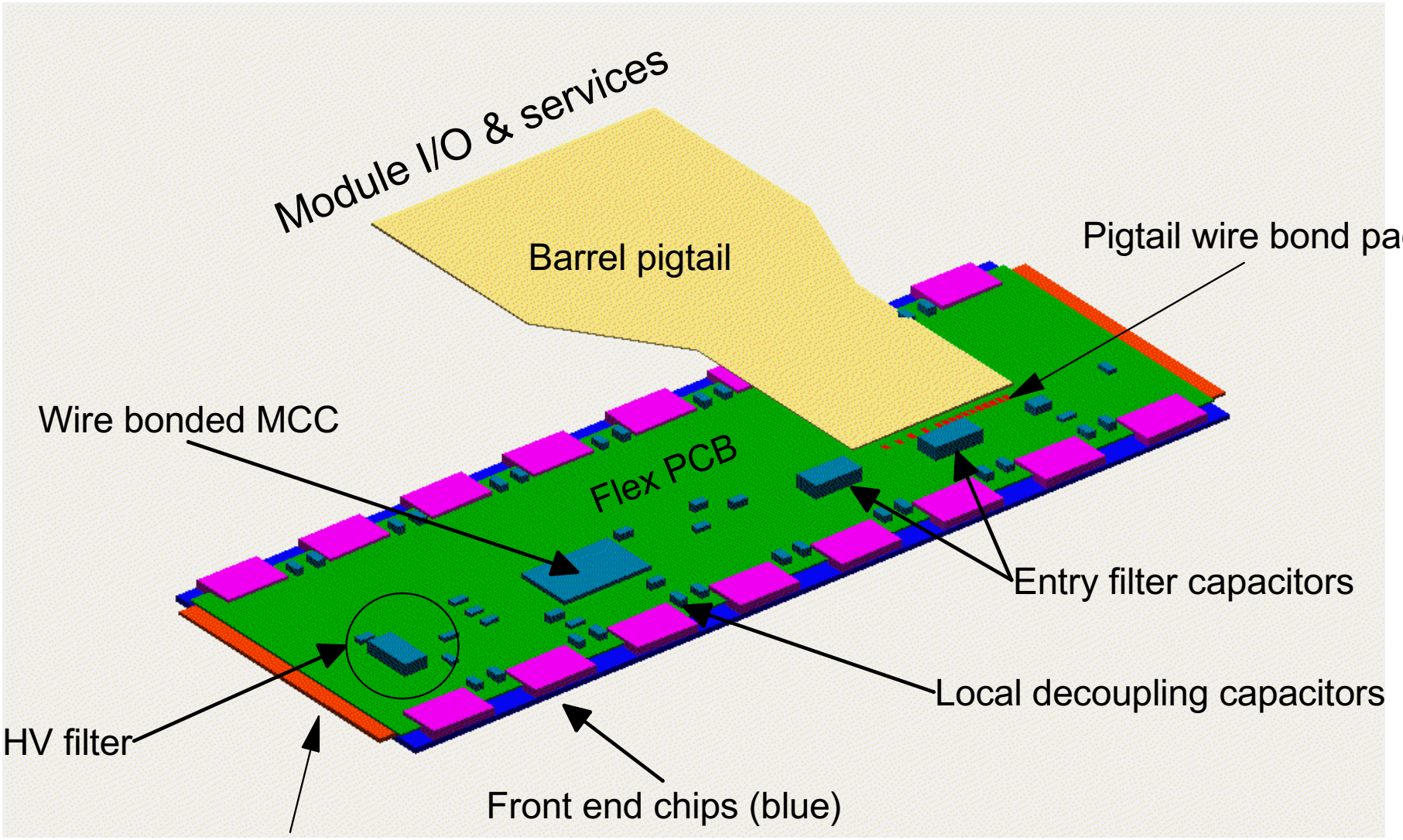
Contents

See the OU Flex Hybrid site for drawings and test results:

http://www.nhn.ou.edu/~boyd/atlas_html/base.html

(send me an e-mail and I'll send you the URL: boyd@ou.edu)

Conceptual Drawing of Atlas Pixel Module

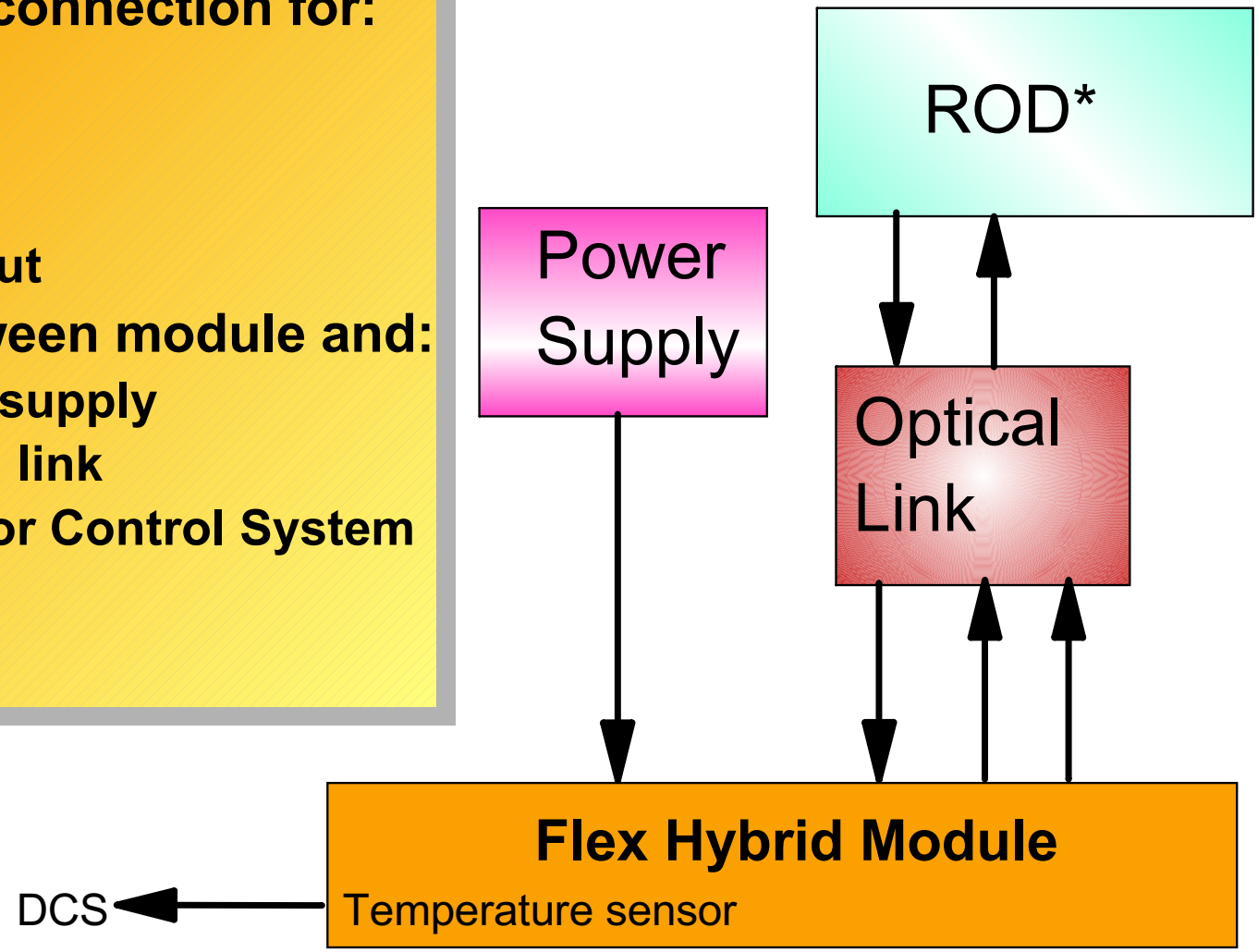


Prototypes

- Five versions of flex hybrid have been built to date, evolving to support electronics, module and mechanical requirements along the way
  - ►v1.0 produced our first flex hybrid modules
  - ►v1.x introduced a more efficient routing scheme and other improvements
  - ►v2.x supported development of services connection to the flex hybrid
  - ►v3 (supporting MCC-A & FE-I) and v4 (supporting MCC-I & FE-I) have seen continued improvements in routing, power decoupling for individual FE chips and services access.
  - ►v4 is designed to fit within the mechanical envelope
- v4 should be very near final design (still need system tests)
  - 100 v4.1 built and used in modules to date (vendor 1)
  - 122 v4.2 flex received (vendor 2) - two modules built and tested in beam
  - Several working v4 modules to date
- Comparison of noise of single chip (bare) modules and flex hybrid modules indicate that the flex hybrid is providing (adequately) clean power and signal routing in the lab and test beam

Function

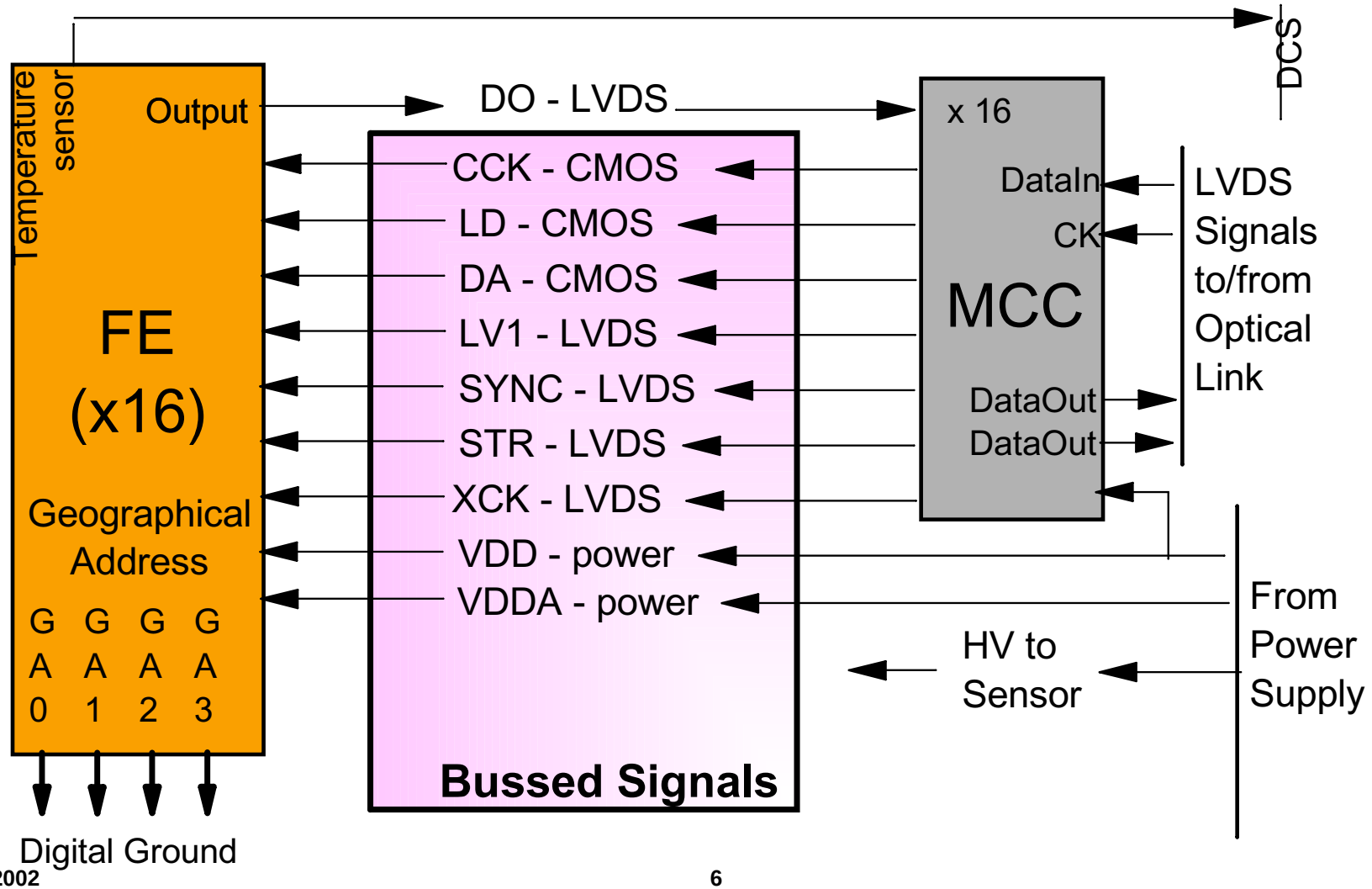
- **Provide connection for:**
  - **Power**
  - **Clock**
  - **Data In**
  - **Data Out**
- **and between module and:**
  - **Power supply**
  - **Optical link**
  - **Detector Control System (DCS)**



*Read Out Driver

Function (*continued*)

- **The Flex Hybrid provides interconnection between the 16 FE's (Front End chips) and the MCC (Module Control Chip)**

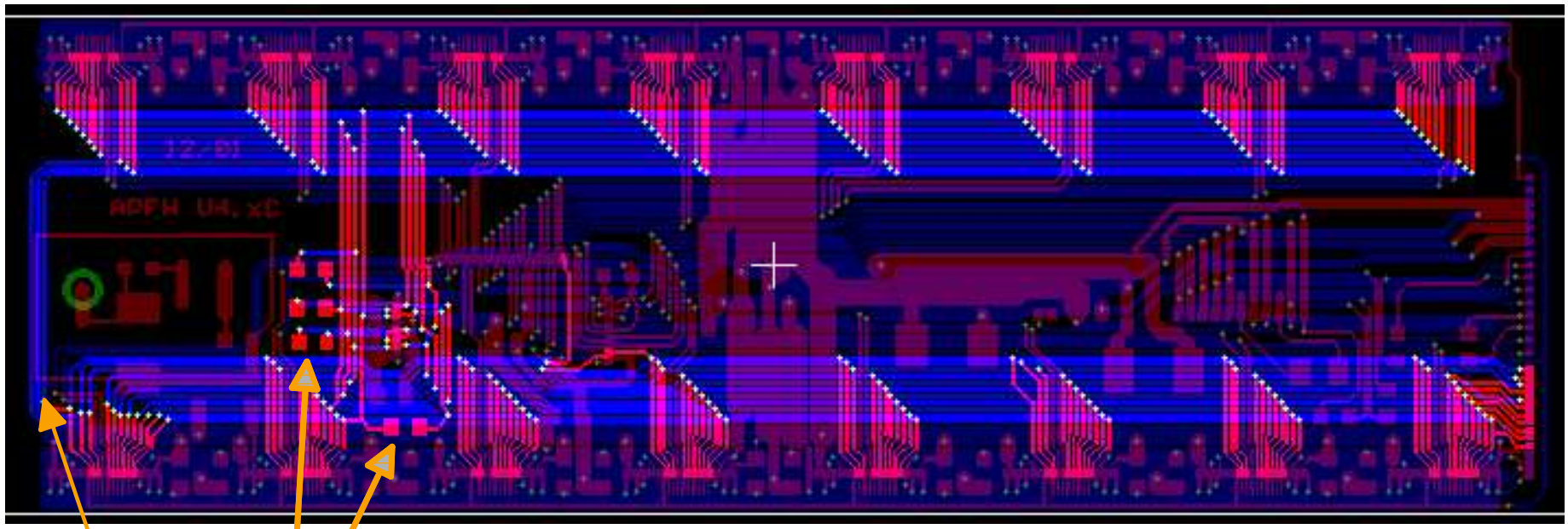


Design

- Flexible printed circuit board technology chosen for low mass (~0.0018 X_0) and low profile
- Two metal layers on polyimide substrate, connected by through-hole vias
- Metallization
  - 17 - 20 μm Cu
  - ~2 μm Ni
  - 0.1 - 0.2 μm Au
- Delivered size: 86.6 mm x 19.6 mm
- Final size on module: 63.1 mm x 19.6 mm
- Cover layers top and bottom - bottom cover layer must hold off up to 800 Vdc
  - Compunetics uses 1.5 mil Pyralux
  - Dyconex uses approx. 60 μm of an LPI soldermask, applied in two layers on the bottom (AKA "green stuff")

Design (*continue*)

- LVDS signals routed using "H" bus layout
- CMOS signals routed using "U" bus layout

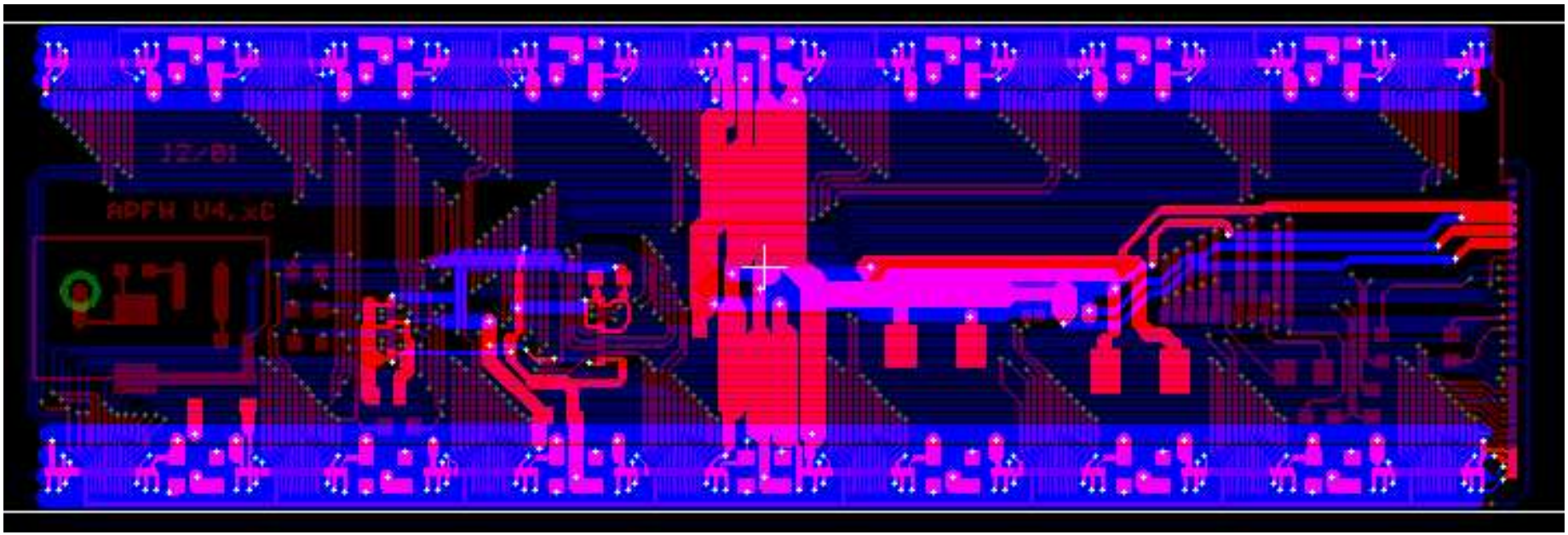


LVDS termination resistor pads

CMOS signals

Design *(continued)*

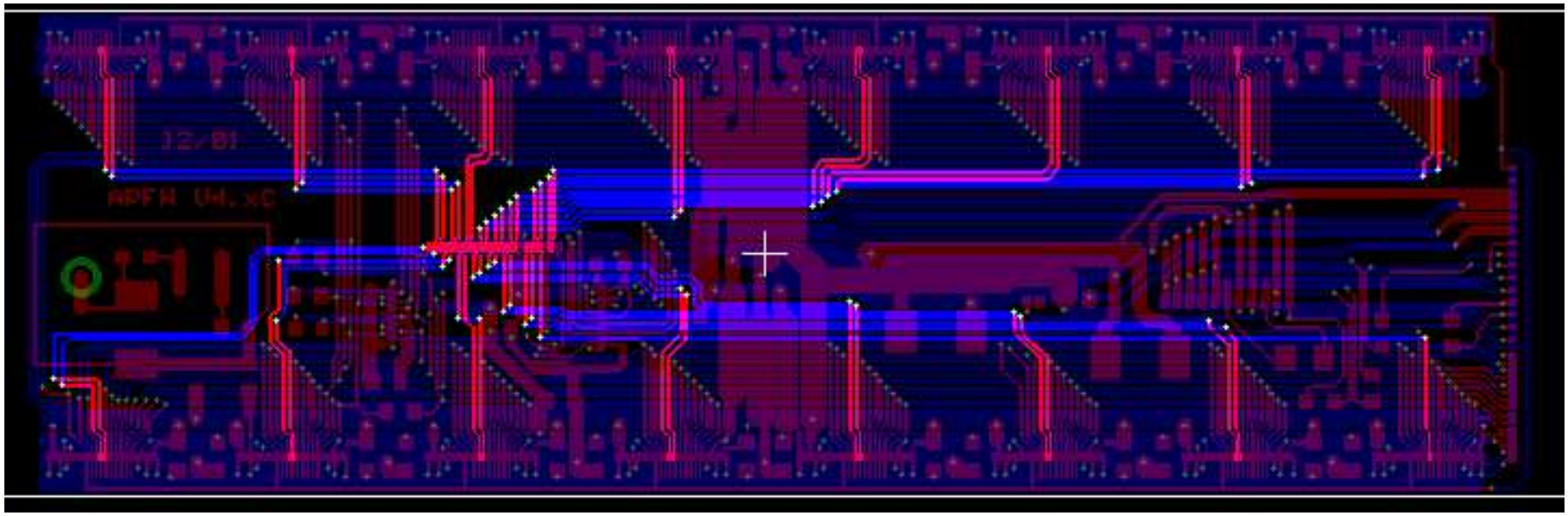
- **Power routed on both edges, as close to FE bond pads as possible, with digital power routed closest. Each supply trace is 750 microns wide.**



Screen capture has limited resolution, so individual traces are not visible

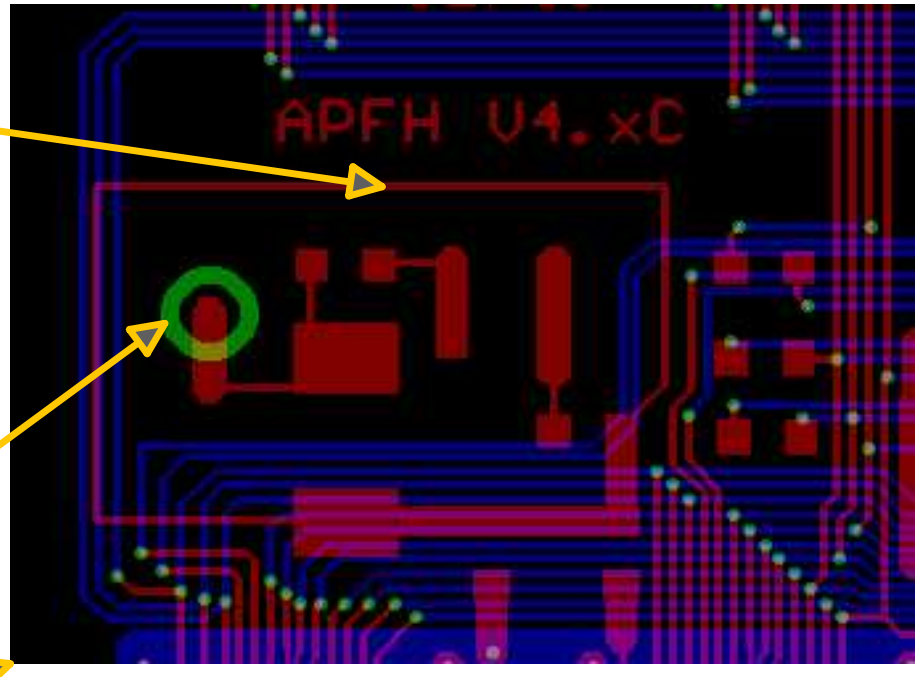
Design *(continued)*

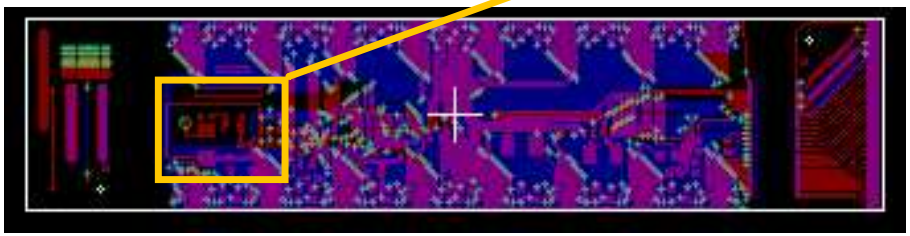
- **FE outputs utilize star topology**



Design *(continued)*

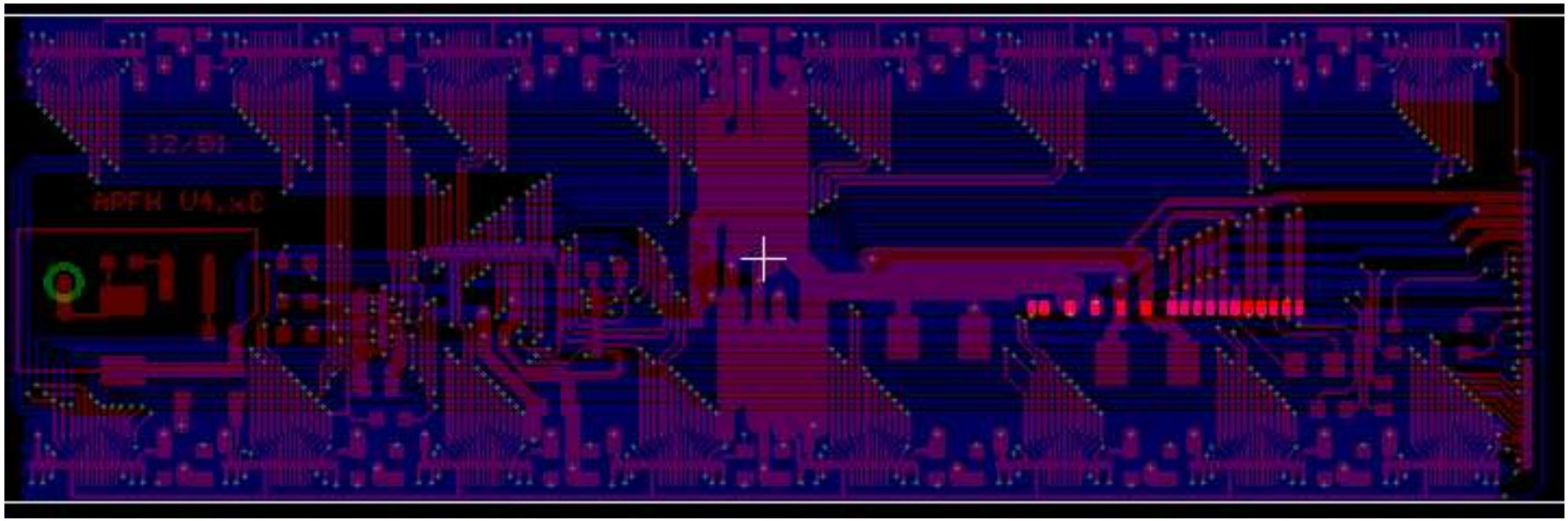
- HV area surrounded by guard ring in top metal that is at least 1 mm from HV features
- HV contact to back side of sensor made by (wire bond) through 1 mm "via"





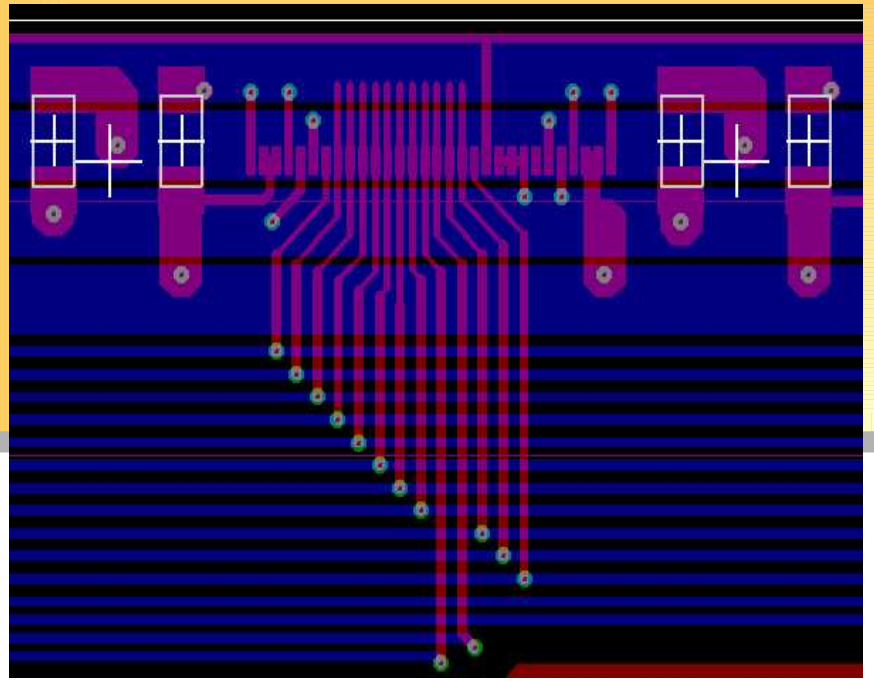
Design *(continued)*

- **Both disc and barrel pigtails connect to common pads**



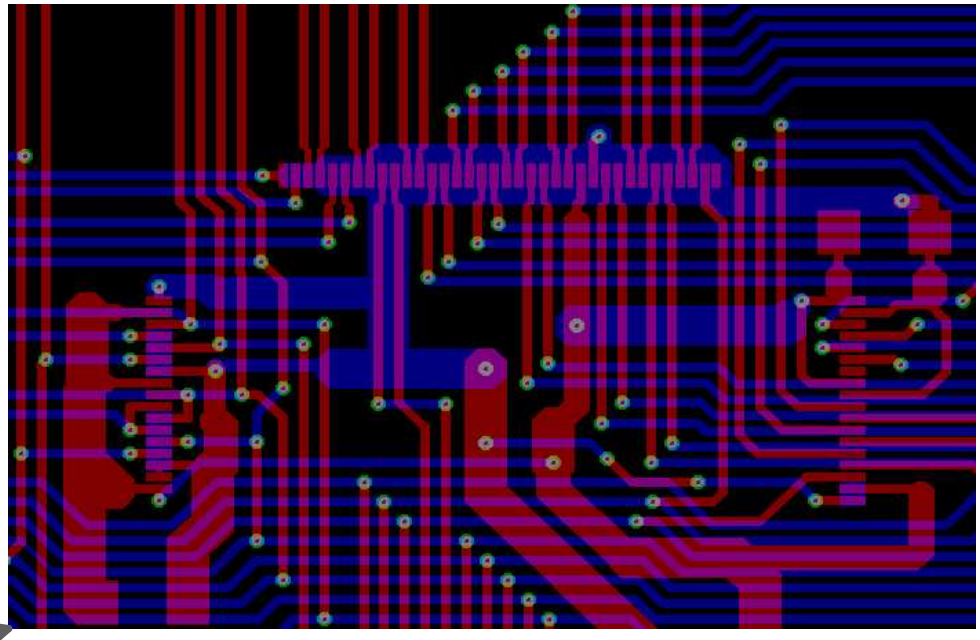
Design (*continued*)

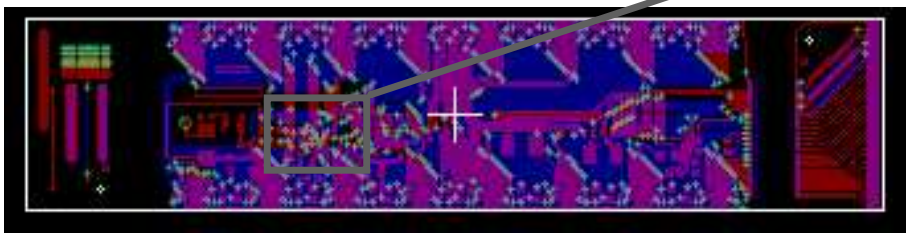
- 'Active' FE bond pads moved to center 2/3 of FE width (7.6 mm pitch)
- Layout for FE bond pads fans out:
  - Bond pads on 150 μm pitch, 100 μm wide
  - Traces leave bond pads at 75 μm traces and spaces
  - They then fan out to 100 μm traces and spaces in minimum distance
- Bond pads anchored by tails
- Traces under bond pads where possible to improve bonding



Design (*continued*)

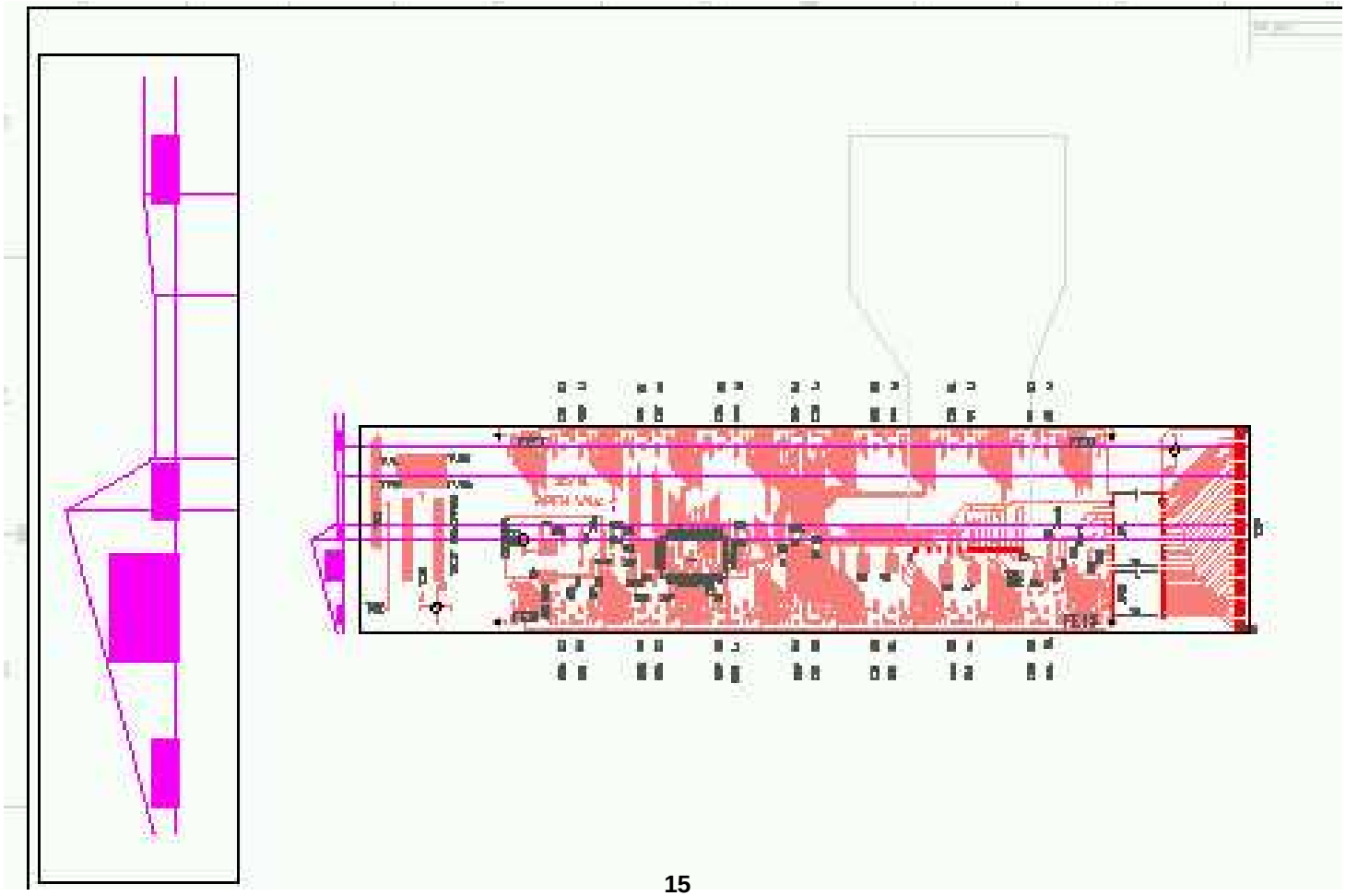
- Layout for MCC bond pads are routed from alternating sides of the top line of pads at 100 μm traces and spaces minimum rules





Design (*continued*)

- **Mechanical envelope constrains placement of most components**



Vendors

- The CERN PC shop produced some early hybrids but is not considered a production source
- Compunetics (Monroeville, PA) has been building flex for ATLAS Pixels since v1.x
  - ►Seems to be able to meet our technical requirements
  - ►Moderate pricing
- Dyconex (Zurich, CH) has built flex for other HEP experiments (e.g., D0)
  - ►Need to qualify - irradiation and module assembly tests
  - ►Low price
- Neither provide in house testing
  - ►Microcontact (Bern, CH) has done testing for all CERN and Dyconex flex using flying probes
  - ►Testing could be done by bed of nails for production?
    - Technology accessible in US and Europe
    - Lower cost and faster than flying probe testing
    - How does it treat thin Au bond pads?
- We are told production can be completed in about 4 months

Components

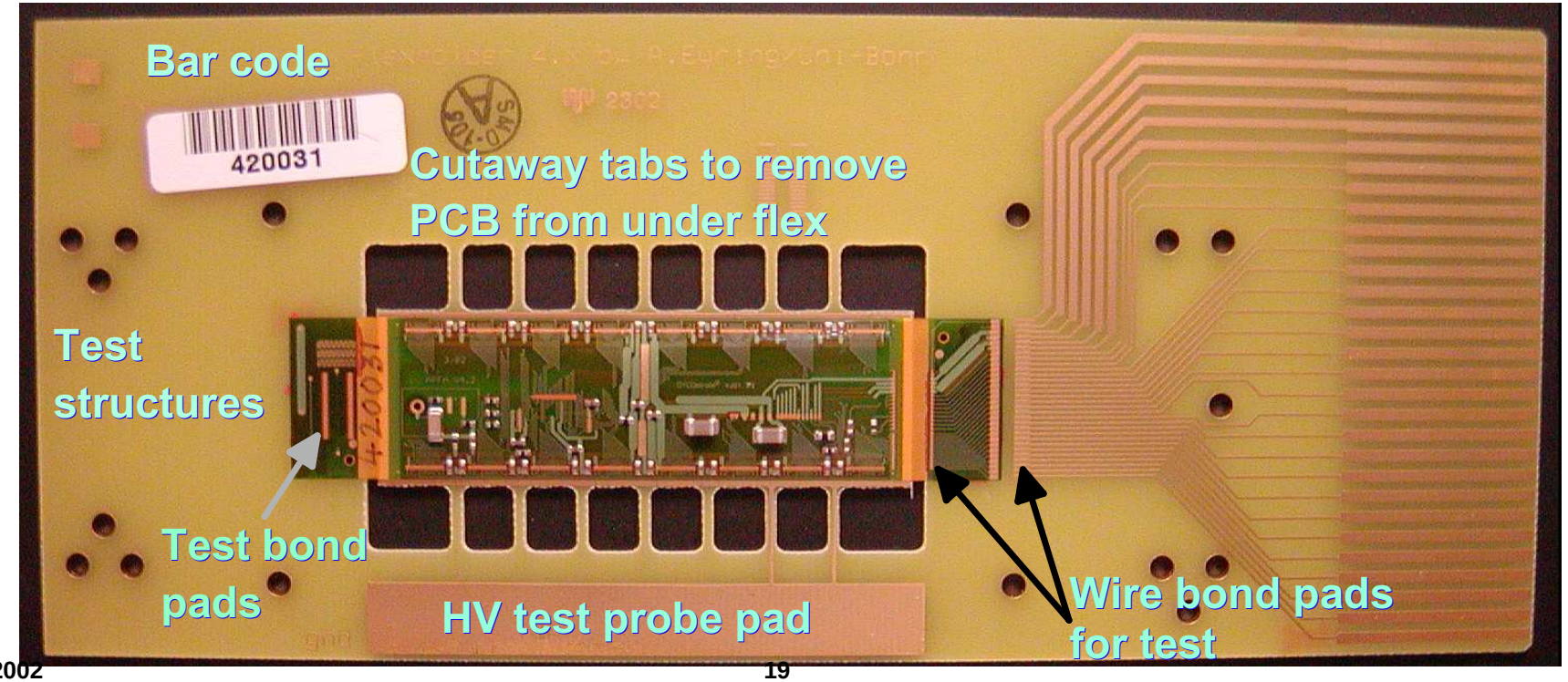
- NTC
  - Selected, irradiated, qualified by Wuppertal
  - 4000 ordered and on hand (Wuppertal)
- We have at least one reel of each of the expected final components:
  - Being used to build v4 flex hybrid modules, which will be irradiated
  - Also irradiating samples at CERN PS in August
  - Plan is to qualify each batch of components by irradiation
  - Final number of components not known at this time, but a very low cost on module scale
- Continuing irradiation program at UOK has found no problems to date
  - Most significant change we see at Pixel doses is a <20% reduction in capacitance value
  - Analyses to be completed soon (he said with much embarrassment)

Assembly and Testing

Activity	Production rate	units	Resource	Production time (days)			
Flex fabrication	200	/week	I	75	Fraction of MCC flex provided by US	0.5	
Visual inspection	6	/hour	S	61	Number of flex	2200	
Lamination of flex onto FPCB's	30	/hour	S	12	Technicians	1	FTE
Load passive components	1	week	I	5	Students	1.5	FTE
Chemically clean flex	30	/hour	S	5	EE supervision	0.5	FTE
Visual inspection:	4	/hour	S	92	Physicist supervision	3	FTE
Plasma clean flex (note 1)	6	?/hour	S	61	Length of project day	6	hr.
Wire bond test access	6	/hour	T	61	Working days/year	240	
Pot above wire bonds	6	?/hour	S	61	Student & Technician day/yr	599	
HV test	6	/hour	Albany	61	Resource definitions:		
We now have flex hybrids, which are split between UOK and Genova					I = Industry		
Attach disk pigtail only	2	?/hour	S	50	S = Student		
Wire bond test	6	/hour	S T,	31	T = Technician		
Short test	6	?/hour	S	31			
Attach MCC	4	?/hour	S T,	46			
Wire bond MCC	4	?/hour	T	46			
Active test each FE position on flex	2	?/hour	S T,	92			
			Total S & T time	648	days		
Notes:							
? indicates rate has yet to be verified at UOK							
1) Subsequent plasma cleaning steps may be required							

Assembly and Testing (*continued*)

- **Testability designed into flex hybrid**
  - ► Signals from one corner of bus routed to FPCB for test and monitoring
  - ► > 95% of HV testing done through FPCB edge connector
  - ► FPCB edge connector and probe card provide electrical test for about 90% of flex hybrid
  - ► Limited routing available - NTC not connected to FPCB

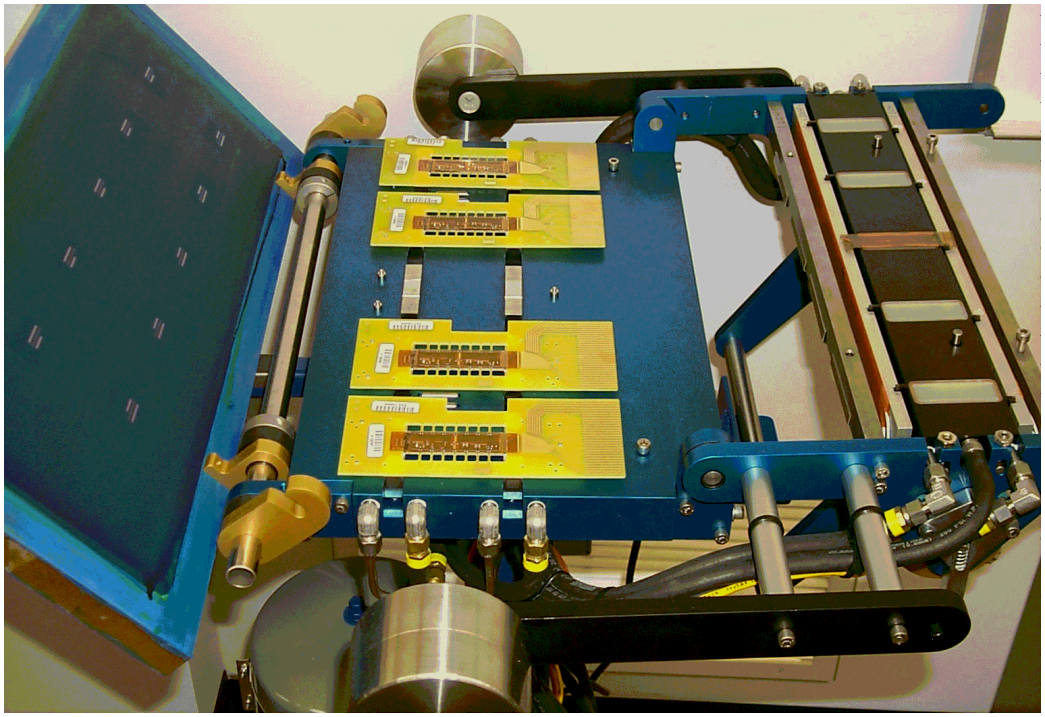


Assembly & Testing (*continued*)

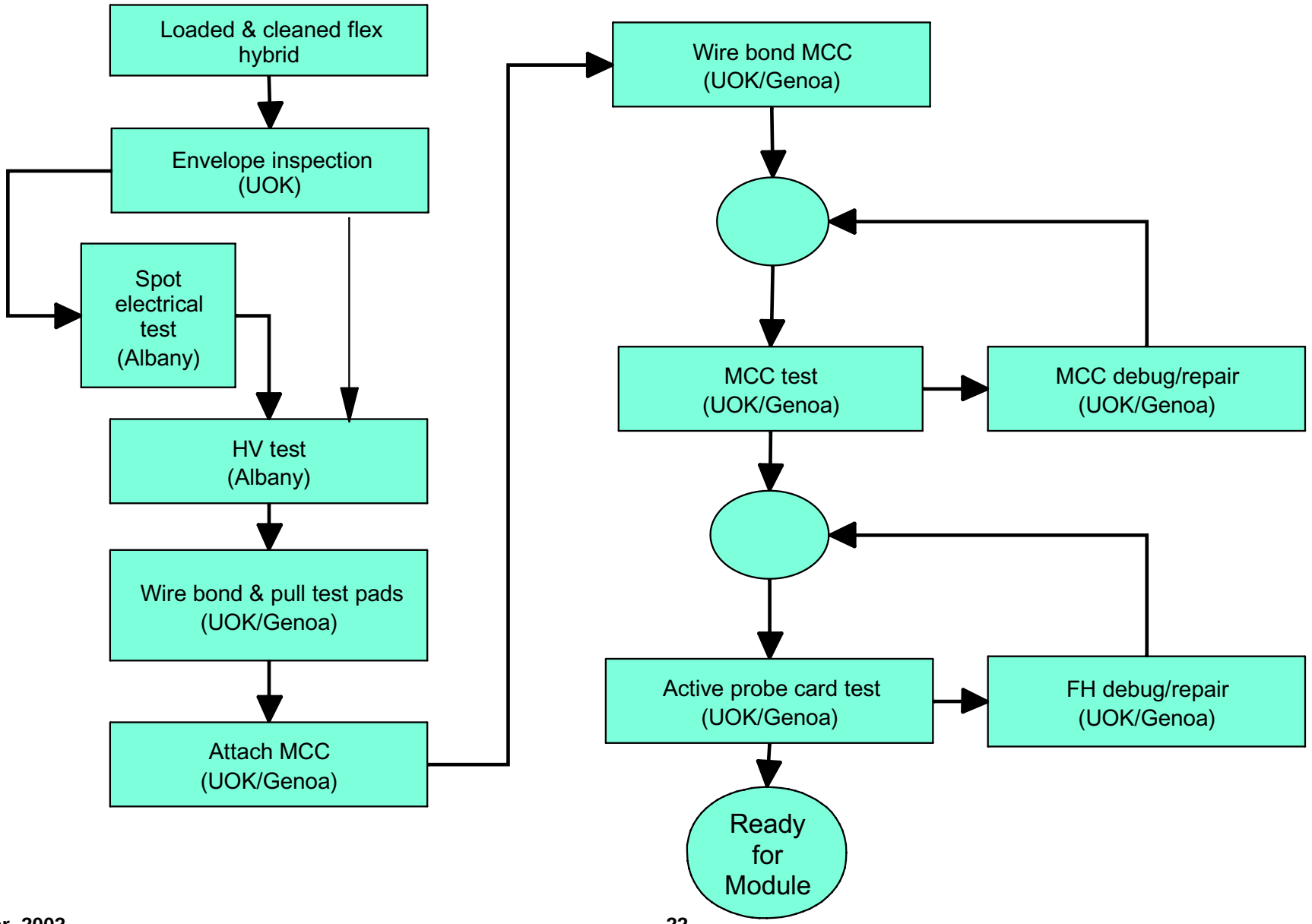
- Bare flex circuits are mounted to Frame PCB with Loctite 3614 Chip Bond adhesive, using a laminator, custom designed and built by the OU Physics Dept. machine shop
- Laminator has a high throughput: could laminate 3000 flex in 1 month
- Next, they are sent out for component loading.

Assembly & Testing (*continued*)

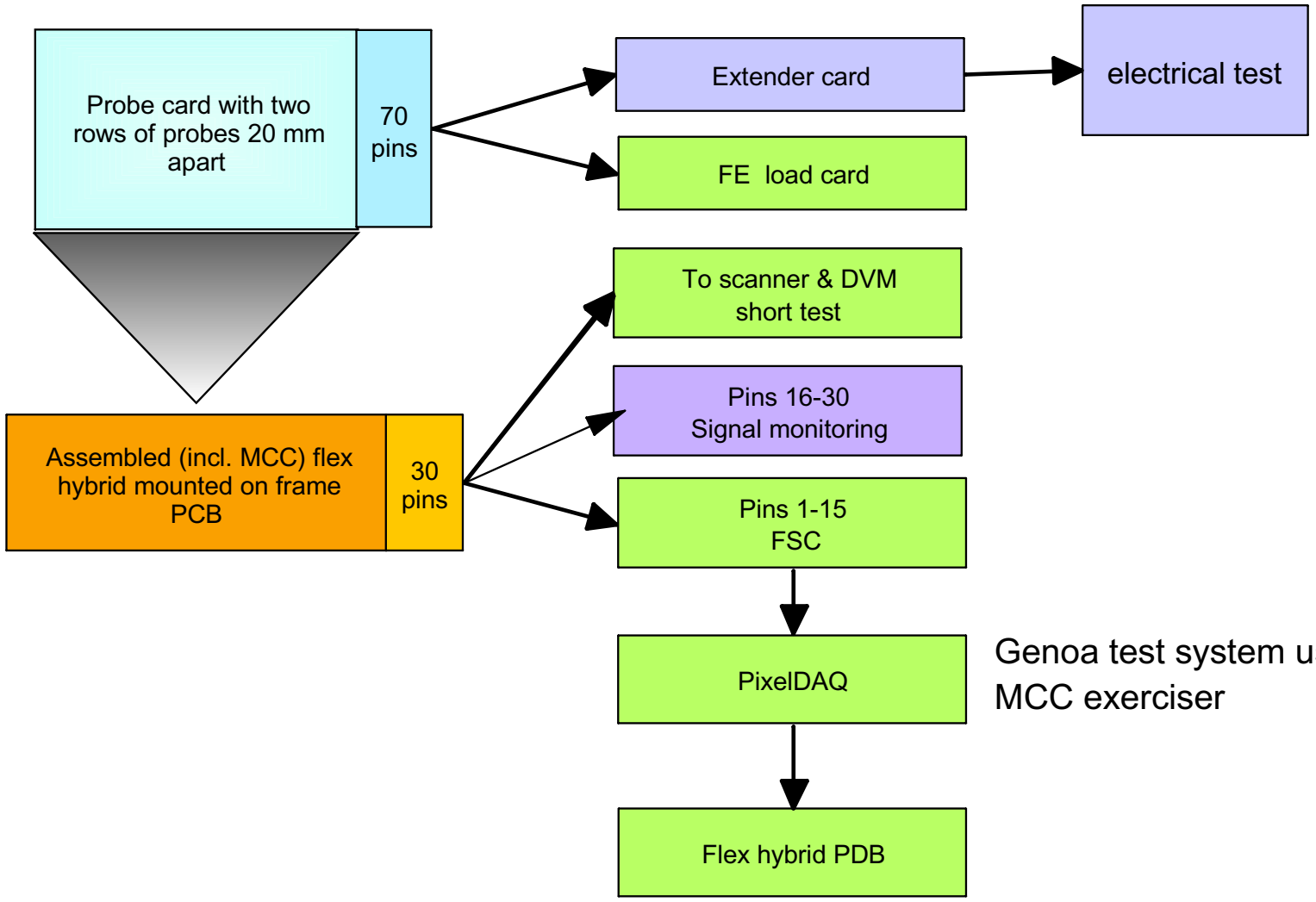
- Surface Mount Depot (OK) has been assembling flex since v2.x
  - ►Seem to have a good understanding of our requirements
  - ►Like most assembly vendors, they are able to build our production order in a matter of days, making a "home town" vendor very attractive



Flex Hybrid Test Flow Chart v1.6

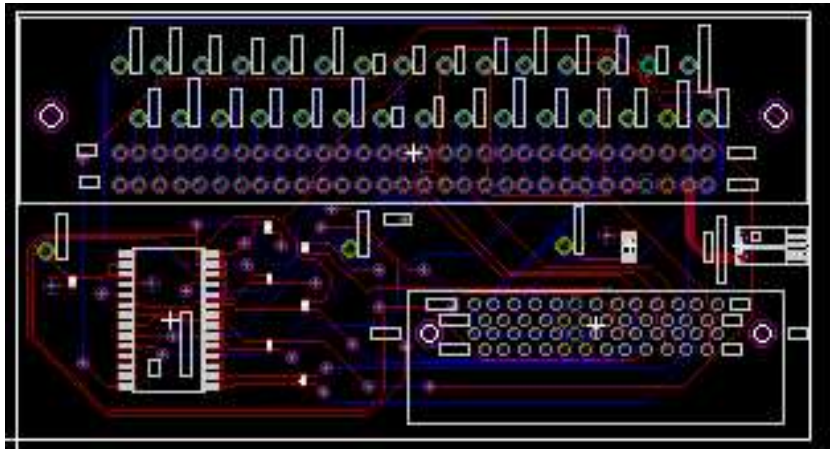


Flex Hybrid Test Block Diagram v1.4

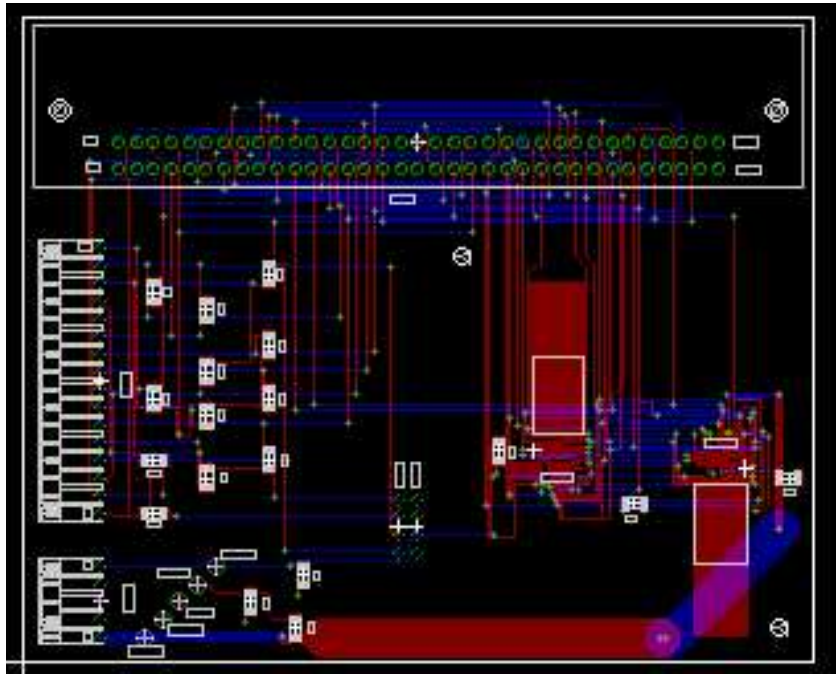


Genoa test system uses MCC exerciser

Assembly & Testing (*continued*)



FSC (Frame Support Card)



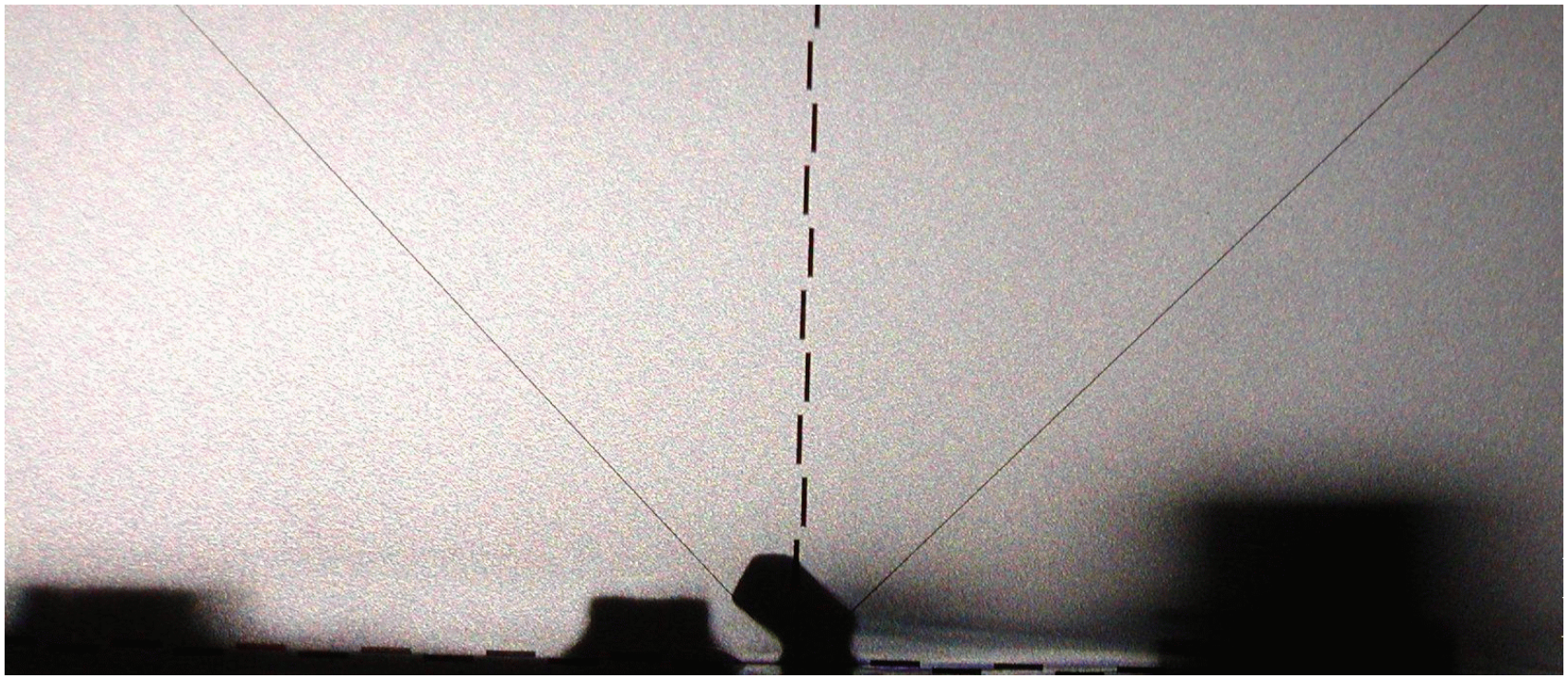
- FE load card

What's Ahead

- Most changes for final design are very minor, but the most important are:
  - Changing SMD pads to vendor recommended sizes for automated assembly (current design was optimized for hand assembly using conductive epoxy)
  - Adding parallel vias in the power traces for increased reliability
  - The reset line (RSIB) has been dropped
  - We may need to AC couple the sensor bias grid, which is currently connected to AGnd
- Only one error has been brought to light (so far) - a zero width trace in GA of FE 12, which we can work around by adapting the wire bonding

What's Ahead (*continued*)

- We recently have had a problem with "tombstoning" of components during reflow soldering



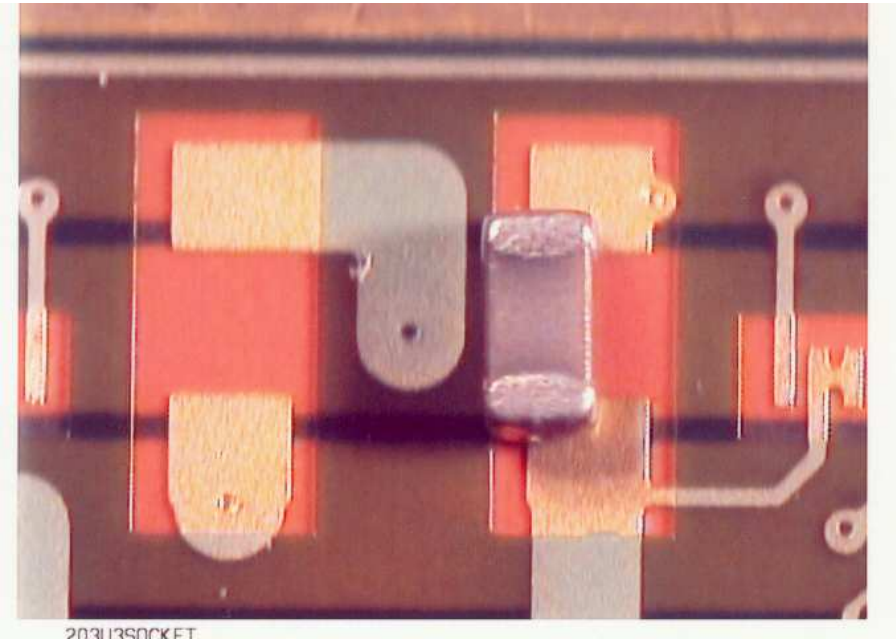
What's Ahead (*continued*)

- **Part of the problem is warping of the Dyconex flex circuits, believed to be caused by the bottom solder mask being twice as thick as the top**

Warped Dyconex flex. These were processed for an extended time (12 min.) in an oxygen plasma cleaner.

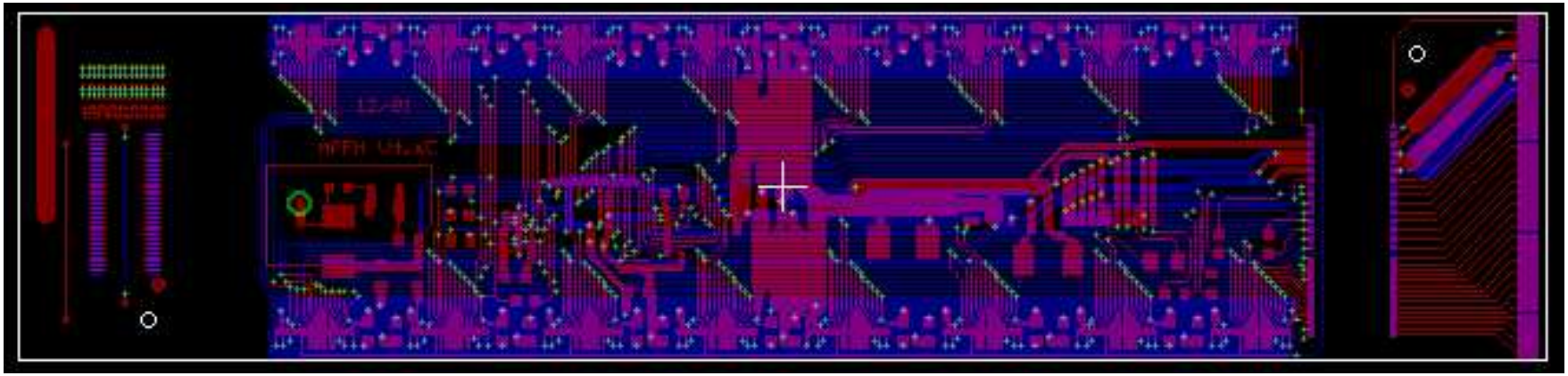
What's Ahead (*continued*)

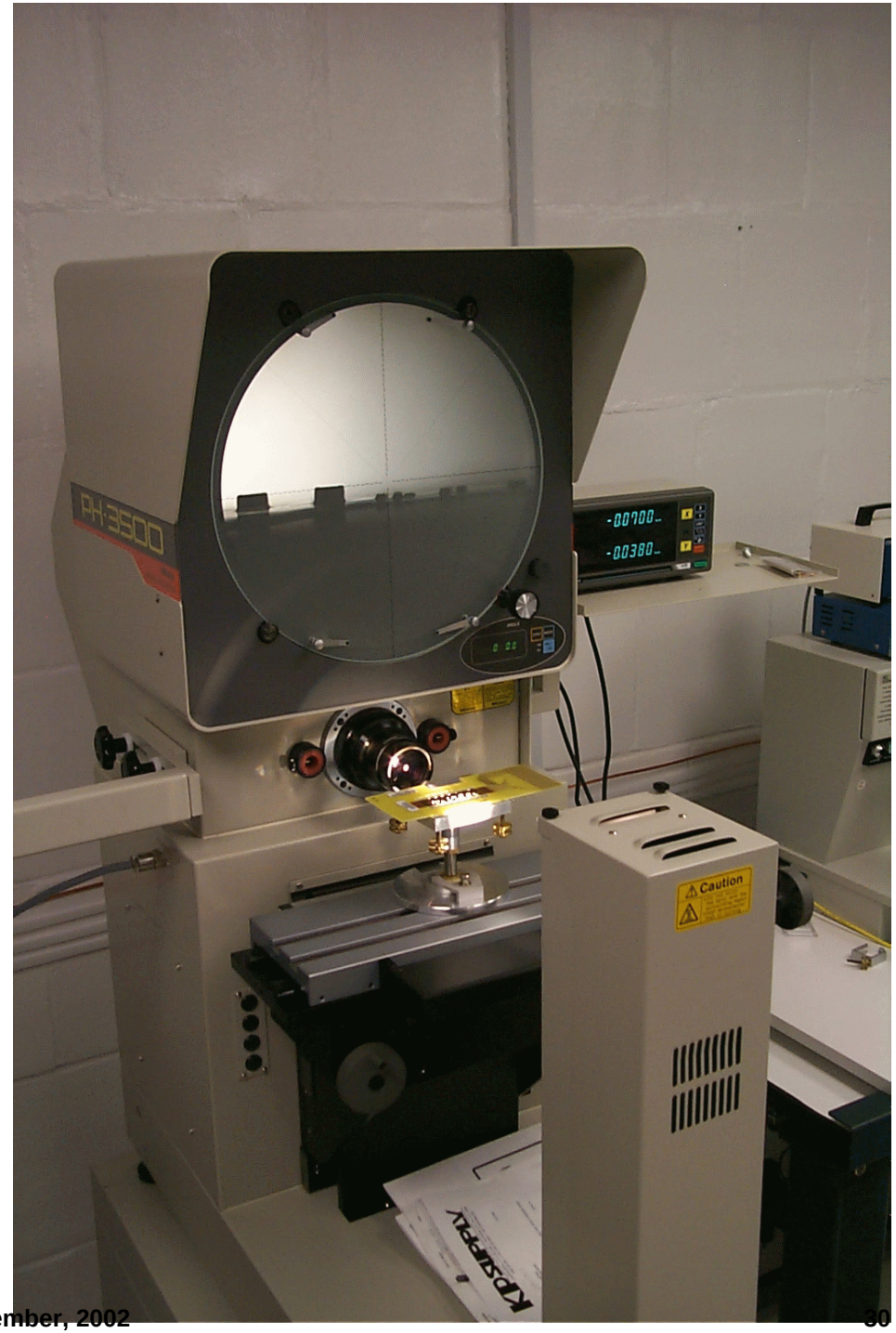
- **Probably more important is the size of the 0402 SMD pads: these were originally designed to optimize the use of conductive adhesive (dropped because of high resistance). They will be changed to manufacturer specified size in the next version.**



Summary

- Two vendors have been identified that seem capable of producing the flex circuits (pending final qualification of the Dyconex solder mask)
- Loading of SMD devices flex circuits can be done in industry, also
- The test system is under development - HV and electrical testing seem to work
- Preparing for Production Readiness Review at CERN 30 September
- Submission of production design (early 2003)

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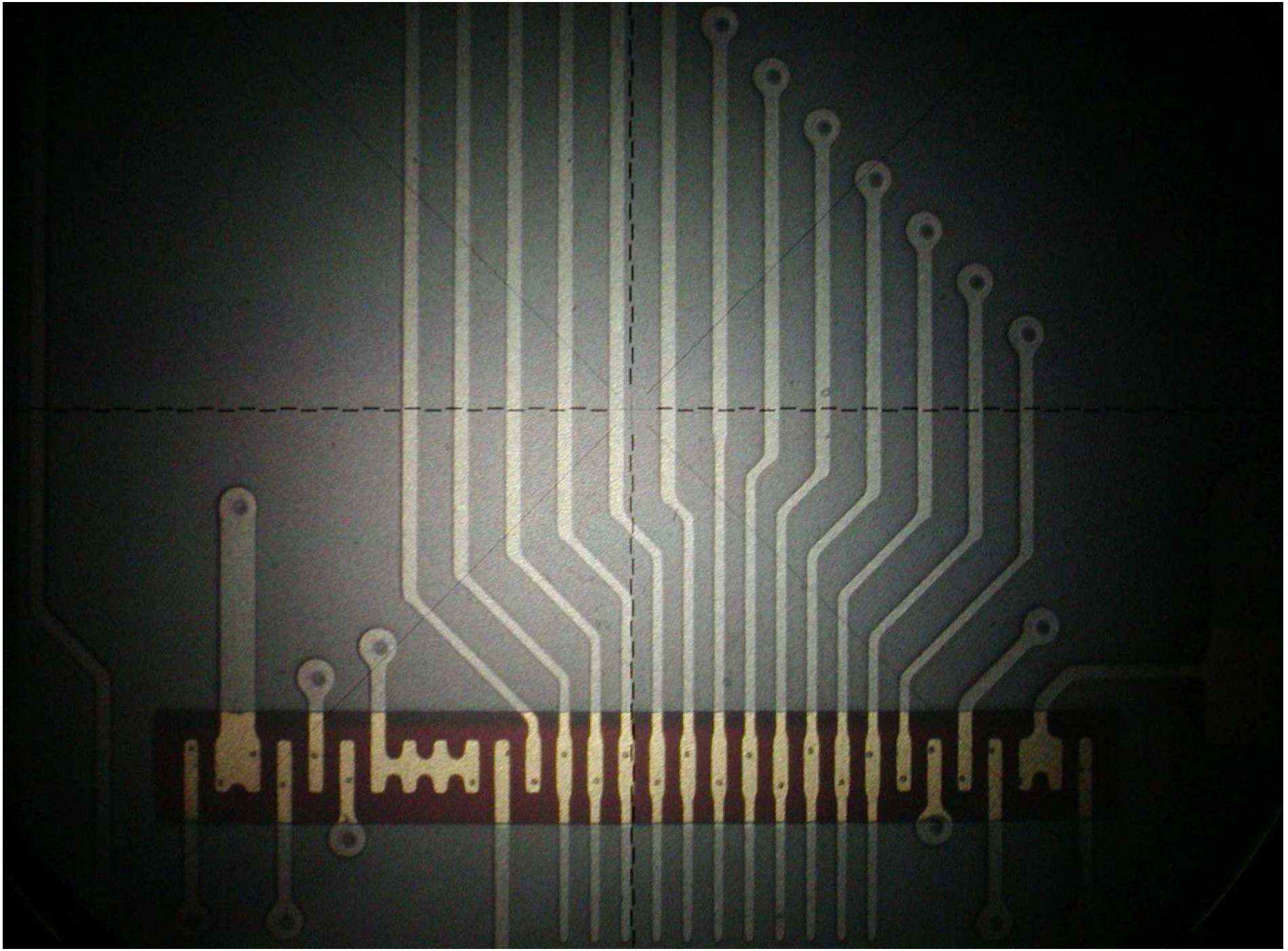


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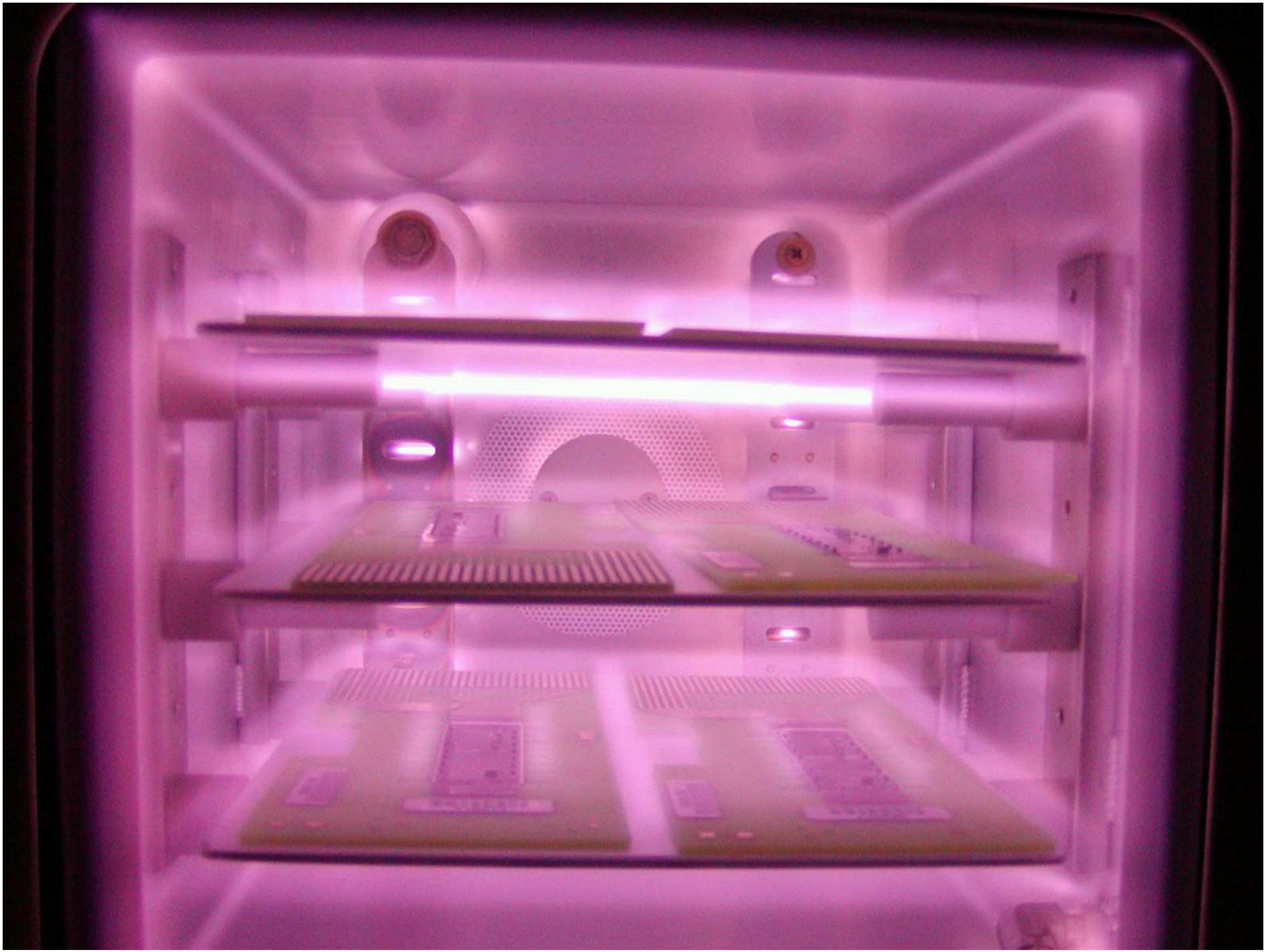


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