The ALICE Silicon Pixel Detector

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1 Abstract

The ALICE Silicon Pixel Detector (SPD) will form the two innermost layers of the ALICE Inner Tracking System (ITS) at radii of 3.9 cm and 7.6 cm, respectively. The SPD consists of 1200 pixel readout ASICs developed in a commercial 0.25μm CMOS process. Each chip contains 8192 readout cells, leading to an overall 9.8 million readout channels in the whole SPD. The sensors are matrices of p^+n-diodes produced on 200 μm thick silicon. An overview of the ALICE SPD is given in this paper. The performance of the ALICE pixel chip as well as results from wafer probing are presented. First results from radioactive source measurements on full size bump-bonded ladders and results from beam tests are shown. Preliminary results indicate the full functionality of the pixel chip and the ladders within the ALICE requirements.

2 Introduction

The ALICE experiment [1] is designed to investigate the properties of strongly interacting matter under the extreme conditions of nucleus-nucleus interactions at the LHC. The study of the production of beauty and charm hadrons is of particular interest in order to probe the formation of deconfined matter. Charm and beauty detection requires an excellent secondary vertexing capability coping with the high

multiplicity environment of nucleus-nucleus collisions. Charged multiplicities of up to 8000 tracks per unit of rapidity in Pb-Pb collisions have been predicted.

The ALICE SPD provides high granularity tracking information close to the interaction region and will thus play an important role in the overall physics performance in ALICE. In the following a description of the SPD layout and construction, the performance of the readout chip and results from bump bonded ladders in the test beam and from source tests are presented.

3 SPD Layout

The SPD consists of two barrel layers at radii of 3.9cm and 7.6cm, respectively. The pseudorapidity coverage of the inner layer is $|\eta| \leq 1.95$. The two layers will be built out of 120 half-staves. Figure 2 shows a schematic drawing of a half-stave. Each half-stave contains two ladders consisting each of a silicon pixel sensor (70.7×16.8 mm^2) bump bonded to 5 pixel chips. Figure 1 shows a CAD drawing of one end of a carbon fiber sector and the staves mounted on it. The staves on the outer layer are mounted in a turbine configuration while those on the inner layer are staggered.

The p^+n sensors are produced on 200 μm silicon wafers with a simple guard ring structure. The estimated fluence integrated over 10 years is in the order of a few 10^{12} neutrons/cm^2 in the innermost layer [1]. The radiation damage at this level is expected to be very low, therefore a standard p^+n design was chosen for the pixel sensors [3].

In order to reduce the multiple scattering of particles with low transverse momenta, which decreases the tracking precision, the overall material budget should be kept to a minimum. The staves are mounted on light-weight carbon fiber sectors, each sector supporting two full staves on the inner layer and 4 full staves on the outer layer. An aluminum-polyimide multilayer bus, glued on top of the ladders, provides the signal and power connections for the readout chips. The thickness of the bus is 240 μm. The readout chip wafers will be thinned down to 150 μm thickness after bump deposition. The cooling tubes are embedded in the sector profile. The overall material budget per layer is estimated to $\approx$1%.

The interconnections from the chips to the bus are made using ultrasonic wire bonding with wires of 25 μm diameter. The picture in figure 3 shows the corner of an ALICE ladder mounted on a prototype bus. In this version the bus was mounted underneath the chips to facilitate testing. In the final version the bus will be mounted as indicated in figure 2.

The readout chip signals are carried by the bus to the multi-chip-module (MCM) at the end of the half-stave. The MCM houses the analog PILOT, the digital PILOT, the gigabit optical link driver (GOL) and the optical module containing two PIN photodiodes and a laser diode. The analog PILOT provides the reference biases for

the pixel chips and an ADC to monitor currents and voltages. All the signals to/from the counting room are transmitted on optical fibres. The digital PILOT handles the incoming clock, trigger and configuration data and provides timing, control and readout for each half-stave. The readout data are serialized by the GOL in a G-link compatible format and sent out at 800 Mb/s. A detailed description of the on detector PILOT system (OPS) can be found in [2].

The numbers of components used in the ALICE SPD are summarized in table 1.

A modular test-system has been developed within the ALICE SPD team in order to perform tests on wafers, single chips, multi-chip modules, staves and in a test beam. The test system is based on VME and LabView [4]. A detailed description of the test system can be found in [5].

4 The ALICE1LHCB Chip

The SPD readout ASIC is named ALICE1LHCB as it has been designed with dual-mode features that allow its use also in the HPD for the LHCb RICH. It is a mixed signal chip in a 0.25μm commercial CMOS process. The radiation tolerant design includes enclosed layout transistors and guard rings [6].

The ALICE1LHCB Pixel chip contains 8192 pixel cells, each with a size of 50 $\times$ 425 μm^2. The cells are arranged in a matrix with 32 columns and 256 rows. The active area of the chip is 12.8 $\times$ 13.6 mm^2, the full size of the chip is 13.5 $\times$ 15.8 mm^2. The chip is clocked at 10MHz for the ALICE experiment and contains about 13 million transistors.

Each pixel cell consists of an analog part with differential preamplifier, two shaper stages and a discriminator and a digital part. A test-pulse can be applied via a test-capacitor to the input of each pixel cell. The digital part consists of a synchronizer followed by two delay units of which each can delay a hit up to 512 clock cycles. If a strobe signal from an outside trigger arrives in coincidence with the output of a delay unit, a logic one is stored in a 4-event FIFO buffer. On readout of the chip the pending events in the pixel FIFOs are loaded into a 256-bit shift register in every column and transfered serially as 32 parallel data streams. Each pixel cells contains also one bit to mask the cell, one bit to set the test-pulse and three bits to fine adjust the threshold. A detailed description of the design of the ALICE1LHCB pixel chip can be found in [7, 8].

Measurements using the test-pulse have indicated a minimum threshold of about 1000 electrons with an rms of about 200 electrons [9]. The mean noise measured is about 110 electrons. These measurements were carried out without individual threshold adjust. The preliminary conversion factor of 66 electrons/mV was obtained from ^{55}Fe-source measurements.

A wafer probing test system was developed in order to select chips which will be

used for bump bonding. The system is based on the modular test system developed within the ALICE SPD team and described in [5]. All tests are carried out on a PA200 wafer prober from Karl Suss. Probe cards to contact the chips via tungsten needles were designed at CERN and produced at CERPROBE [10]. A complete test procedure was developed including current consumption measurements, test of all DACs, a JTAG test, measurement of the minimum threshold and a threshold scan. According to the results of these tests, chips are classified in three classes. Chips used for bump bonding (class I) have to have a mean measured threshold of all pixels of less than 30 mV (≈2000 electrons), less than 1% of defect pixels and less than 620 mA of total current consumption. Each wafer contains 86 ALICE1LHCB pixel chips.

Figure 4 shows the mean measured threshold of all class I chips on one wafer. The distribution peaks at 18.1 mV with an rms of 1.4 mV. No chip had to be excluded from the class I group due to a mean threshold exceeding 30 mV.

In order to test the functionality of the bus, one prototype bus with metal layers made of copper was equipped with 10 ALICE1LHCB pixel chips. The chips were mounted in the same configuration as for a half stave. Systematic tests were carried out to investigate the voltage sensitivity and the sensitivity of the chips to the clock signal as well as the mean measured threshold of the chips at minimum threshold. The average value of the mean threshold measured on the 10 chips is 21.4 mV with an rms of 2.4 mV. No systematic variation in threshold or noise between chip 0 and chip 9 was observed. The values of the mean threshold and noise are in agreement with the values observed during wafer probing tests.

5 Assembly and Ladder Test Results

Flip-chip bonded single chip assemblies and ladders are produced using two different bump bonding techniques: Indium with Alenia Marconi Systems (Roma, Italy) (AMS [11]) and Pb-Sn with VTT (Helsinki) (VTT [12]).

First results on bump bonded single chip assemblies are described in [9] indicating good bump bonding yield from radioactive source measurements and low minimum threshold. Measurements were carried out using ^{55}Fe and ^{90}Sr-sources with the assemblies mounted on test cards.

The test system on the wafer prober was used to test bump bonded assemblies and ladders without mounting them permanently on a test card. Additionally a trigger system using the Fast-Or information from the chip was installed.

Several ladders and assemblies have been produced at VTT during the last year indicating a good bump bonding yield. On the most recently delivered ladders the level of faulty bump bonds was ≈0.1-0.7%. Several ladders were produced using 200 μm thin sensors and chip wafers that were back grinded to 300 μm thickness. Currently work is in progress to thin the chip wafers to 150 μm thickness, the projected

thickness for the ALICE SPD. Figure 5 shows the results of a ^{90}Sr-source measurement on a ladder with 300 μm thin chips and a 200 μm thin sensor. The response of the pixel matrix of each chip to the source is shown, with the z-scale set to 1. Faulty bump bonds are shown in white. During the measurement the detector was biased at 20 V (depletion voltage: 12 V). The bump bonding yield of the ladder is: 99.3% (chip1), 99.9% (chip2), 99.5% (chip3), 99.7% (chip4) ,99.3% (chip5). The full ladder contains 40960 bump bonds. Similar measurements were carried out on ladders delivered from AMS.

6 Results from the Test Beam in 2002

A test beam was carried out in July 2002 in the H4 beam line at CERN using 350 GeV/c protons. The setup consisted of 3 stages of ALICE pixel detectors aligned along the beam axis. The first and the last stage were used as reference planes for tracking. Each reference plane consisted of two single chip assemblies mounted one behind the other. The distance between these two single assemblies along the beam axis is $\approx$2 cm. Both singles were read out together via one DAQ chain similar to the readout scheme of a bus. Therefore a reference plane is referred to as mini-bus. The two reference planes, each equipped with one mini-bus, provided 4 space points for tracking. The reference planes consisted of 32768 bump bonded pixel cells. The central plane was mounted on a x-y table which allowed also to rotate the plane with respect to the beam axis.

The trigger was provided by the coincidence signal from 4 scintillators. Two small scintillators (2×20 mm^2, 2 mm thick) were mounted orthogonally directly in front of the first reference plane, selecting a beam spot of about 2×2 mm^2. One large scintillator (5×5 cm^2, 5 mm thick) was mounted $\approx$10 m upstream of the setup. A 1×1 cm^2 scintillator (5 mm thick) was placed directly behind the second reference plane.

During the 2 weeks of test beam 2 single assemblies were tested in the center position of the setup. One assembly consisted of a 200 μm thick detector bump bonded to a 750 μm thick chip (VTT49) and the other single assembly consisted of a 300 μm detector on a 750 μm thick chip(AMS76). For both assemblies timing scans, threshold scans, bias scans and measurements at different angles were carried out. The measured online efficiencies were 99.6% (VTT49) and 98.8% (AMS76). The online efficiency was determined using the information from the scintillator trigger. The precision of this measurement is in the order of 1-2%.

One ALICE ladder (VTT2-2001) mounted on a prototype bus was also tested in the center position of the setup. Figure 6 shows a reconstructed track in the ladder using the tracking information from the pixel reference planes. The online efficiency of the ladder was determined to be better than 99%. The same set of measurements

as carried out for the single assemblies was repeated for each chip on the ladder. Additional threshold scans were taken by positioning the beam spot between two chips. In the region between two chips the pixel cells are elongated (625 μm instead of 425 μm) to fully cover the gap between chips. No difference in online efficiency was observed for the inter-chip regions compared to the center of one chip. Figure 7 shows the online efficiency measured as function of the bias voltage measured at three different thresholds on chip 3 of the ladder. Vth indicates the internal DAC setting for the global threshold setting of the chip. Vth=220 corresponds to about 1000 electrons threshold and vth=185 corresponds to about 4200 electrons. The depletion voltage is 21 V. A wide plateau in efficiency above 99% is observed for all three threshold settings above depletion voltage. The individual pixel thresholds were not adjusted for these measurements.

7 Summary

Detailed tests on the ALICE1LHCB pixel chip were carried out indicating a low mean threshold of about 1000 electrons with an rms of about 200 electrons. First tests of 10 chips mounted on a prototype bus indicate full functionality. A wafer probing test setup was developed to select chips for bump bonding. The first results of source tests on bump bonded ALICE ladders indicate good bump bonding yield. A test beam was carried out using a 350 GeV/c proton beam. A pixel telescope made by 4 single chip ALICE assemblies was used for tracking information. Single assemblies and one ALICE ladder mounted on a prototype bus show wide plateaus of about 99% online efficiency in threshold and bias voltage scans in the test beam.

References

[1] ITS Technical Design Report, CERN-LHCC **99-12**, (1999).

[2] A. Kluge et al., The Read-Out System of the ALICE Pixel Detector, these proceedings.

[3] G. Lindstroem et al., Nuclear Instruments an Methods in Physics Research A, vol. 465, no. 1, p. 60-69, (2001).

[4] see http://www.ni.com/

[5] F. Antinori et al., The ALICE Pixel Detector Readout Chip Test System, Proceedings of the 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, September 2001, CERN-LHCC-2001-034.

[6] Ken Wyllie, Front-End Pixel Chips for Tracking in ALICE and Particle Identification at LHCb, these proceedings.

[7] R. Dinapoli et al., An Analog Front-ent in Standard 0.25 μm CMOS for Silicon Pixel Detectors in ALICE and LHCb, Proceedings of the 6th Workshop on Electronics for LHC Experiments, Cracow, Poland, 11-15 Sept. 2000, CERN-LHCC-2000-041 pp.110.

[8] K. Wyllie, A Pixel Readout Chip for Tracking at ALICE and Particle Identification at LHCb, Proceedings of the 5th Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, 20-24 Sept. 1999, CERN-LHCC-1999-033.

[9] P. Riedler et al., First Results from the ALICE Silicon Pixel Detector Prototype, Proceedings of the VERTEX 2001, Brunnen, Switzerland, accepted for publication in Nuclear Instruments and Methods in Physics Research A, 2002.

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Components	
Staves	60
Silicon Sensors	240
Readout Chips	1200
Bump Bonds	$\approx$ 9.8 million
Wire Bonds	$\approx$ 150.000

Table 1: Components of the ALICE SPD.

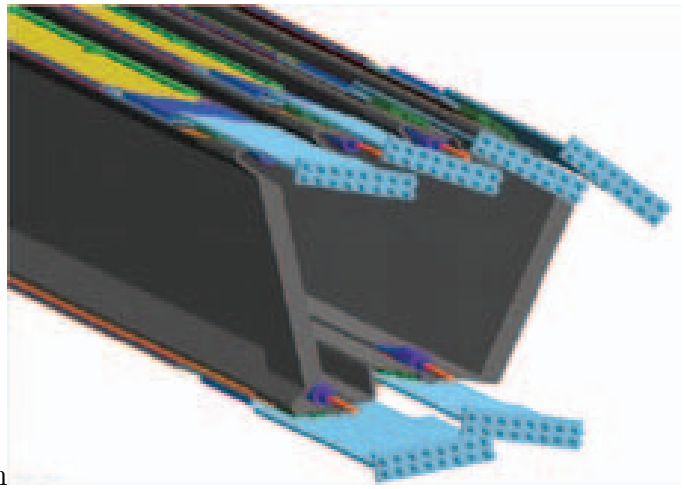
chch 

Figure 1: CAD drawing of a carbon fiber support. 4 staves are mounted on the outer layer and 2 on the inner layer.

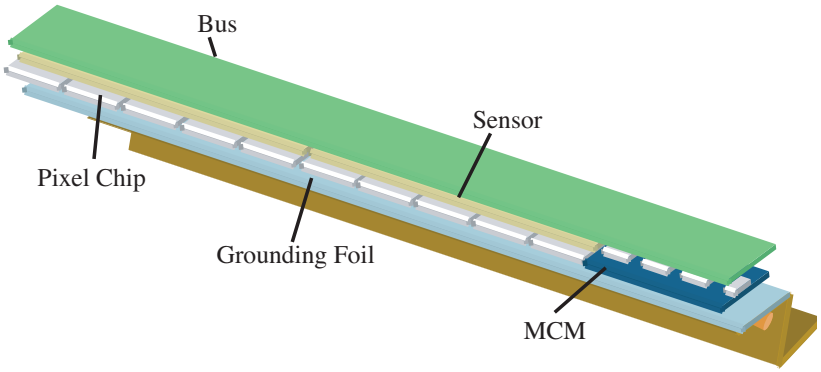


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Figure 2: Schematic drawing of half-stave.

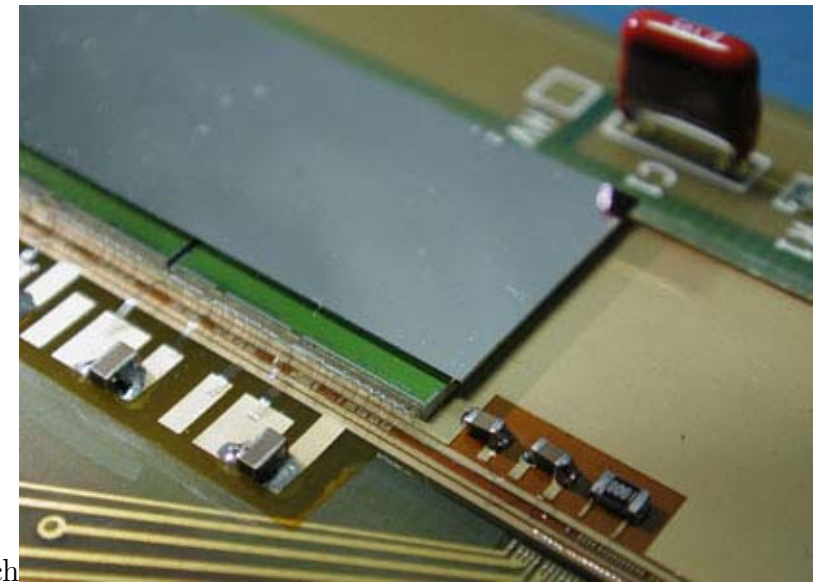
chch 

Figure 3: Picture of a ladder mounted on a bus.

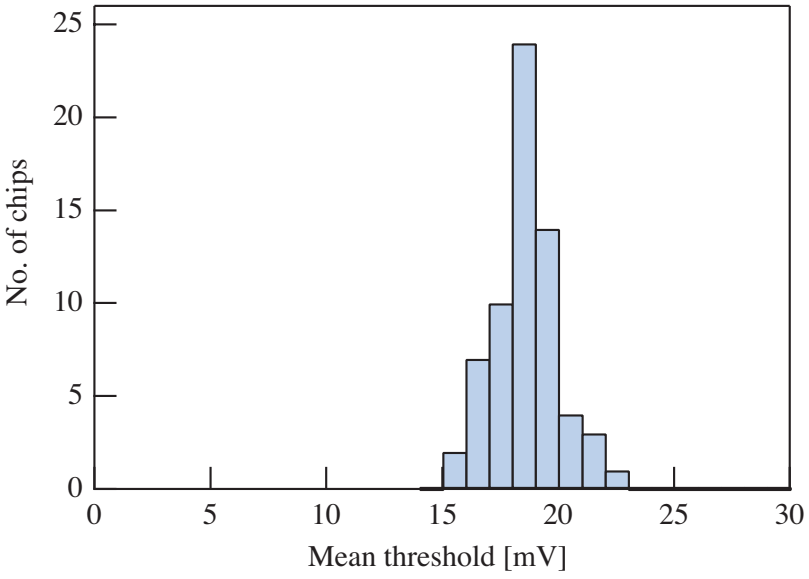
chch 

Figure 4: Mean threshold of all class I chips measured on one ALICE1LHCB chip wafer.

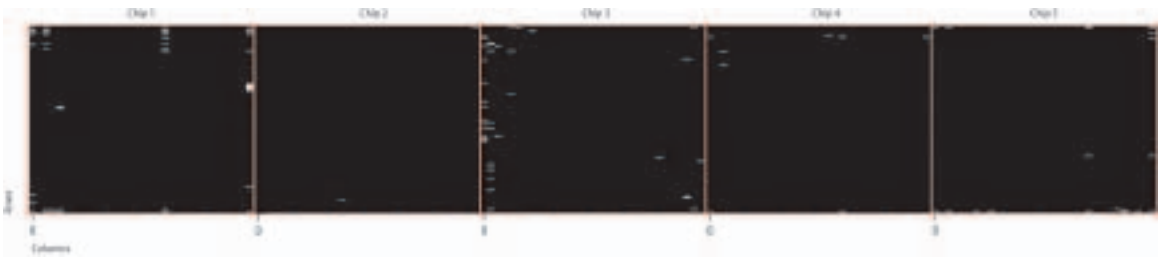


Figure 5: Pixel response to a ^{90}Sr-source of a thinned ladder bump bonded at VTT.

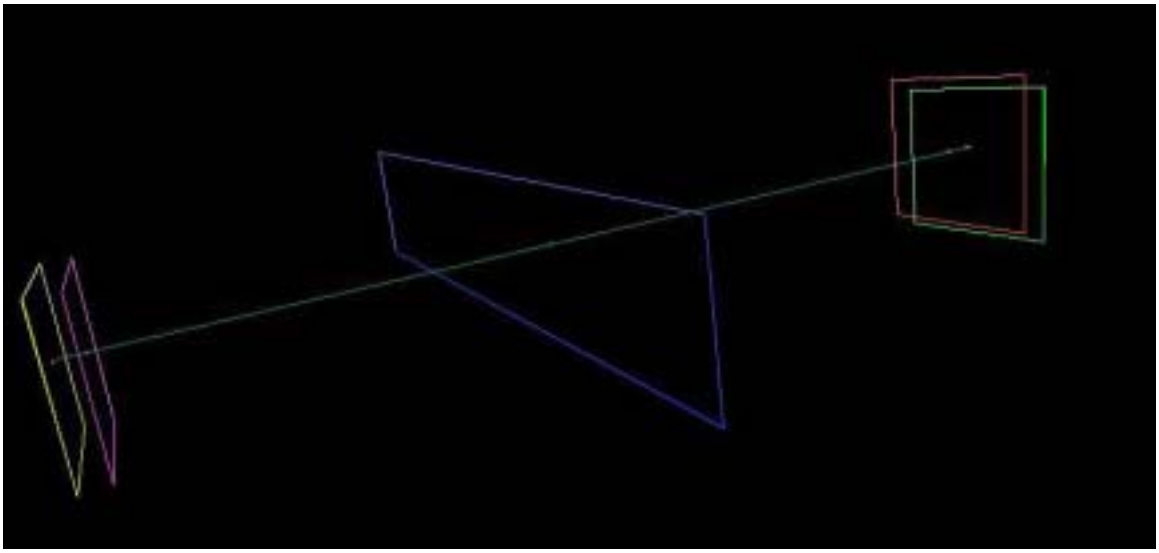


Figure 6: Reconstructed track in the VTT2-2001 ladder.

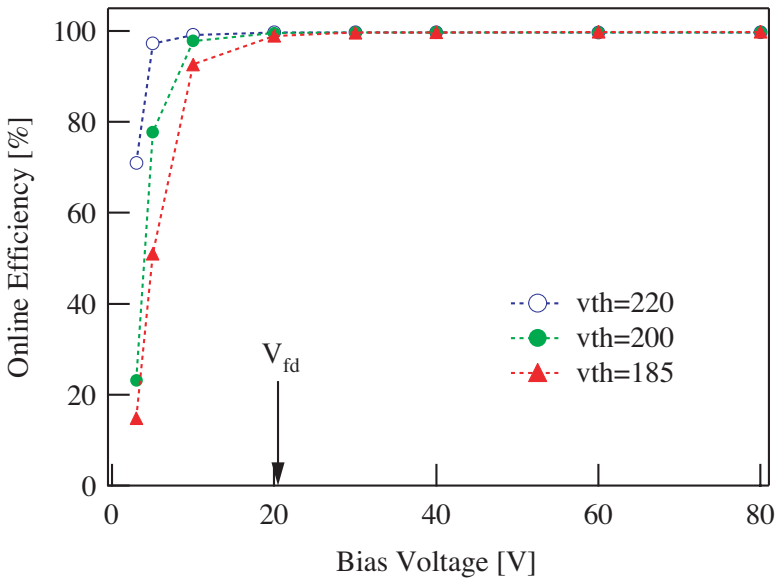


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Figure 7: Online efficiency measured as function of the sensor bias voltage on VTT2-2001 ladder for three different threshold settings.