Future Directions in Hybridization of Pixel Detectors

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Research Center of
Microperipheric Technologies

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Outline

- Introduction
- Wafer Bumping and Flip Chip Bonding for ATLAS
- Future Options and Requirements:
  - Bump size and Pitch
  - Lead Free Bumping
  - Thin Silicon
  - Integration of Passives
  - 3D Integration

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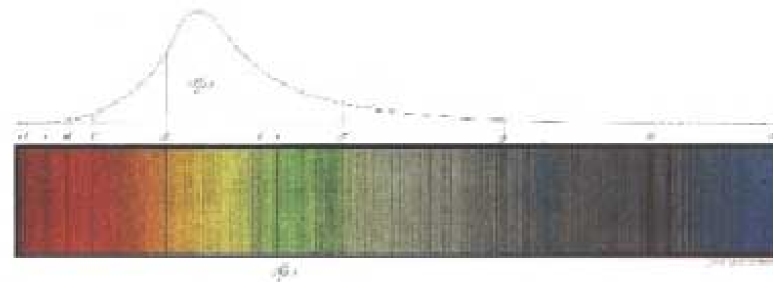
Joseph von Fraunhofer (1787 - 1826)

Researcher
discovery of "Fraunhofer Lines" in the sun´s spectrum

Inventor
new methods of lens processing

Entrepreneur
head of royal glass factory



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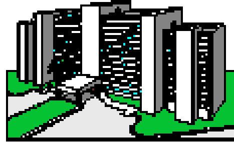
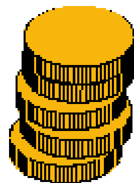
Fraunhofer in profile

56
institutes



9500
employees
(full-time
equivalence

900 million Euro
bugdet



Materials and components

Production technology

Information and communication

Microelectronics and microsystems

Sensor systems, testing technologies

Process engineering

Energy, contruction, environment, health

Technical and economic studies

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Research Center of
Microperipheric Technologies

- **220 Scientists and Engineers (+100 Students)/ Cleanroom 800 m^2**
- **Applied Research and Development of Advanced Packaging Solutions for Microelectronics**
- **Branch Labs and Centers in Chemnitz, Teltow, Paderborn, Oberpfaffenhofen and Munich**
- **Worldwide Technology Transfer and Consulting Services**

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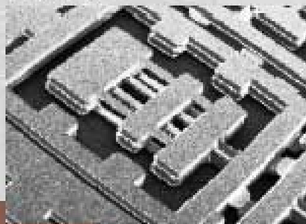
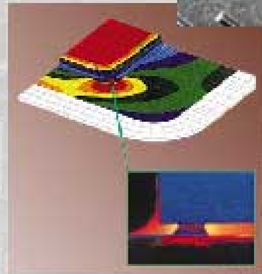
Material Development and Simulation

Micro Devices and Equipment



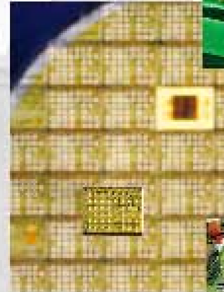


Mechanical Reliability and Micro Materials

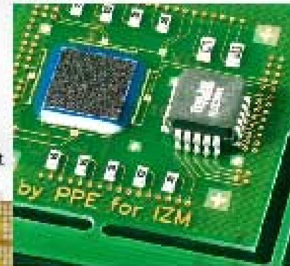
Polymeric Materials and Composites

Packaging Technologies

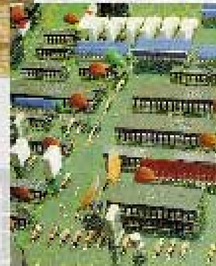
High Density Interconnect & Waferlevel Packaging



Chip Interconnection Technologies



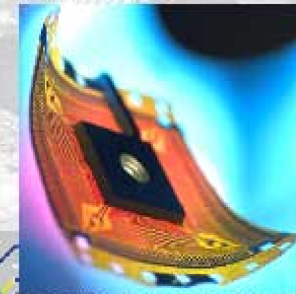
Board Interconnection Technologies

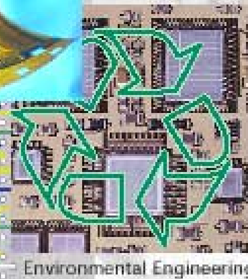


Packaging for Microelectronics / Microsystems and Mechatronics

System Integration

Pervasive Computing System Technologies





Environmental Engineering

Advanced System Engineering

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Packaging Roadmap

2000 till 2004

LC-TB-BGA, **stacked modules**, VSI, chip in polymer, S-CSP, **Polytronic**, **ULC-CSP**, **Flex-Sys**, **stacked CSP**, **WLP**, thin silicon

1998 1999

TB-BGA, **MC-BGA**, **FC-MCM**, **COF/FCOB**, **CSP**

1997

BGA, SQFP, MCM COB, PGA, QFP, FC, VSO, CCC, **SO**, **SOJ**, TFP, **VTFP**, **V-PAK**, **stacked chips**, **DIP**

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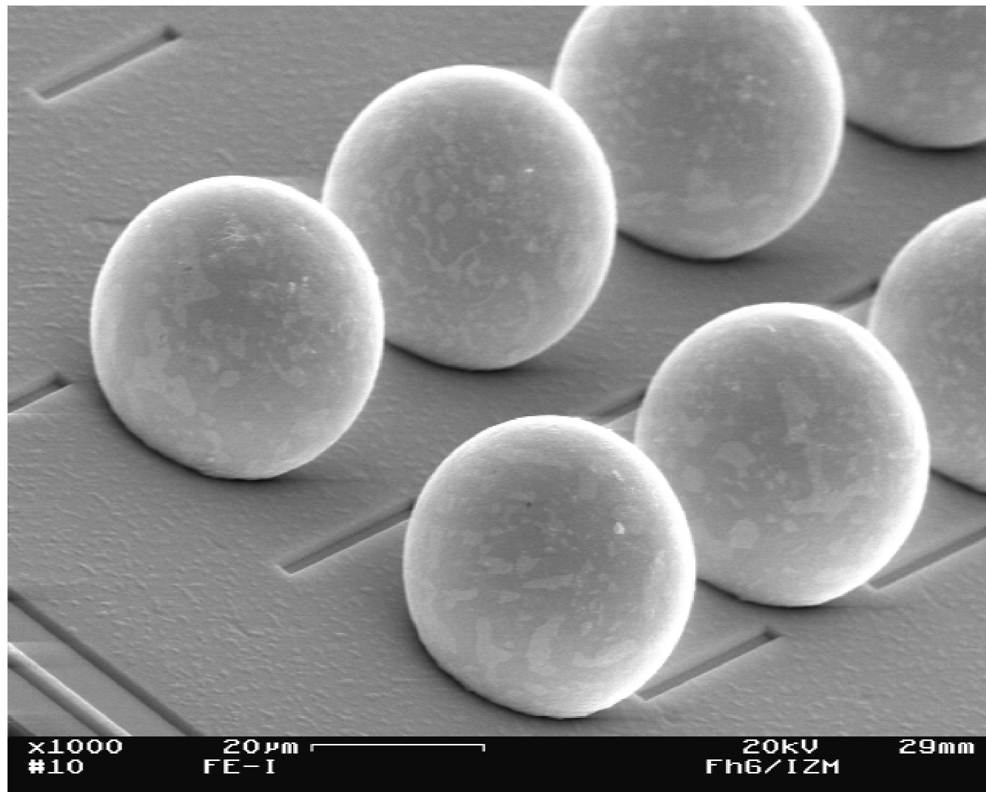
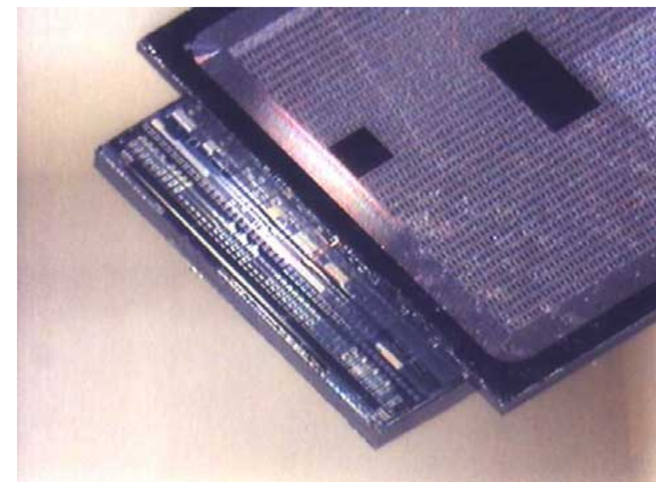
Wafer Bumping and Flip Chip Bonding for ATLAS





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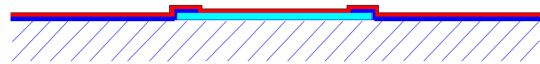
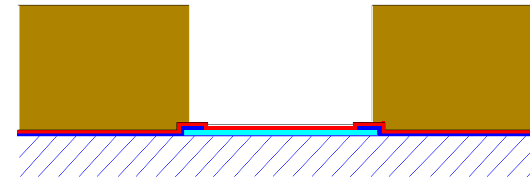
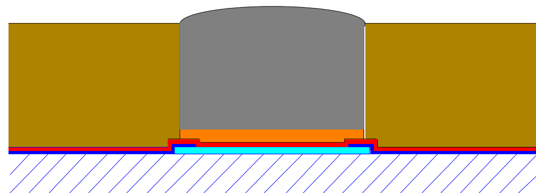
Processflow PbSn-Bumping using Electroplating



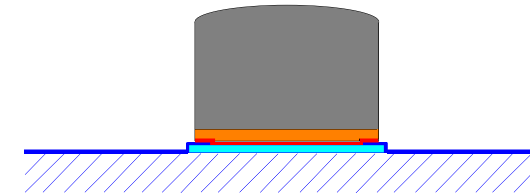
Sputter Etching and Sputtering of the Plating Base / UBM



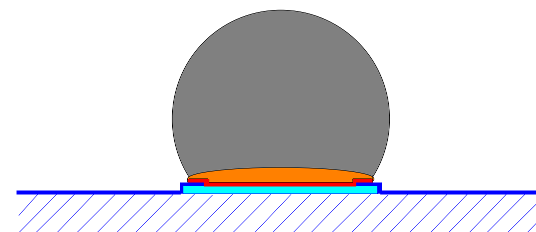
Spin Coating and Printing of Photoresist



Electroplating of Cu and PbSn



Resist Stripping and wet Etching of the Plating Base



Reflow

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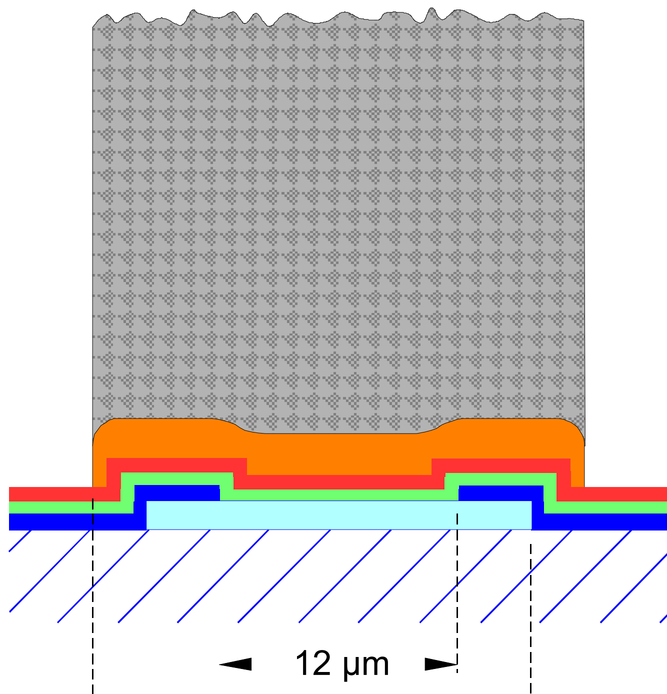
Fundamental Construction of Bumps on ATLAS Detector Chips



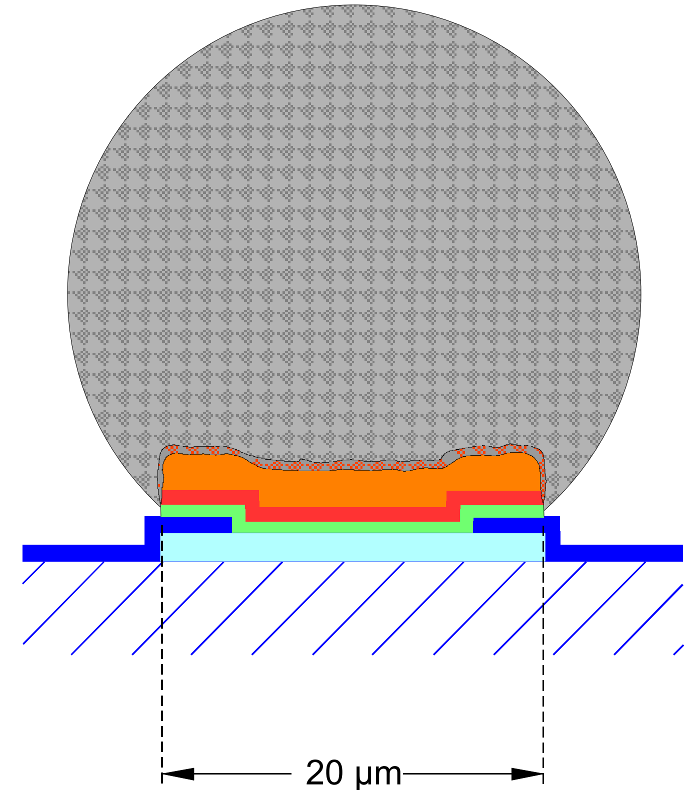
25 µm electroplated PbSn63

5 µm electroplated Cu
as solderable base

300 nm sputtered Cu
as plating base

200 nm sputtered Ti:W
as adhesion layer
and diffusion barrier

Al chip pad with
overlapped passivation



as plated

after reflow

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PbSn Bumping Process Flow in Detail

- incomming optical inspection
- cleaning SRD
- sputtering platingbase ion etching (Ar) Ti:W (200 nm) / Cu (300 nm)/
- optical inspection
- warp & sheet resistance control
- photoresist spin on / prebake/ exposure / develope/ postbake
- optical inspection
- resist thickness control measurement
- pre-conditioning (plasma O_2)
- pre-conditioning (etching)
- electroplating Cu
- rinse (DI water)
- electroplating PbSn60
- 3 x rinse (DI water)

2

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PbSn Bumping Process Flow in Detail (cont.)

2

photoresist stripping (aceton)

optical inspection

UBM etching Ti:W (H_2O_2)

UBM etching Cu ($CuCl_2$)

optical inspection

Reflow

bump shape control high measurement

photoresist spin on / bake

Wafer thinning

Wafer dicing

resist stripping (aceton)

optical inspection (100 %)

selection & sorting

Flip Chip Bonding

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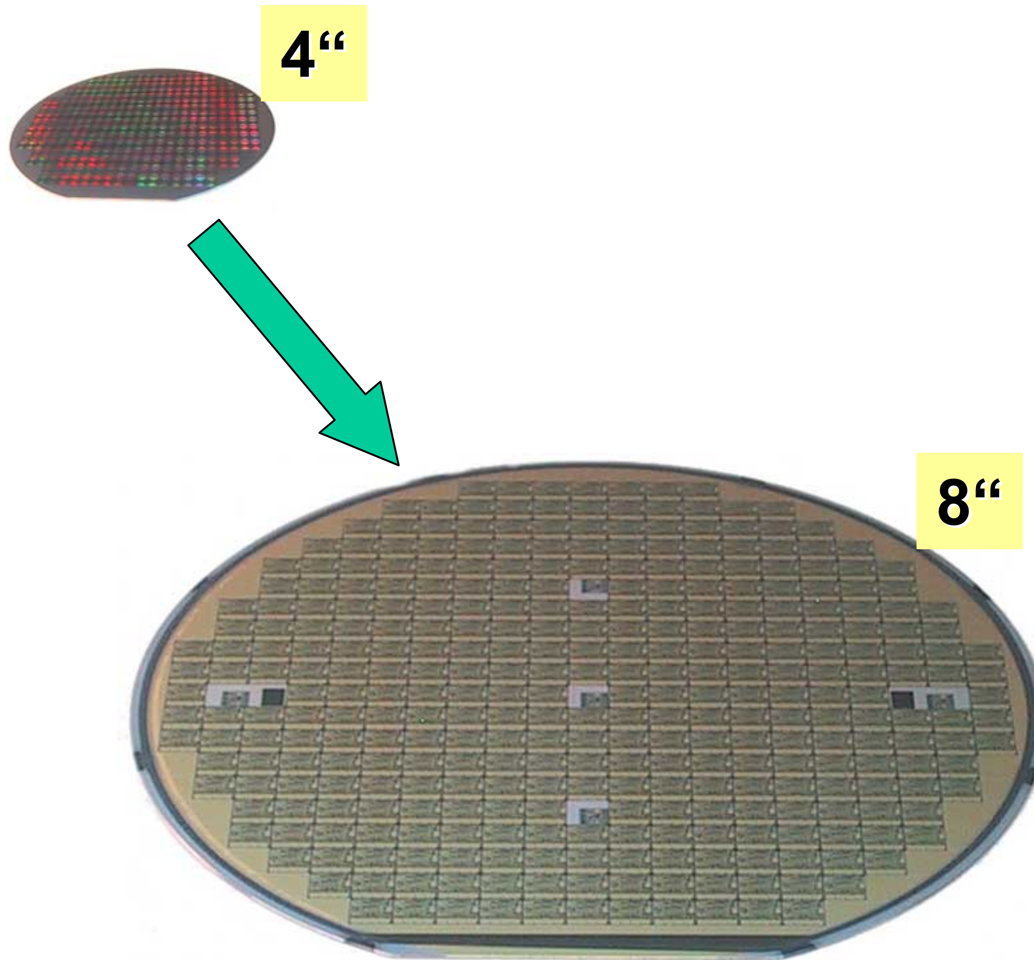
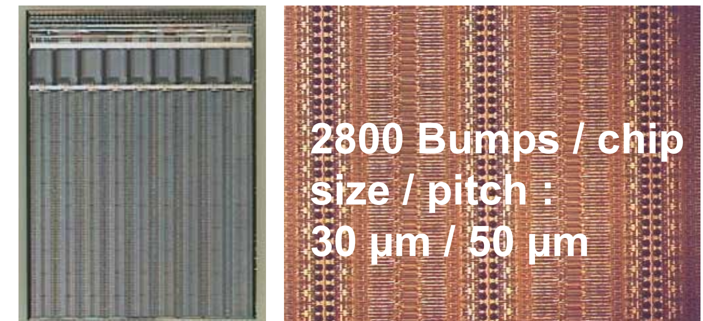
High Density ECD Bumping & Flip Chip
IBM 0.25 µm rad tolerant design





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Cleanroom
800 sqm

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Electropłating Equipment Semitool Equinox

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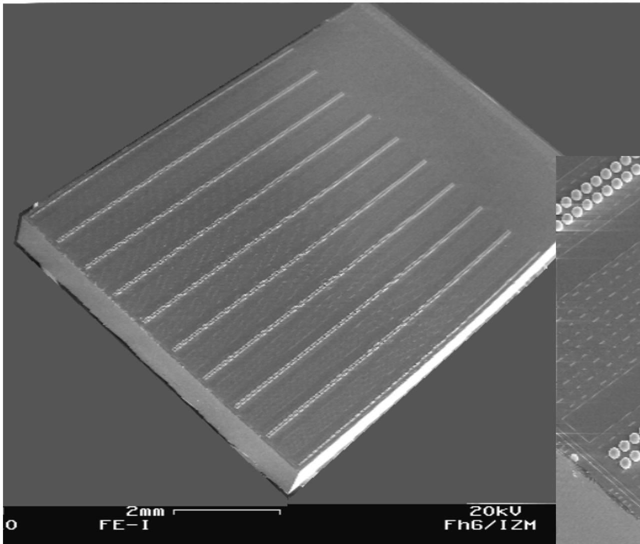
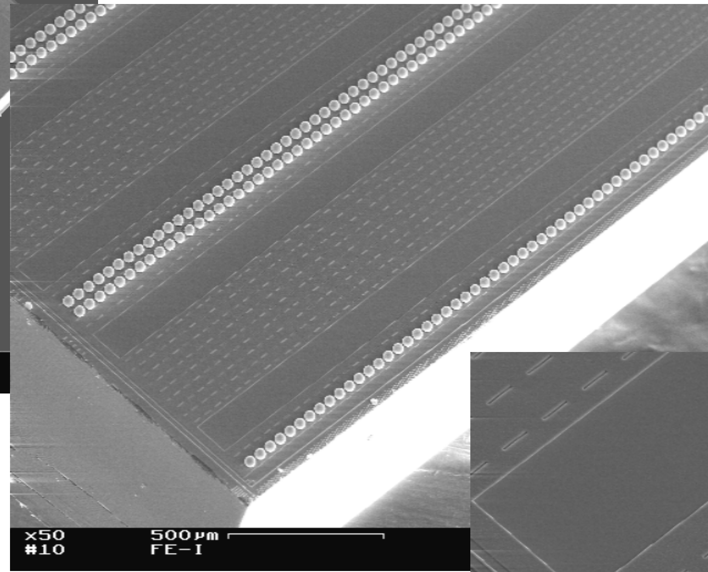
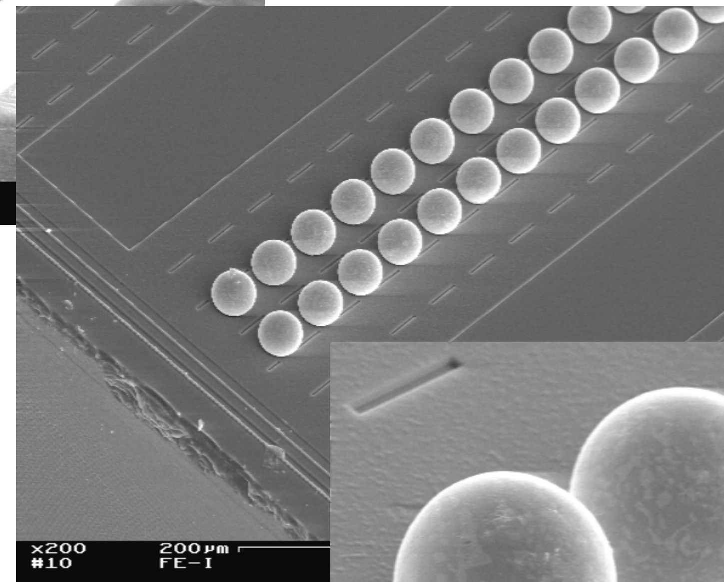
Bumped FE-I Chip

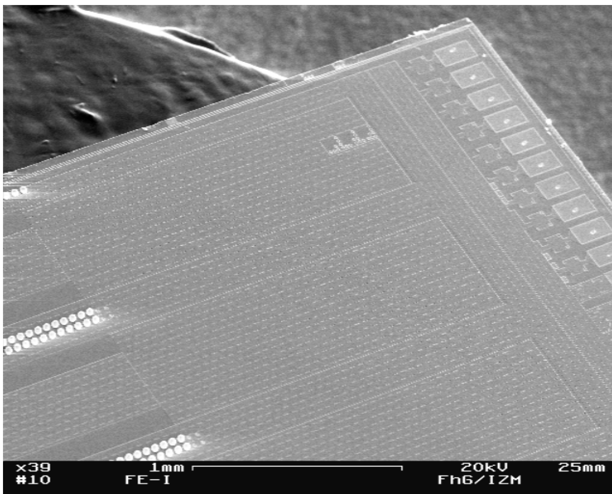
IBM 0.25 µm rad tolerant design

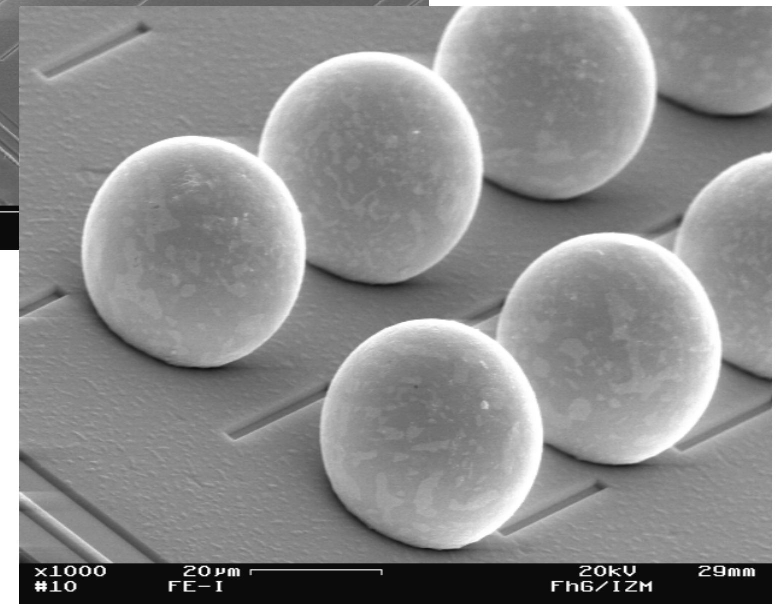


Chip with 9 column pairs









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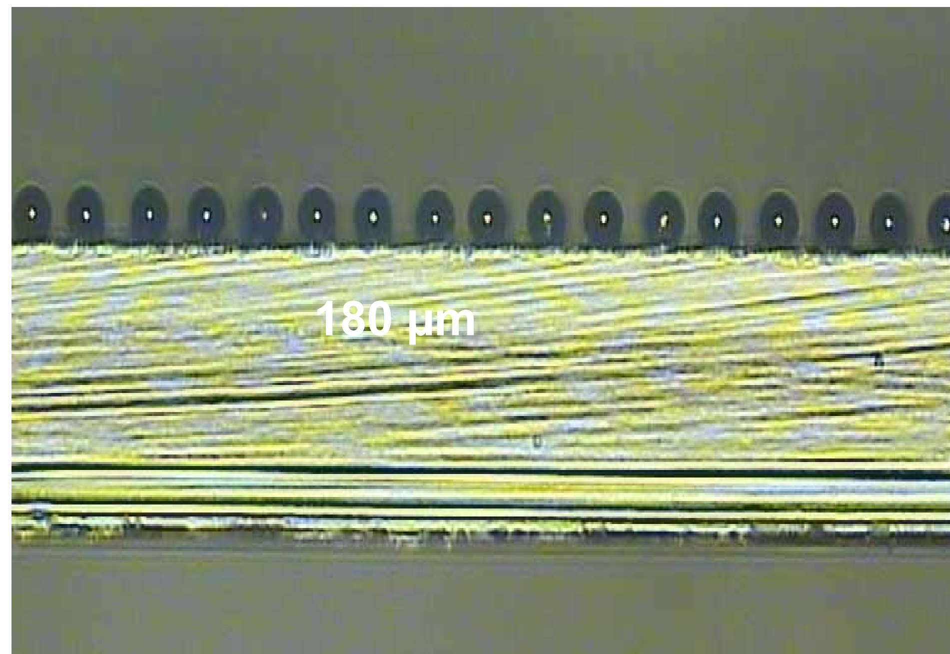
Thinning of bumped FE - I wafers:

development of resistlayers to protect the bumps from damage during the grinding and etching process



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Optical Bump Inspection

Automated Defect Inspection System NSX-90 August Technology

Inspection time:

ATLAS FE-I [8“]

bump size: 20µm

pitch: 50µm

≈ 120 min / wafer all bumps

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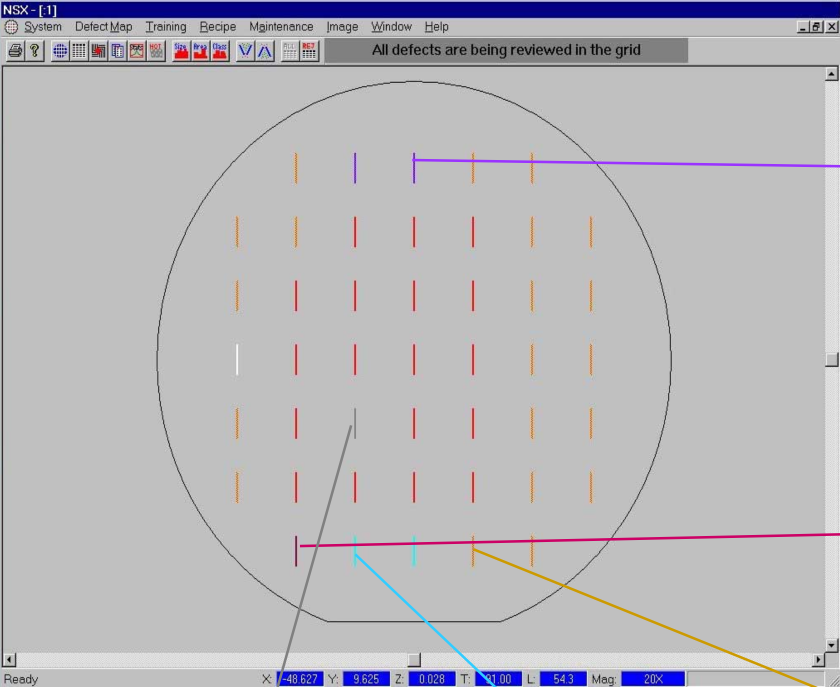
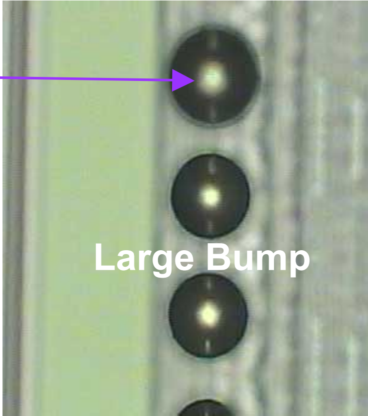
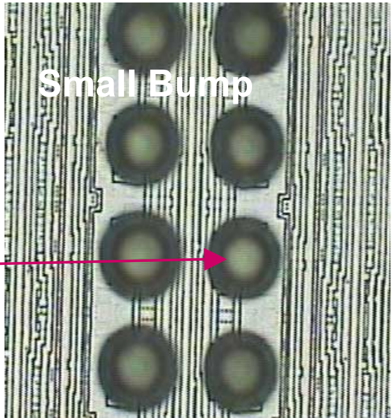
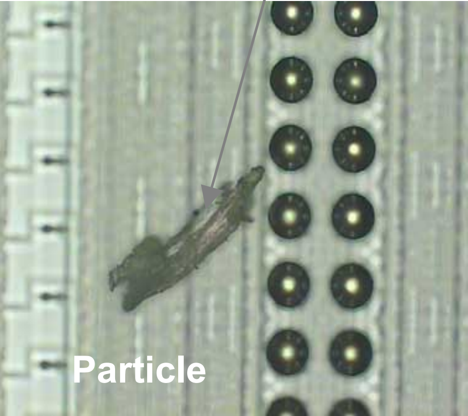
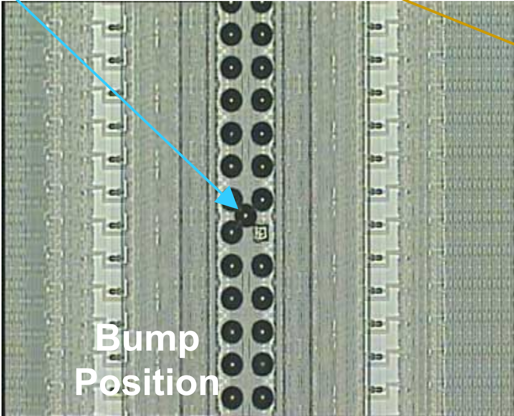
Defect Classes

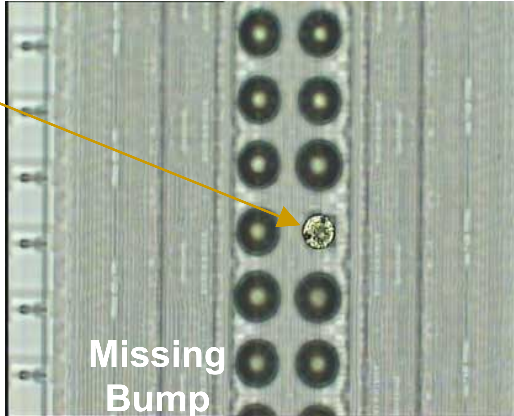












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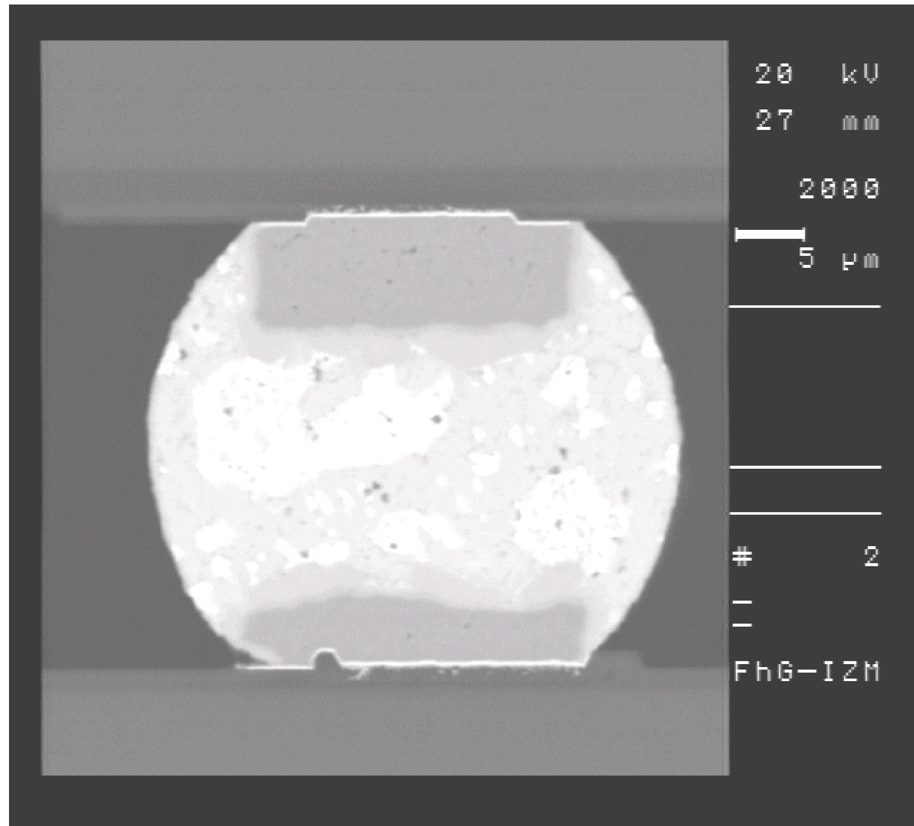
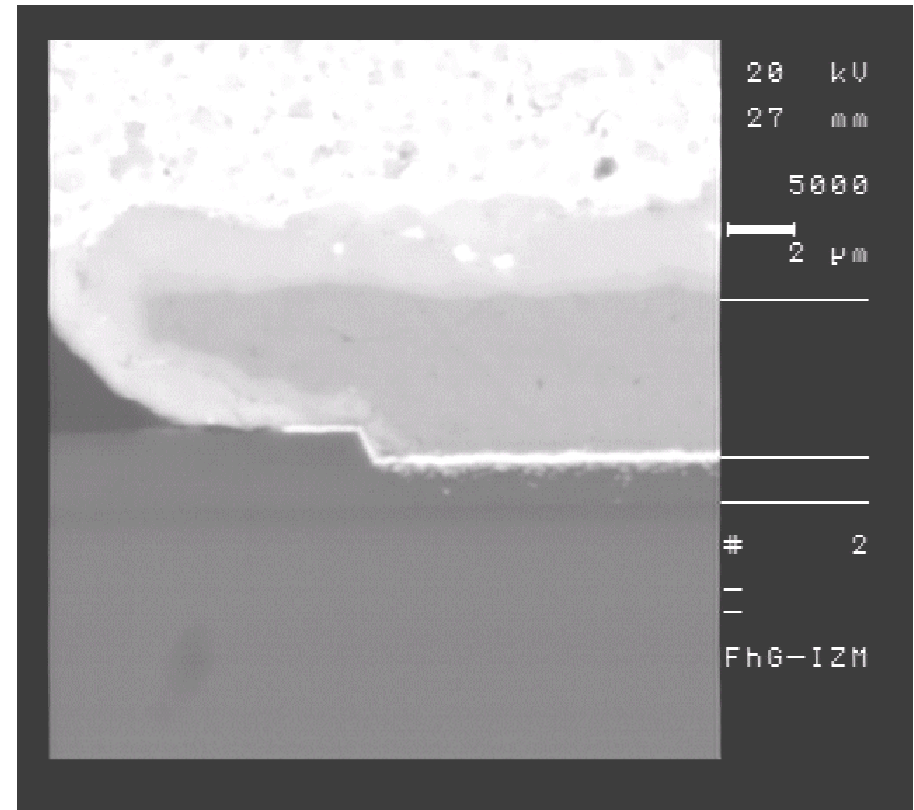
Flip Chip Bonds





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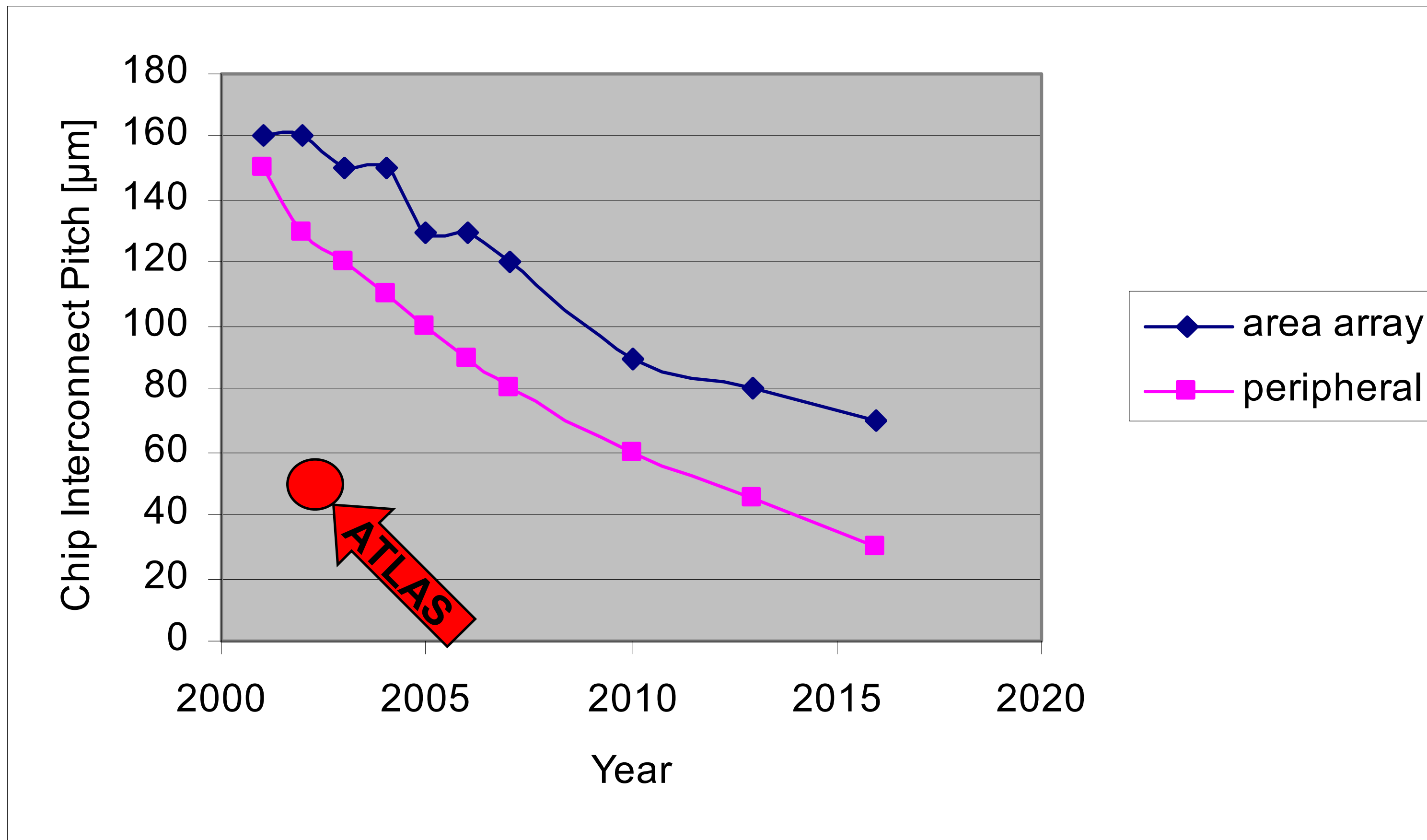
IC Technology Roadmap: Chip Interconnect Pitch



Source: ITRS

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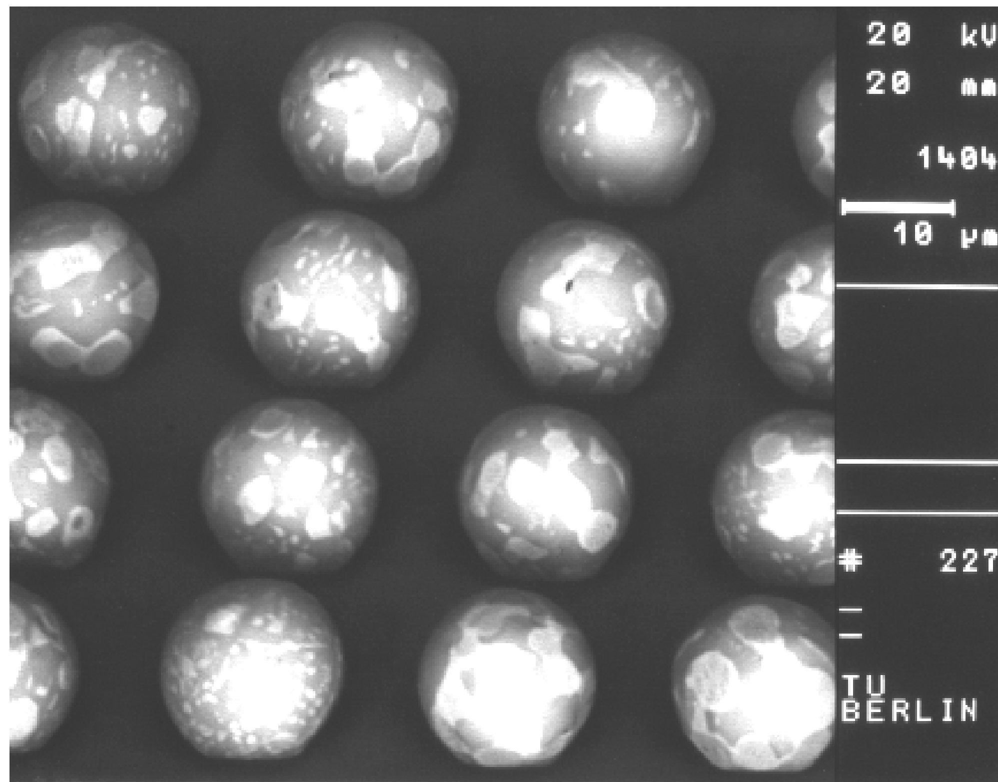
Future Requirements: Bump size and Pitch



Solder Bumping PbSn37/63

Diameter: 10 µm

Pitch: 20 µm

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Future Requirements: Lead Free

Solder for FC Interconnects		Melting Point
SnBi	42/58	138°C
PbSn	37/63	183°C
SnZn	91/9	199°C
SnAg	96.5/3.5	221°C
SnCu	99.3/0.7	227°C
AuSn	80/20	280°C
PbSn	95/5	314°C

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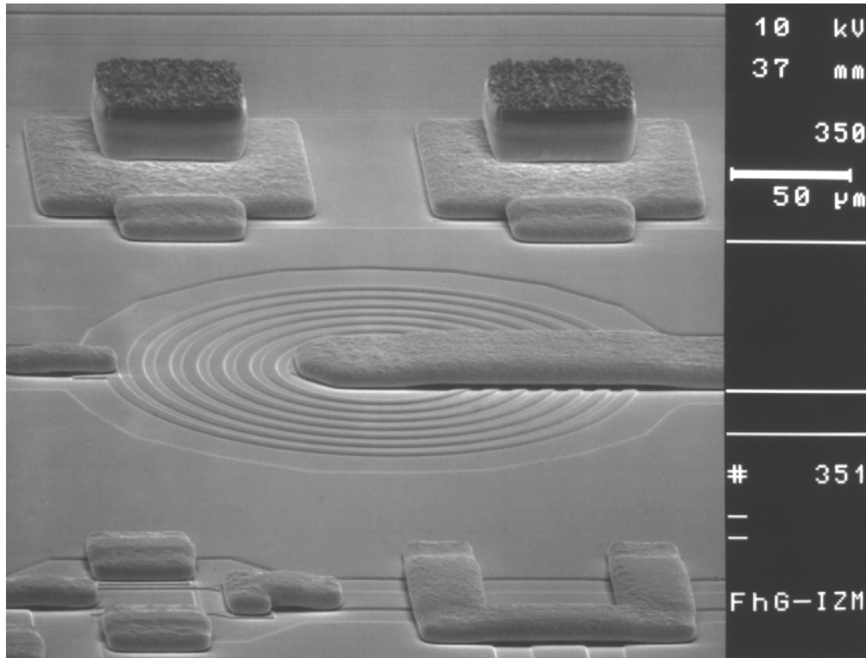
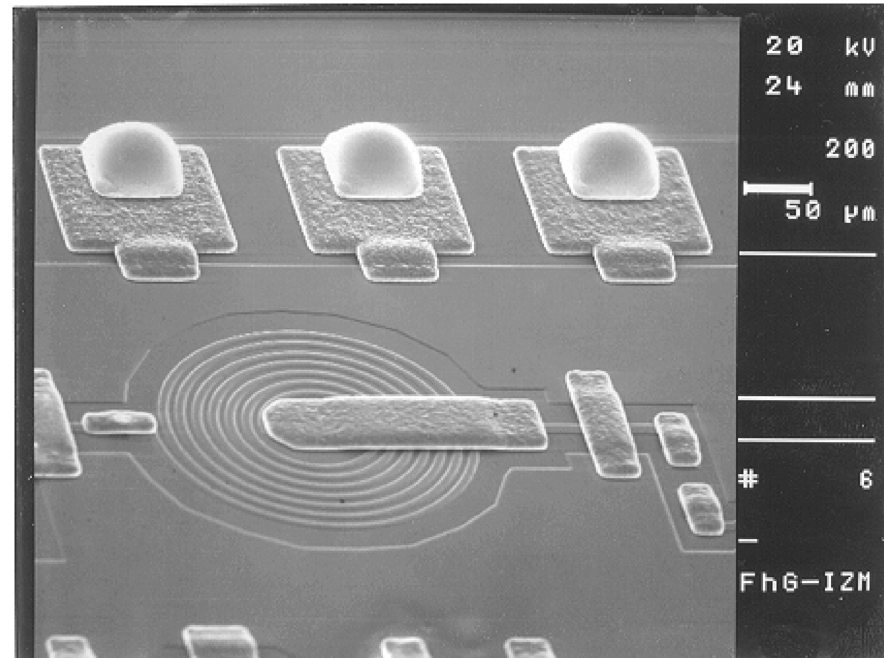
Au-Sn Bumping on GaAs



Au-Sn-Bumps - (48 x 48) μm²
after Electroplating



Au-Sn-Bumps - (48 x 48) μm²
after Reflow

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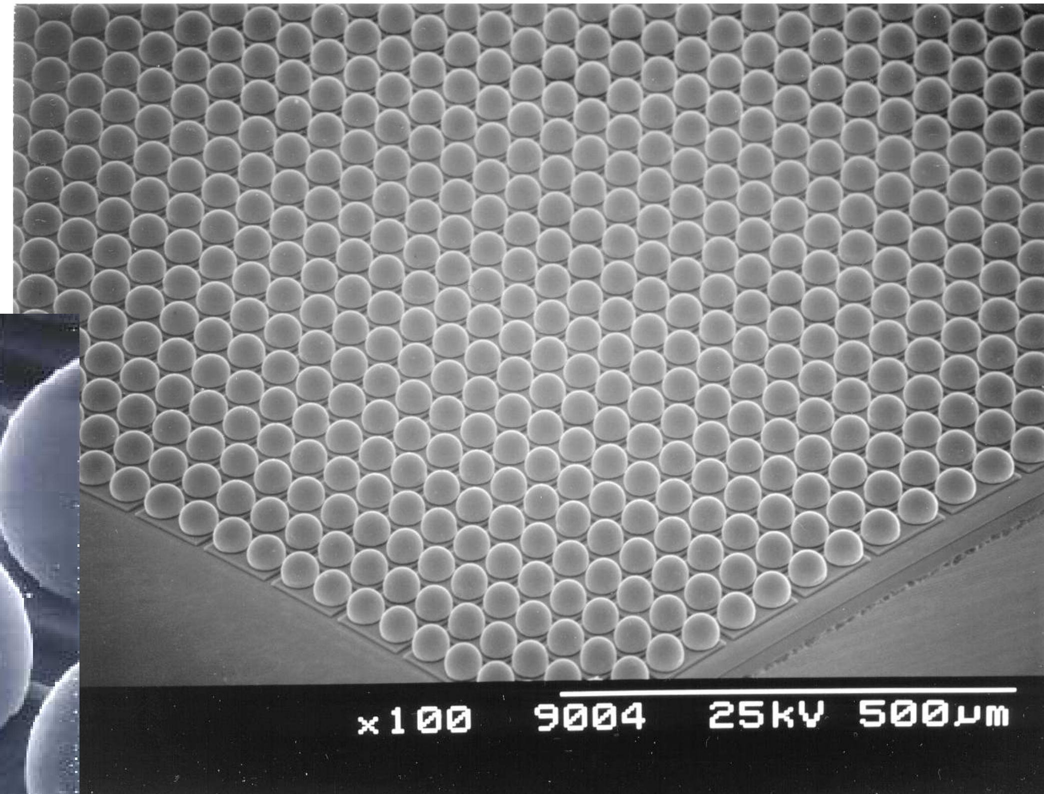
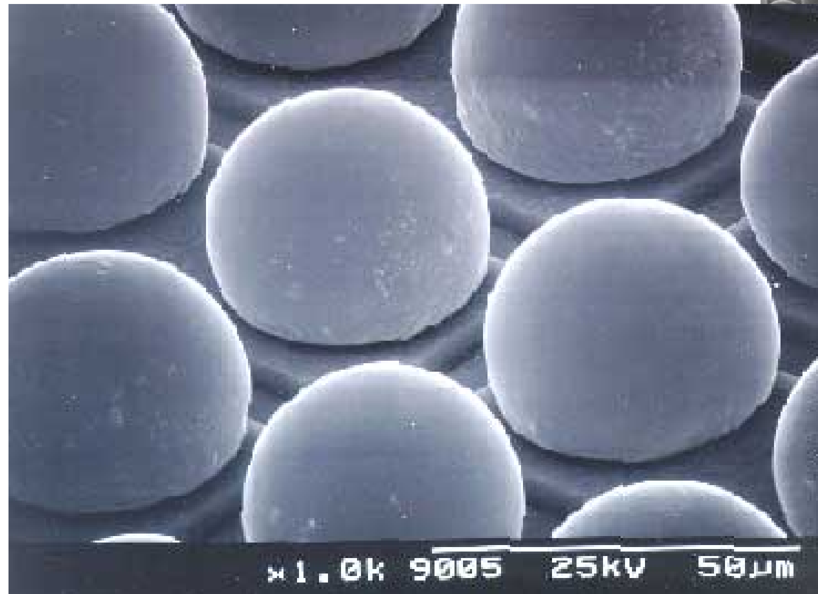
AuSn Electroplated Bumps

- 50 µm pitch full array
- 30 µm AuSn20
- x-ray pixel detector





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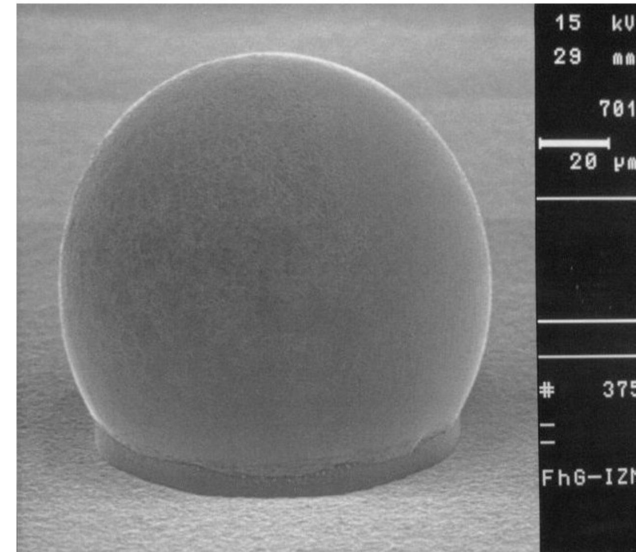
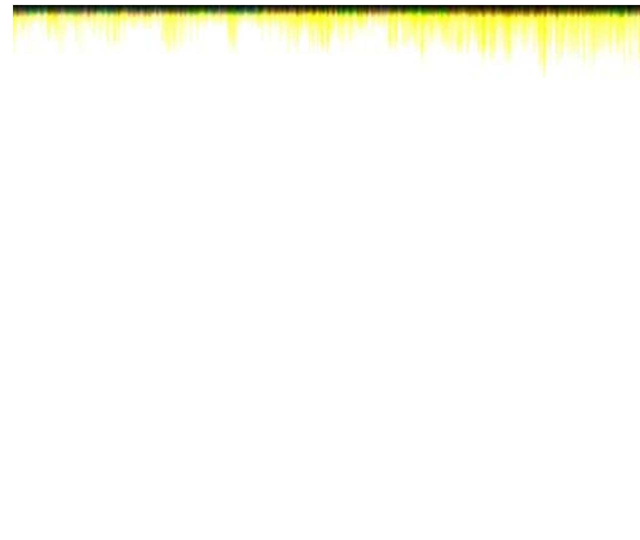
Lead Free Bumping

SnAg

Meeting the requirements of future environmentally friendly lead-free flip chip interconnects basing on the EU-directive ROHS 2000





Bump dimensions
Size: 30 -100 µm
Pitch: down to 50 µm
Ag composition: 3.0 ~ 4.0 at.%
Melting point: 221 °C

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Future Requirements: Thin Silicon

Silicon becommes flexible when thickness is reduced down to less than 30µm

- bending radius 1mm / 1µm thick-ness
- fully flexible and ultra thin systems available
- best opportunities to proceed with FC and CSP technologies
- basis for 3D chip integration

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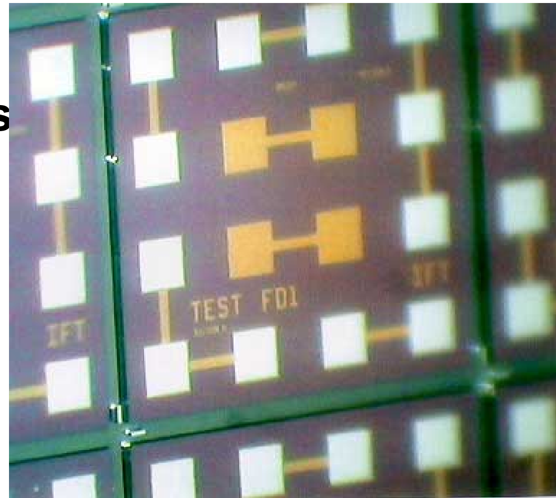
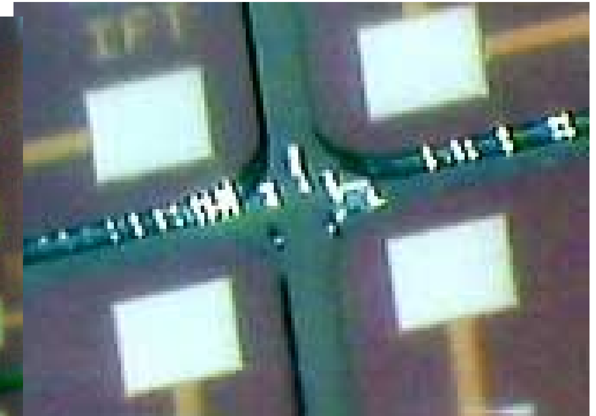
Dicing by Thinning

Rounded chip corners





•Dry Etching of about 30µm deep groves

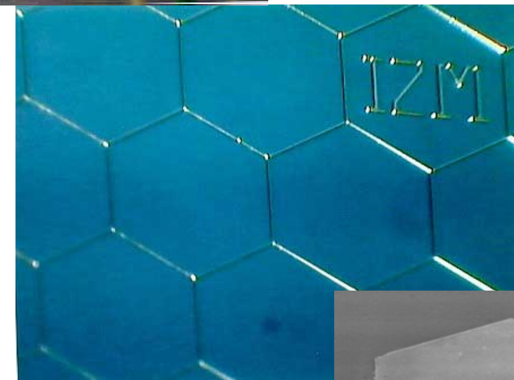
•Backside Grinding - Etching - CMP

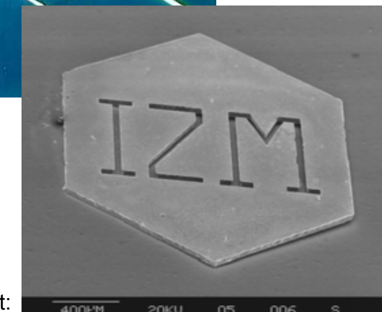
•nearly ideal chip edges (rounded corners are possible)

• shorter process times for singulation into individual chips

• narrow cuts save silicon area for small chips

•non rectangular dies are possible





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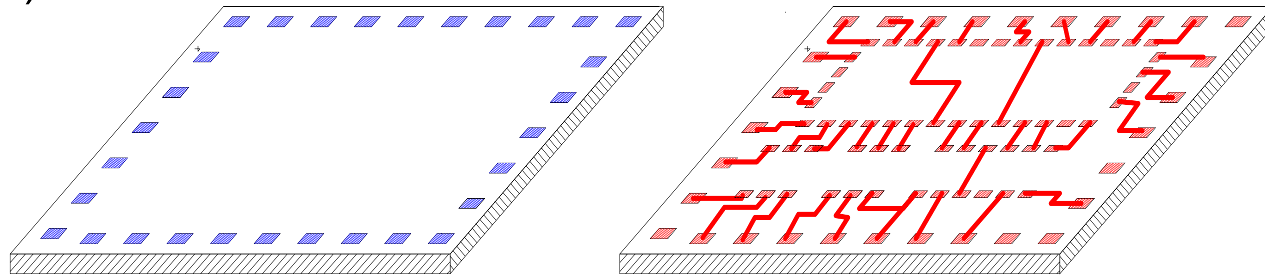
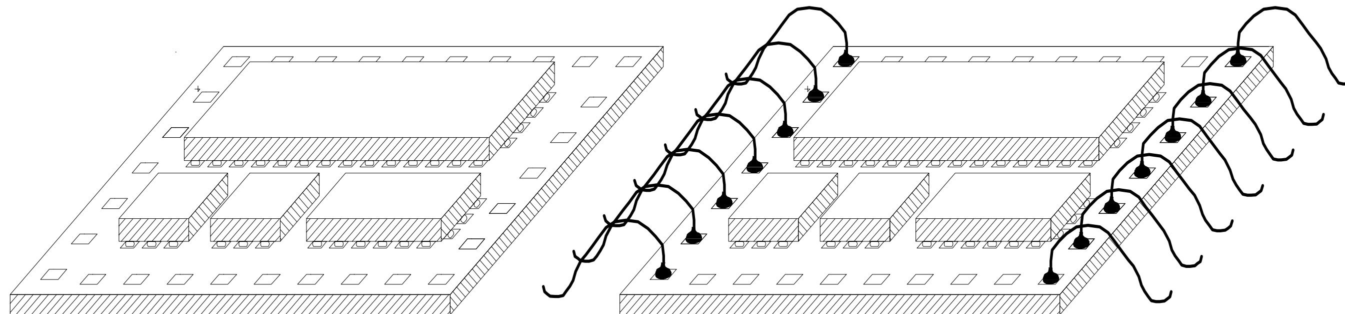
Status of Silicon on Silicon Modules

base chip
(i.e. sensor)

redistribution
polymer / copper
(if required)





FC bonded
system chips

wire bonds to next
packaging level
(flex or pwb)

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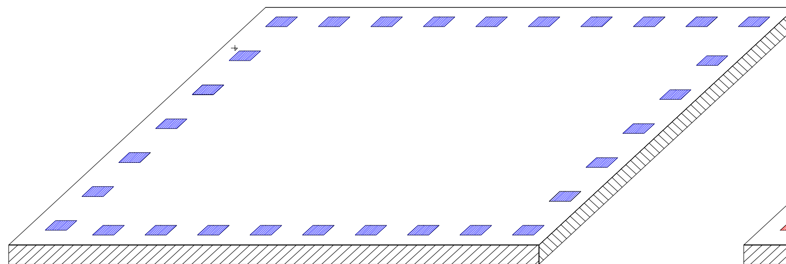
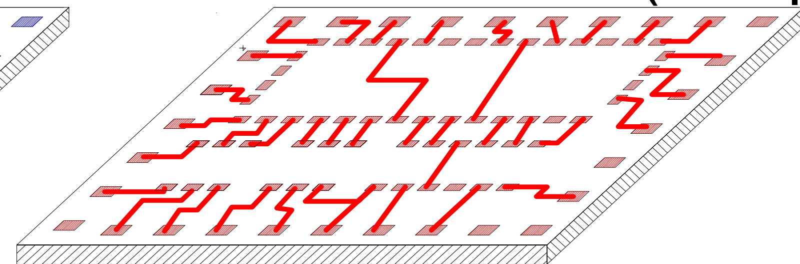
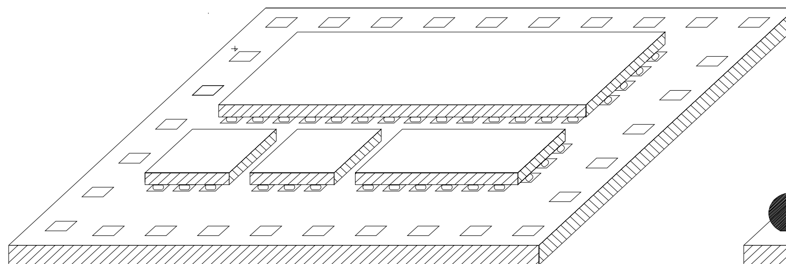
Thin Dies help to avoid Wire Bonds

base chip

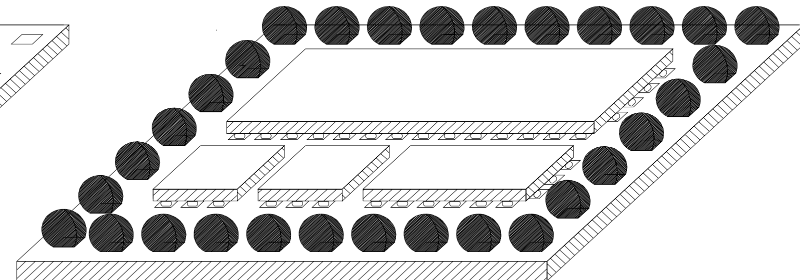


redistribution
polymer / copper
(if required)





FC bonded thinned
system chips



balls for interconnection
to the next packaging level
(flex)

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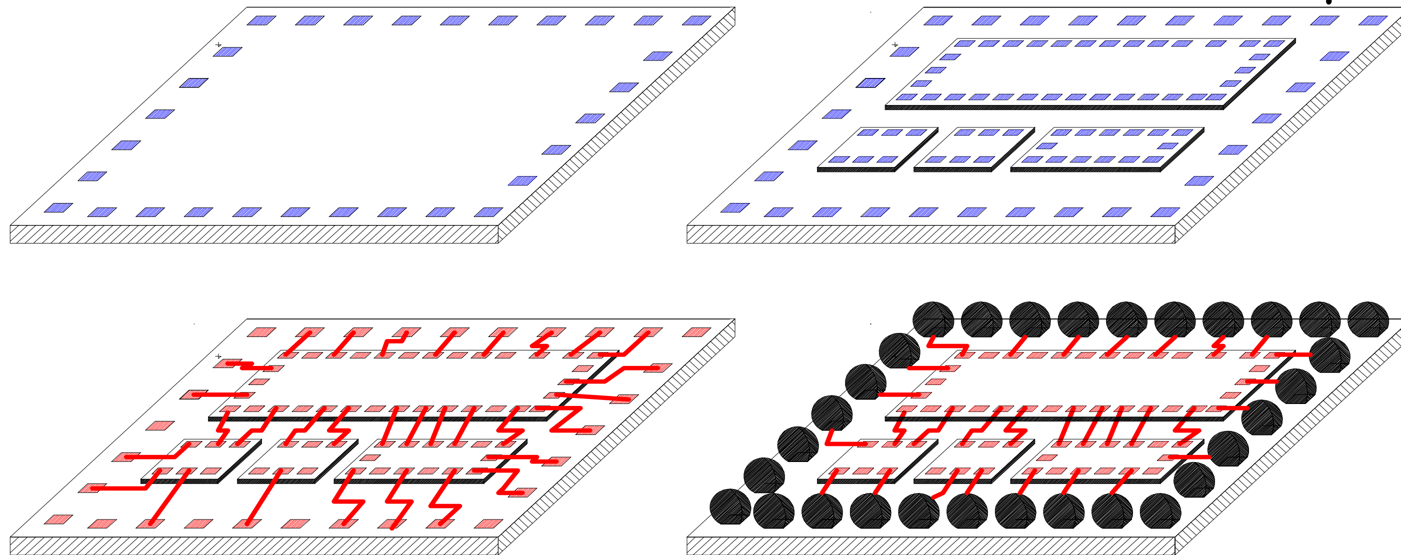
Silicon on Silicon Modules with direct interconnectes Dies

Base Chip

Mounting of thinned Dies d=20µm



Redistribution
Polymer / Copper

Balls für
Boardmounting

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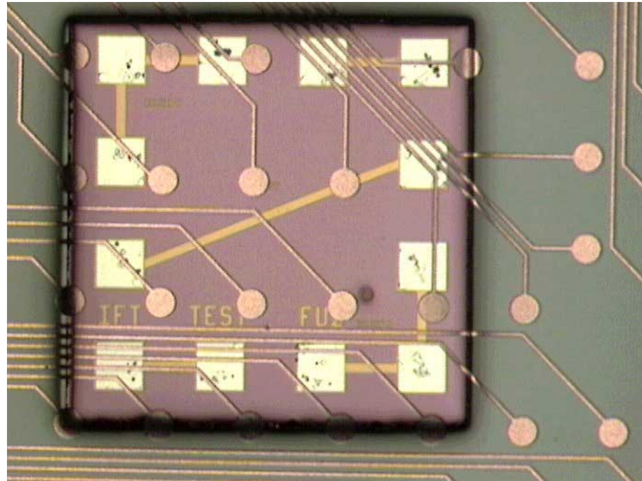
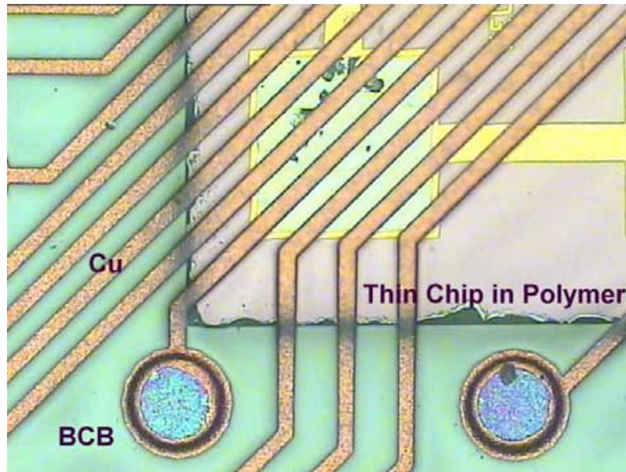
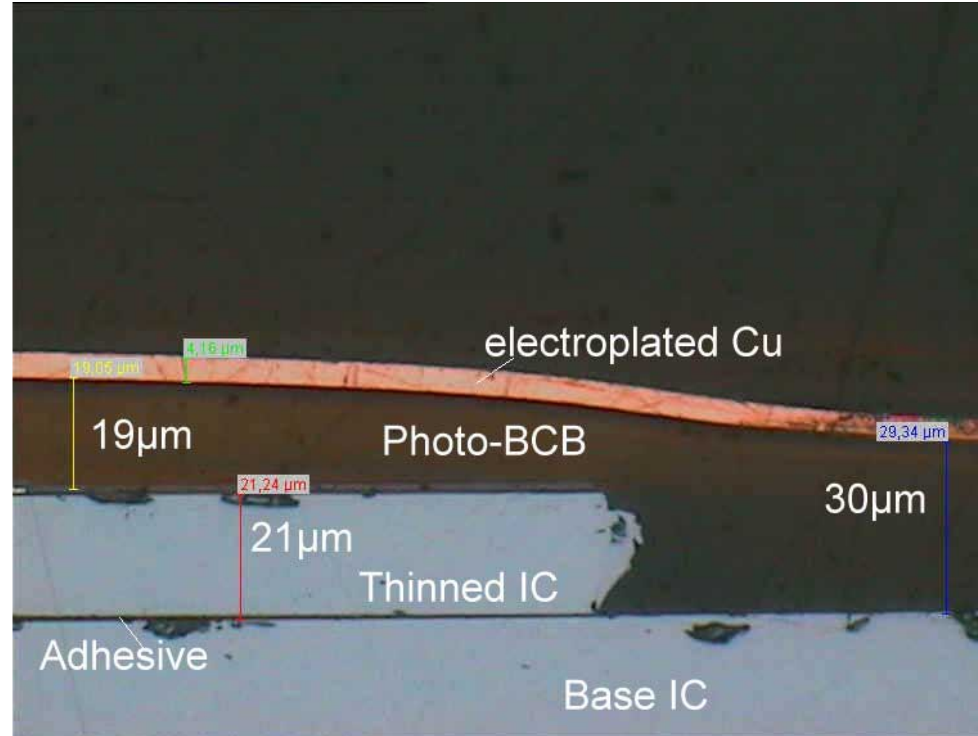
Silicon on Silicon Modules with direct interconnectes Dies







Reliability

passed 1000 cycles
-55°C / +125°C

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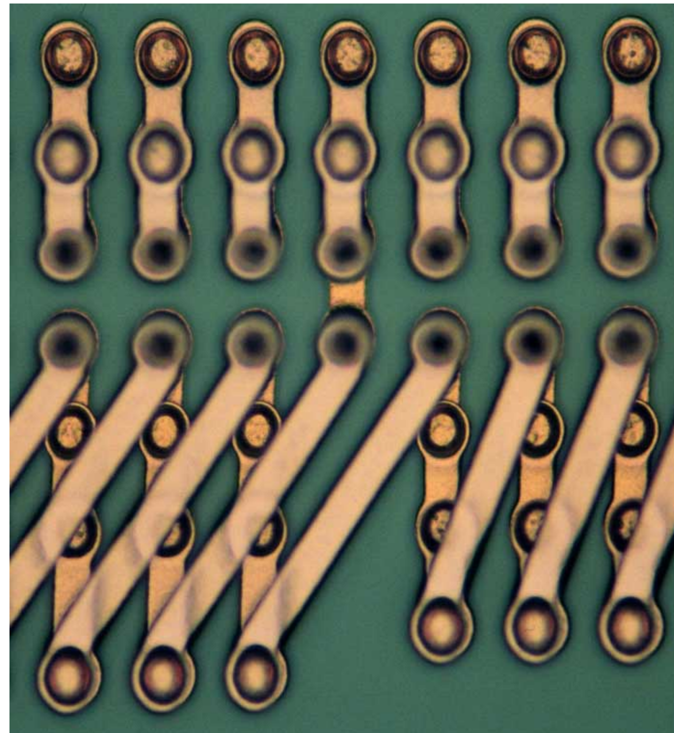
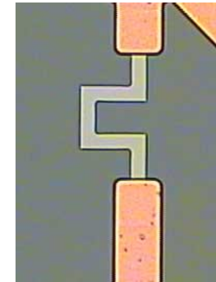
Future Requirements: Integration of Passive Components

ATLAS
MCM - D

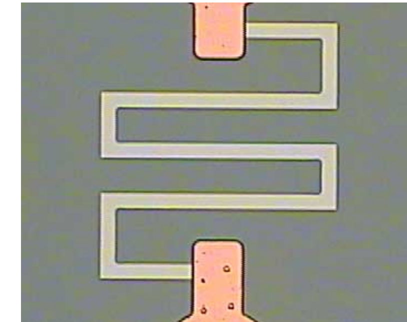
Si Substrate
Multilayer of 5 metal & 5 dielectric layers
Dielectric:
Photo-BCB: 5 µm
Metallization:
Ti:W/Cu - ep. Cu (3 µm)



thinfilm resistors

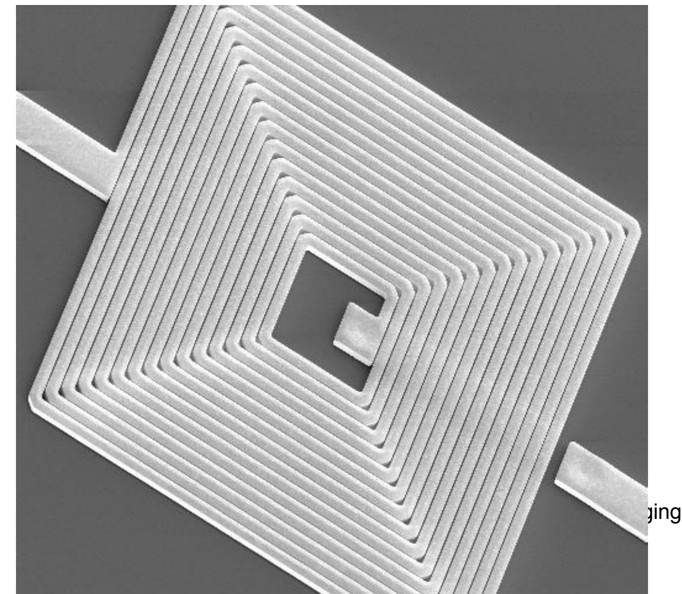


R = 1kΩ



R = 5kΩ

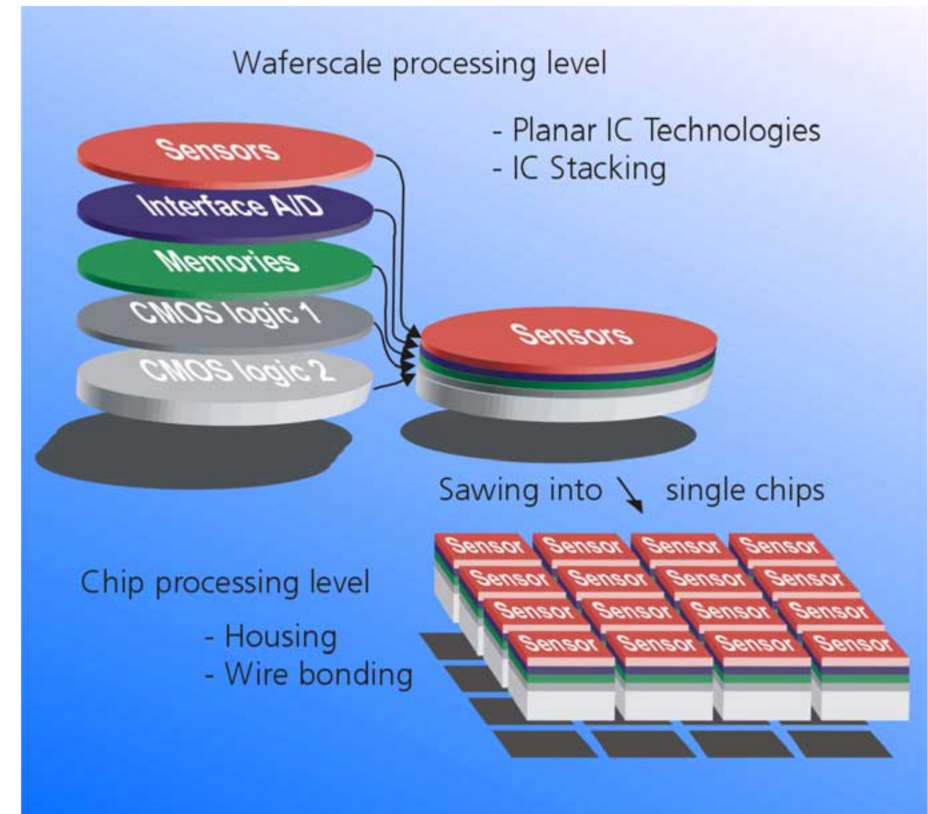
thinfilm inductors



Future Requirements: 3D Integration:
Vertical System Integration - VSI

- **Increased Performance**
  - **Less wiring delay**
  - **More bits of memory / cm²**
- **Combination of the advantages of different device technologies**

- **Portable Systems (minimum volume)**
- **Systems for high parallel signal processing**



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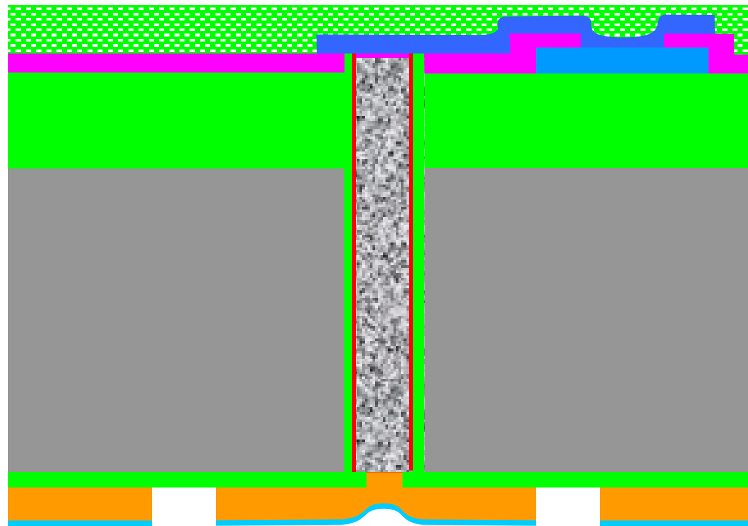
Vertical System Integration
InterChip Via Technology (ICV) / Soldering Concept

Top Wafer



- **Fabrication of Tungsten or Copper filled InterChip Vias on Top Substrate**
- **Via Opening and Metallization**
- **Thinning (20µm)**
- **Opening of Plugs**
- **Electroplating**

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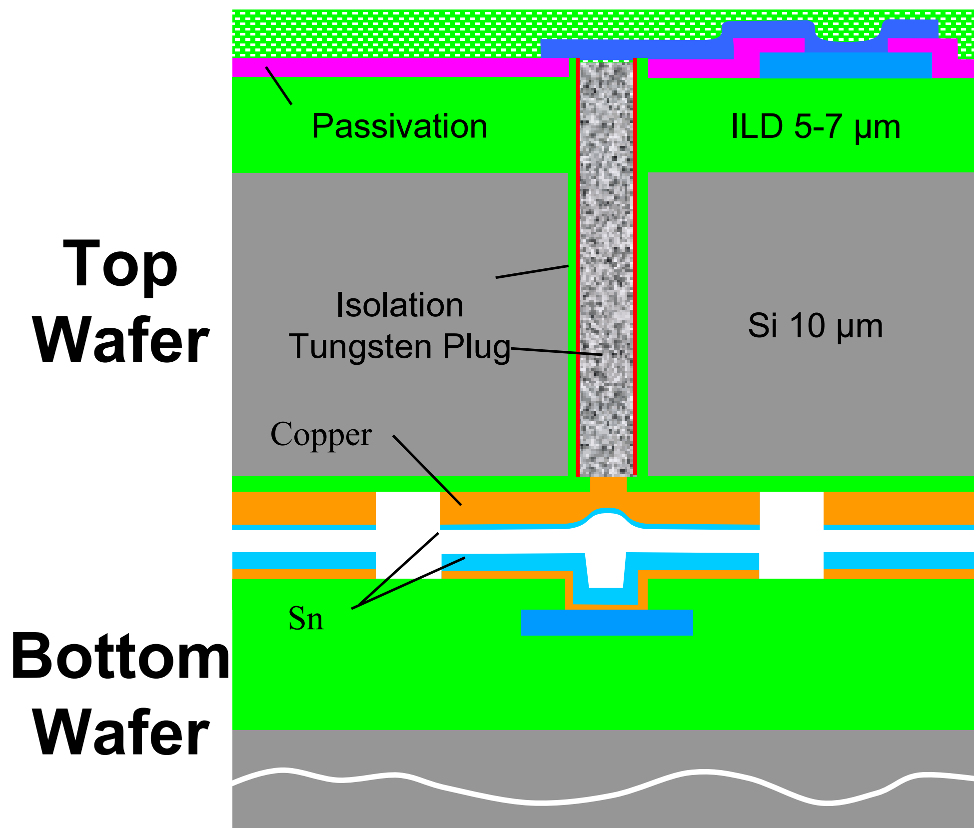

- **Fabrication of Tungsten or Copper filled InterChip Vias on Top Substrate**
- **Via Opening and Metallization**
- **Thinning (20µm)**
- **Opening of Plugs**
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- **Alignment and Soldering**

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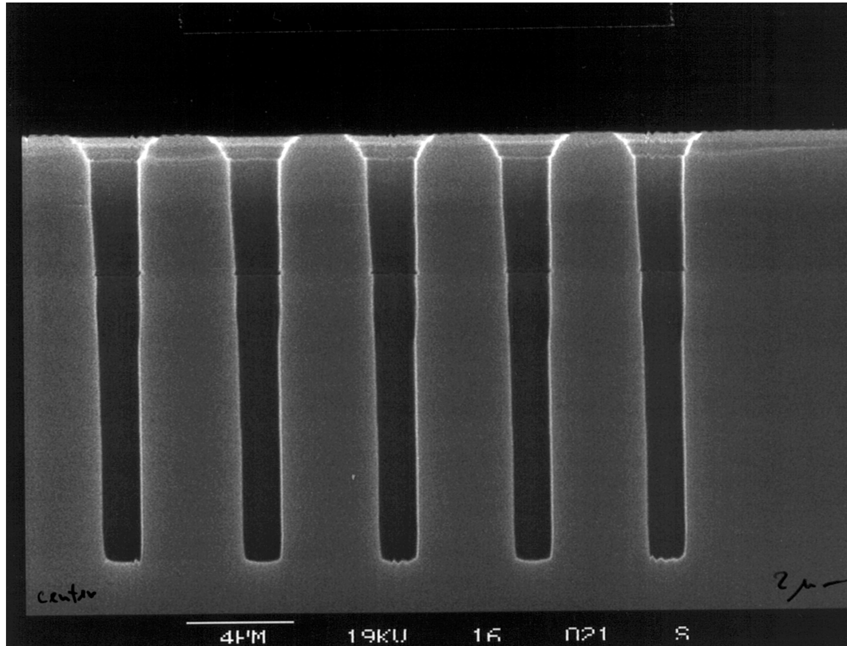
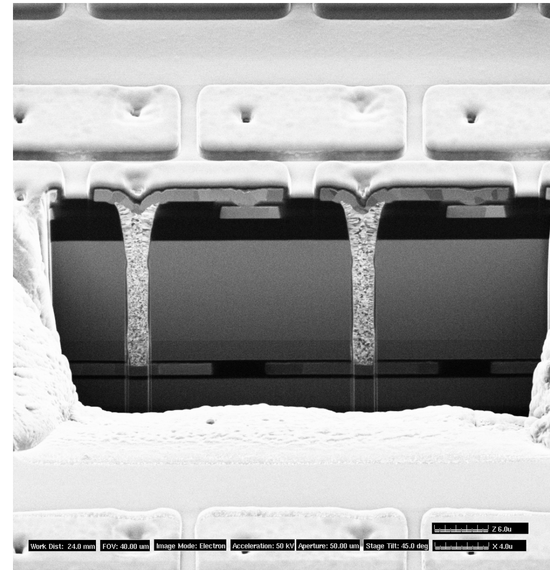
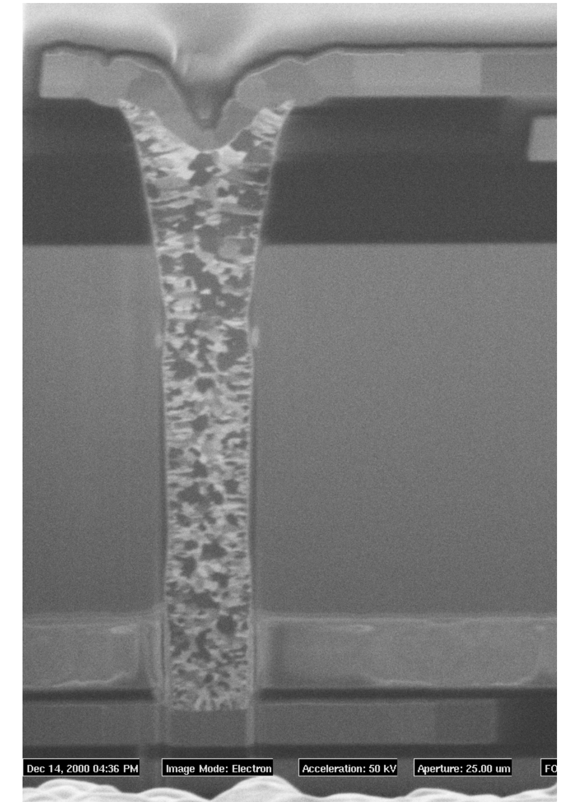
InterChip Via Technology (ICV) / Soldering Concept



Si Trench Etch



Cross section of a vertically integrated test chip structure, showing 2.5 x 2.5 µm² Tungsten-filled interchip vias (FIB)



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thank you for your attention

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