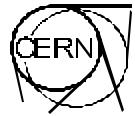


Front-end pixel chips for tracking in ALICE and particle identification at LHCb

Ken Wyllie for the ALICE and LHCb pixel groups

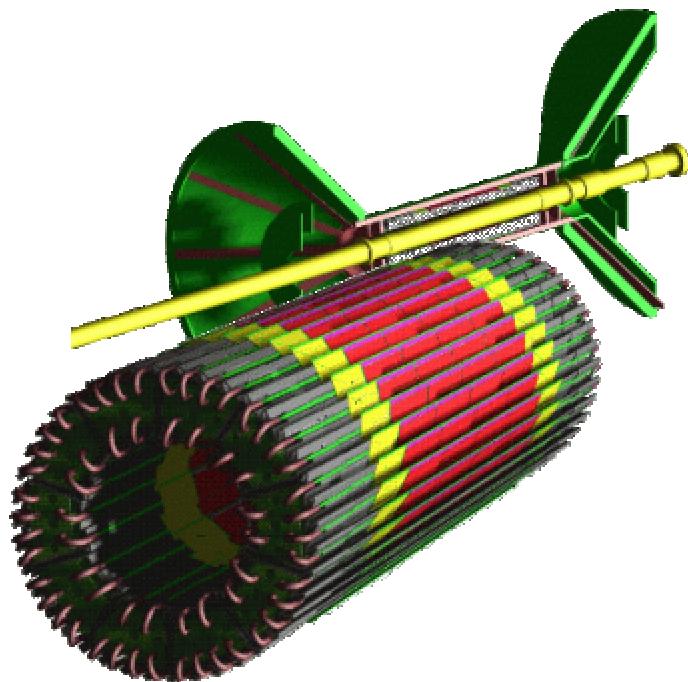
OUTLINE

- The two applications: ALICE and LHCb
- ALICE1LHCb: General chip description
- Pixel cell description
- The two operational modes: ALICE and LHCb
- ALICE1LHCb: Results
- LHCPIX1: Version 2
- LHCPIX1: Results
- Conclusion and future plans

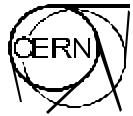


Pixel electronics for tracking in ALICE

See earlier talks by Petra Riedler and Alex Kluge

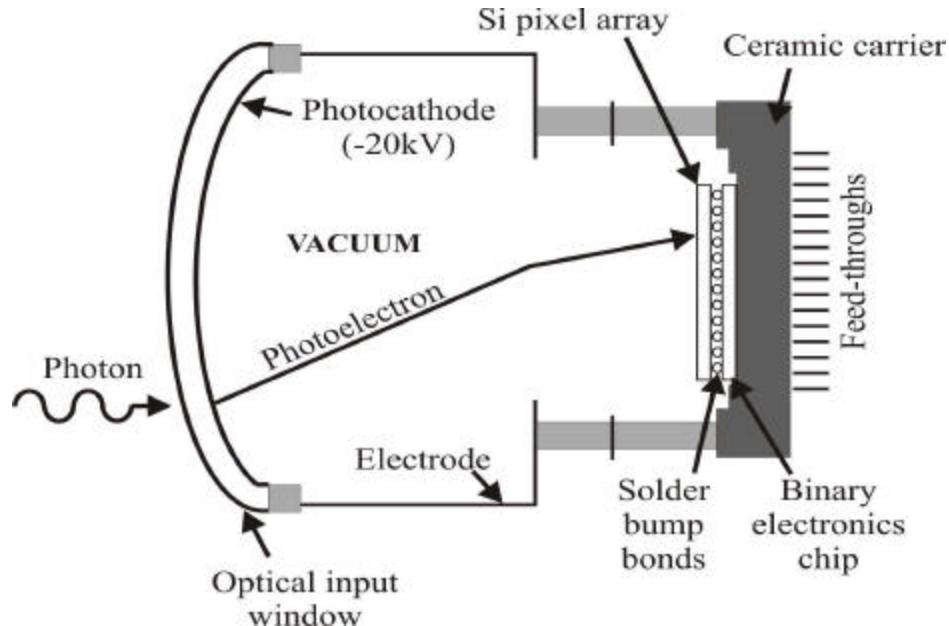


- Spatial resolution of 12mm in r-f => 50um pixel
- Thin sensors (12000 e⁻ signal)
- Data buffers before both Level-1 & Level-2 triggers
- 10MHz readout clock
- Radiation tolerant to ~ 500 krad
- Low power consumption
- Tight mechanical constraints

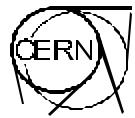


Pixel electronics for particle ID in LHCb

Baseline photo-detector in the LHCb RICH:
Hybrid Photon Detector (HPD)
(See talk on Thursday)

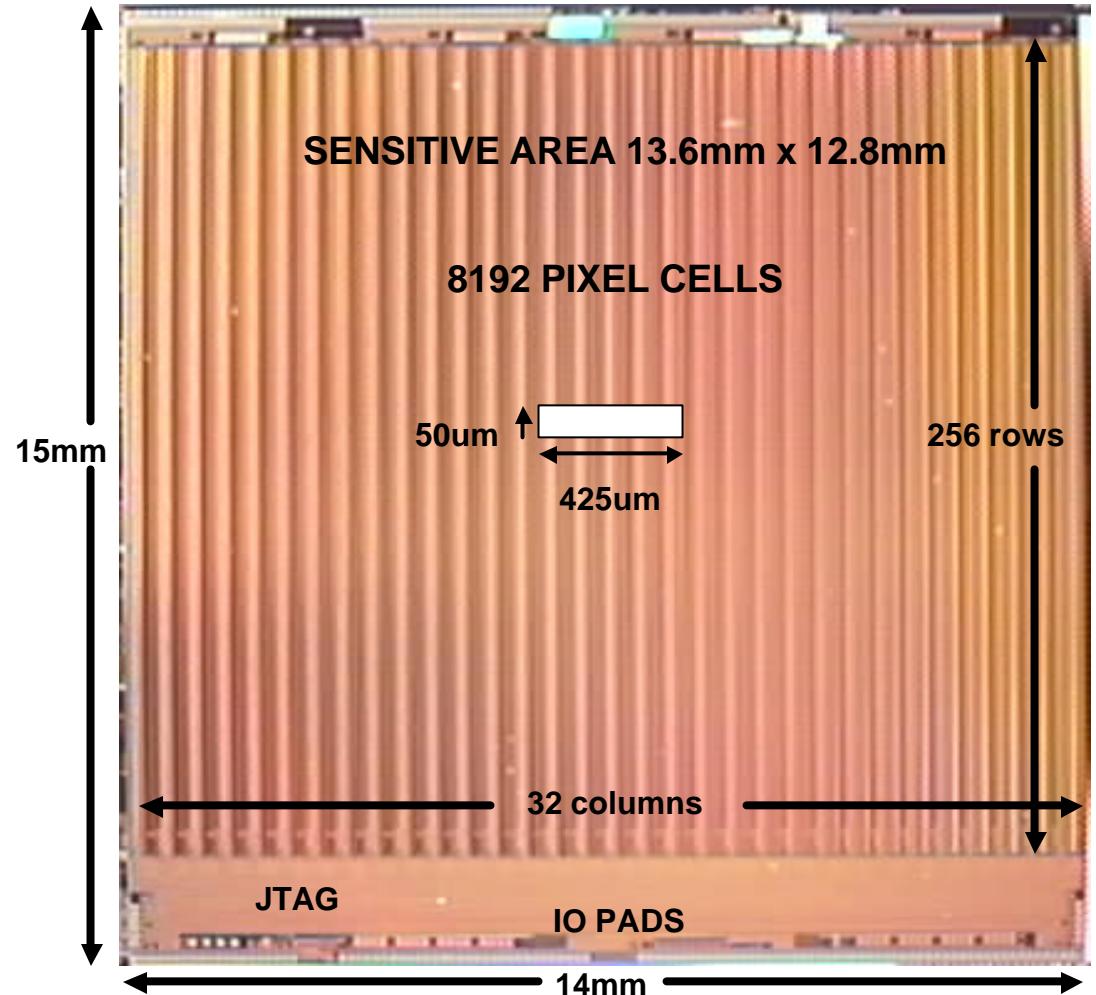


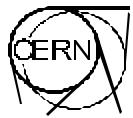
- **5000e⁻ most probable signal (20kV H.T.)**
- **25ns time precision**
- **500mm x 500mm channel size**
- **8% maximum time occupancy**
- **1MHz average Level-0 trigger rate**
- **Buffering of Level-0 triggered events**
- **40MHz readout clock**



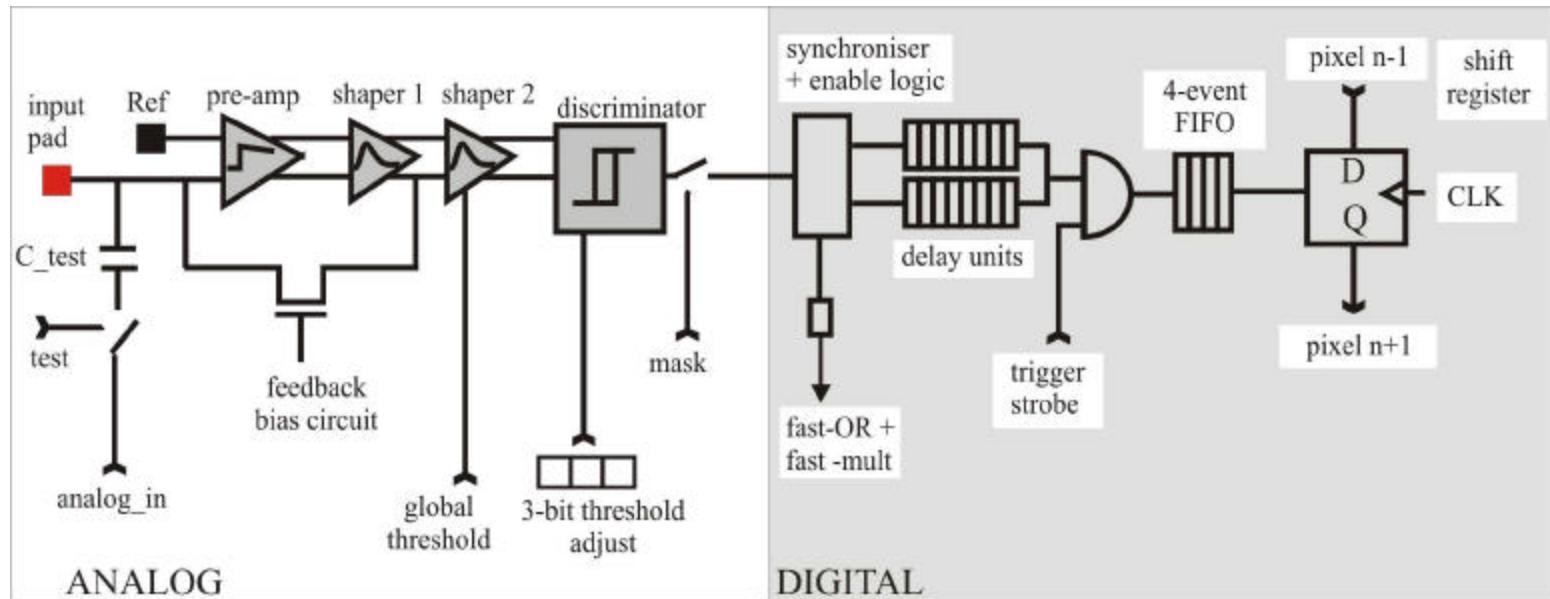
ALICE1LHCB General Chip Description

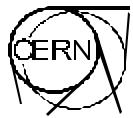
- ◆ Commercial 0.25mm CMOS process
- ◆ 6 metal layers
- ◆ Radiation-tolerant layout
 - Total dose
 - SEU
- ◆ 13 million transistors
- ◆ 800mW total power
- ◆ Current-starved logic
- ◆ Internal bias DACs
- ◆ Configurable via JTAG



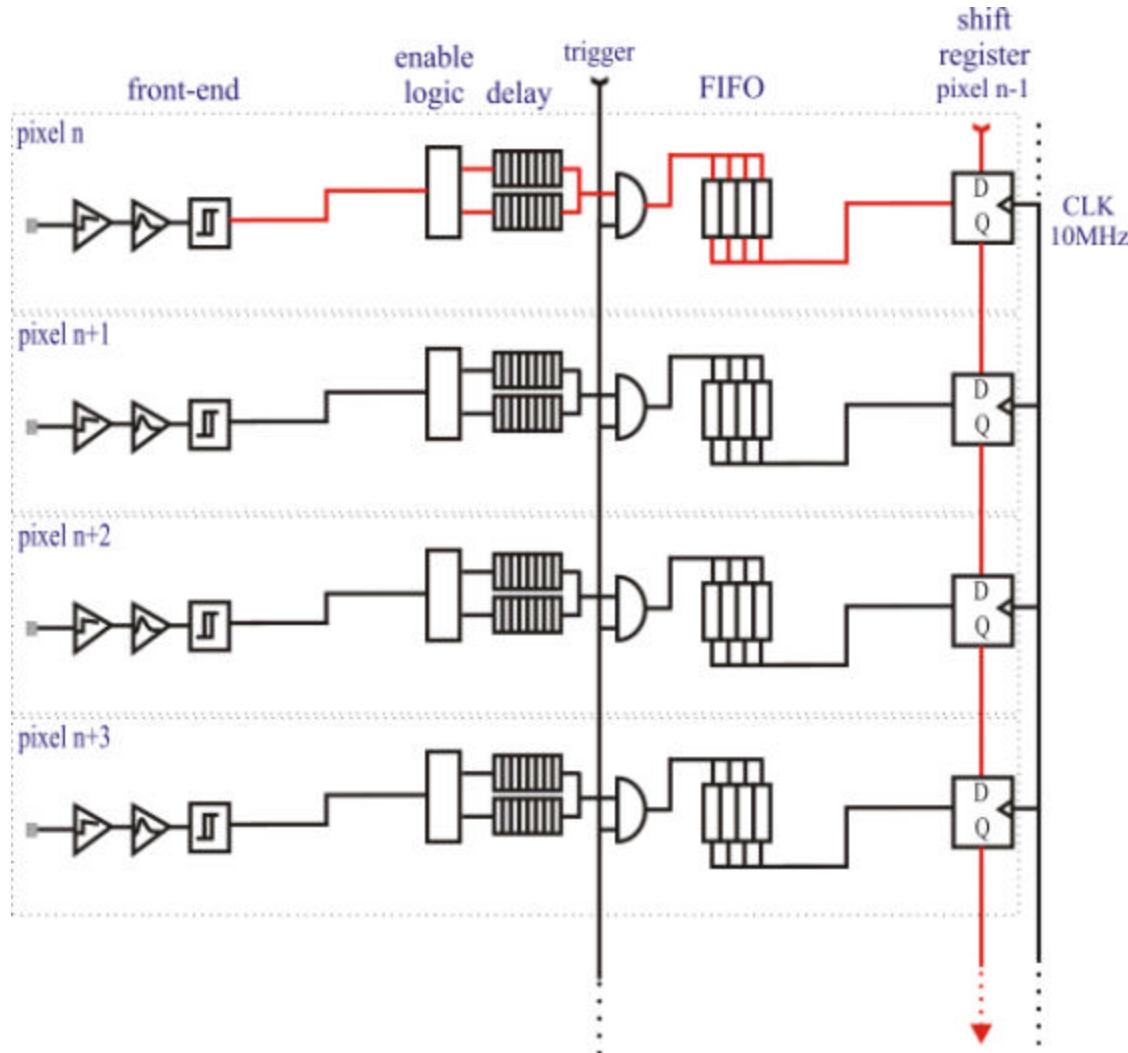


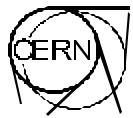
Pixel Cell Description



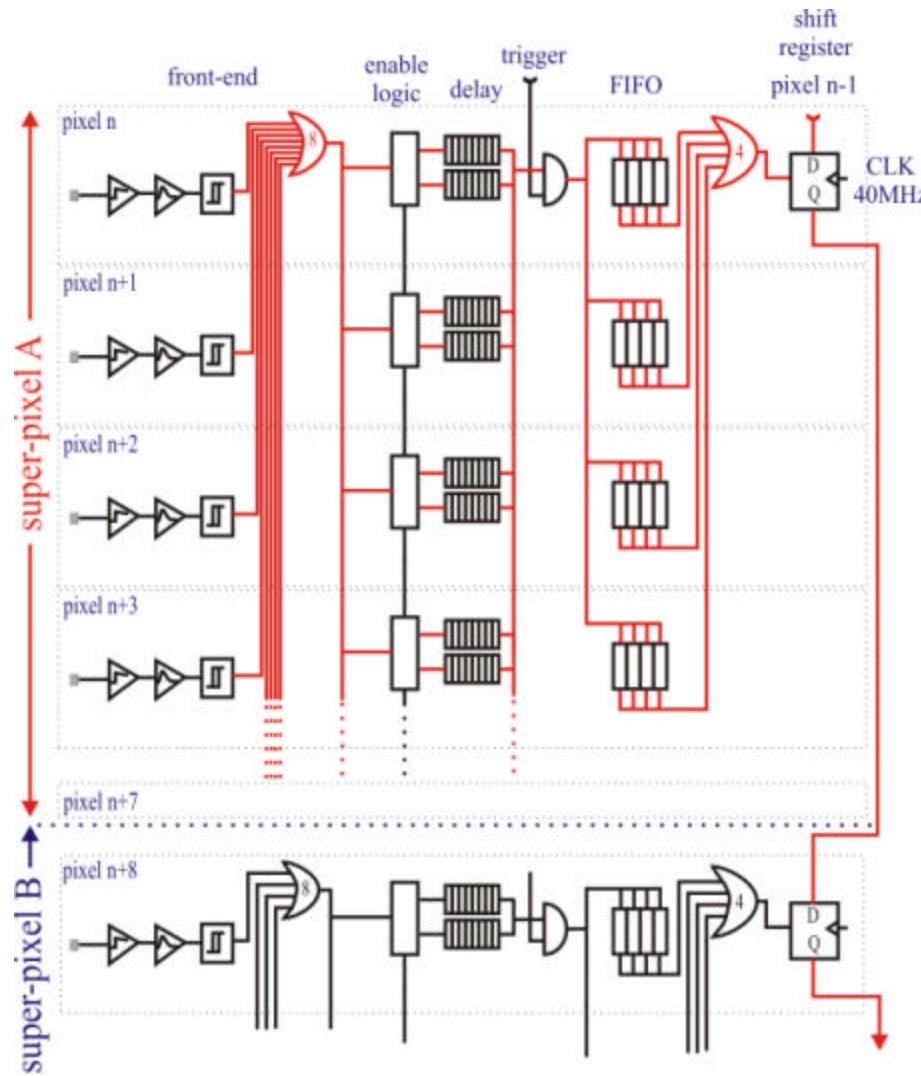


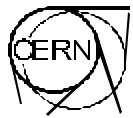
Two modes: ALICE mode



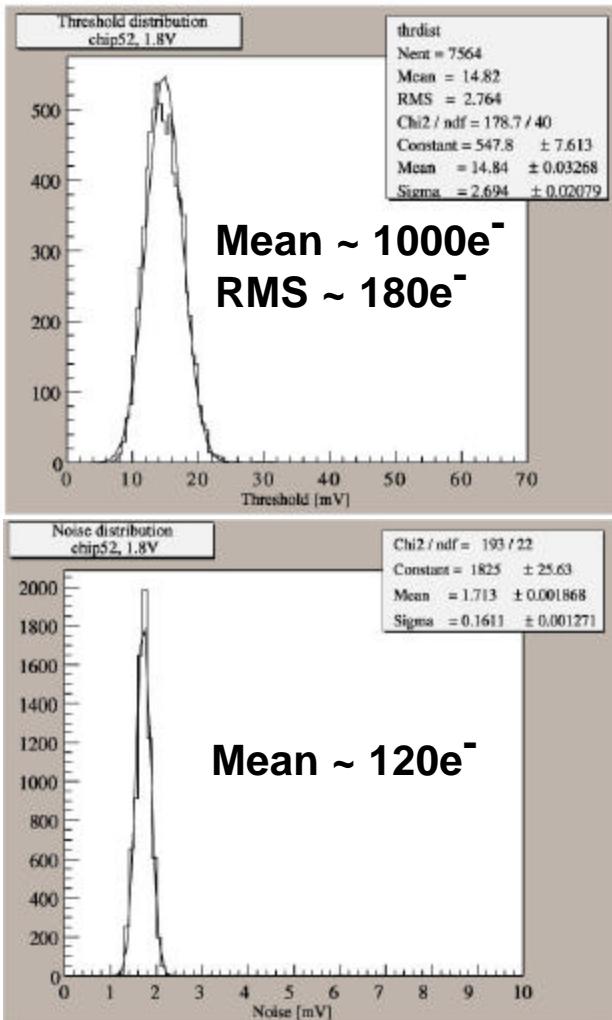


Two modes: LHCb mode

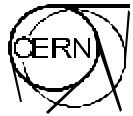




ALICE1LHCb results 1



- ◆ Front-end performance good ☺
 - Minimum threshold ~ 1000 e⁻
 - RMS ~ 180e⁻ (no adjust)
 - Noise ~ 120e⁻
- ◆ Radiation-tolerance OK ☺
 - Total dose > 10Mrad
 - SEU threshold > 6.3 MeVmg⁻¹ cm²
 - ⇒ OK for ALICE & LHCb



ALICE1LHCB results 2

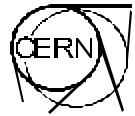
- ◆ Digital performance – full functionality
BUT limited to ~ 15MHz maximum clock frequency
 - OK for ALICE ☺
 - Not OK for LHCB ☹

Biggest problem:

Power supply drops within chip due to

- mechanical constraints,
- limits on metal layer coverage

- ◆ Calibration pulse poorly distributed



LHCPIX1: the sequel

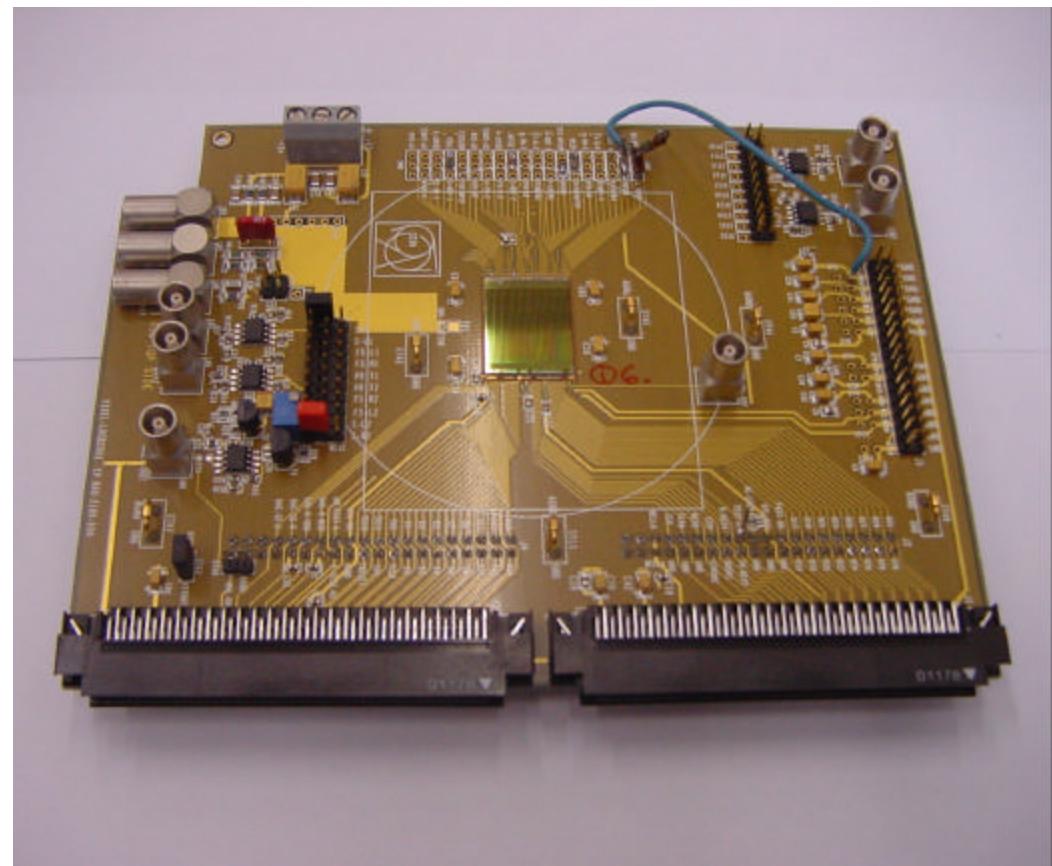
Schematically similar to ALICE1LHCb

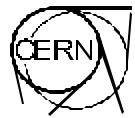
Relaxed mechanical constraints for LHCb:

- Stretch of pixels: 62.5mm x 500mm
(superpixel: 500mm x 500mm)
⇒ more metal for power & decoupling

- Space available above pixel matrix
⇒ power pads & routing,
calibration pulse distribution

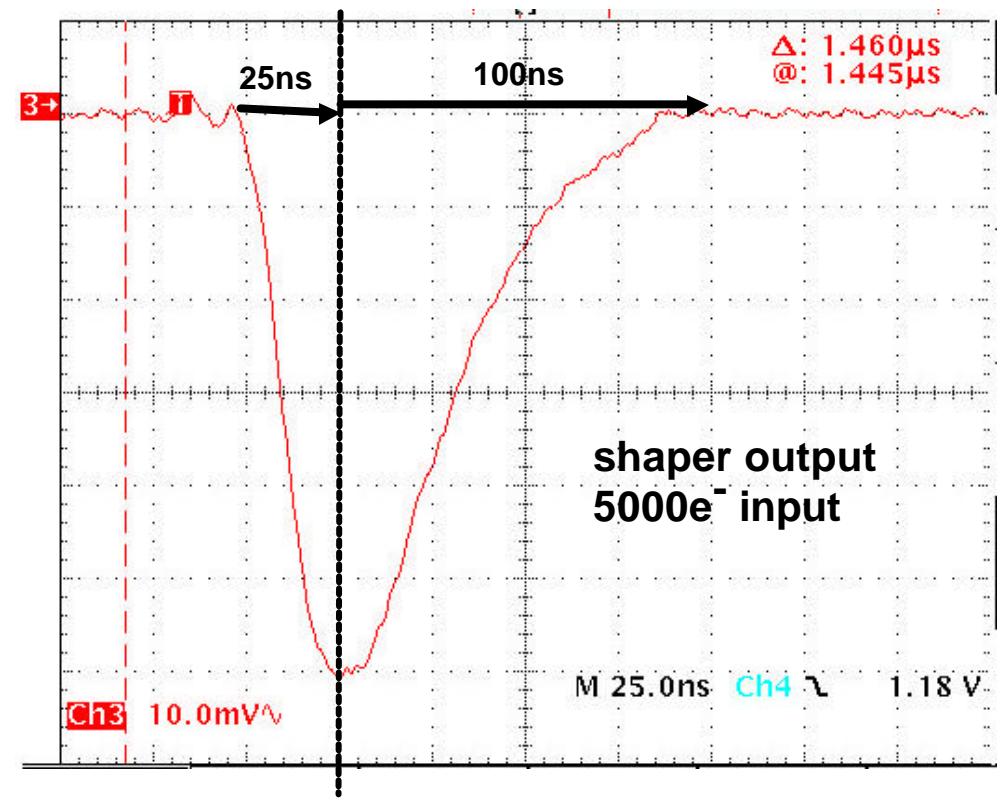
Chip is BIG! 16mm x 21mm

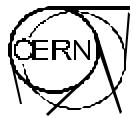




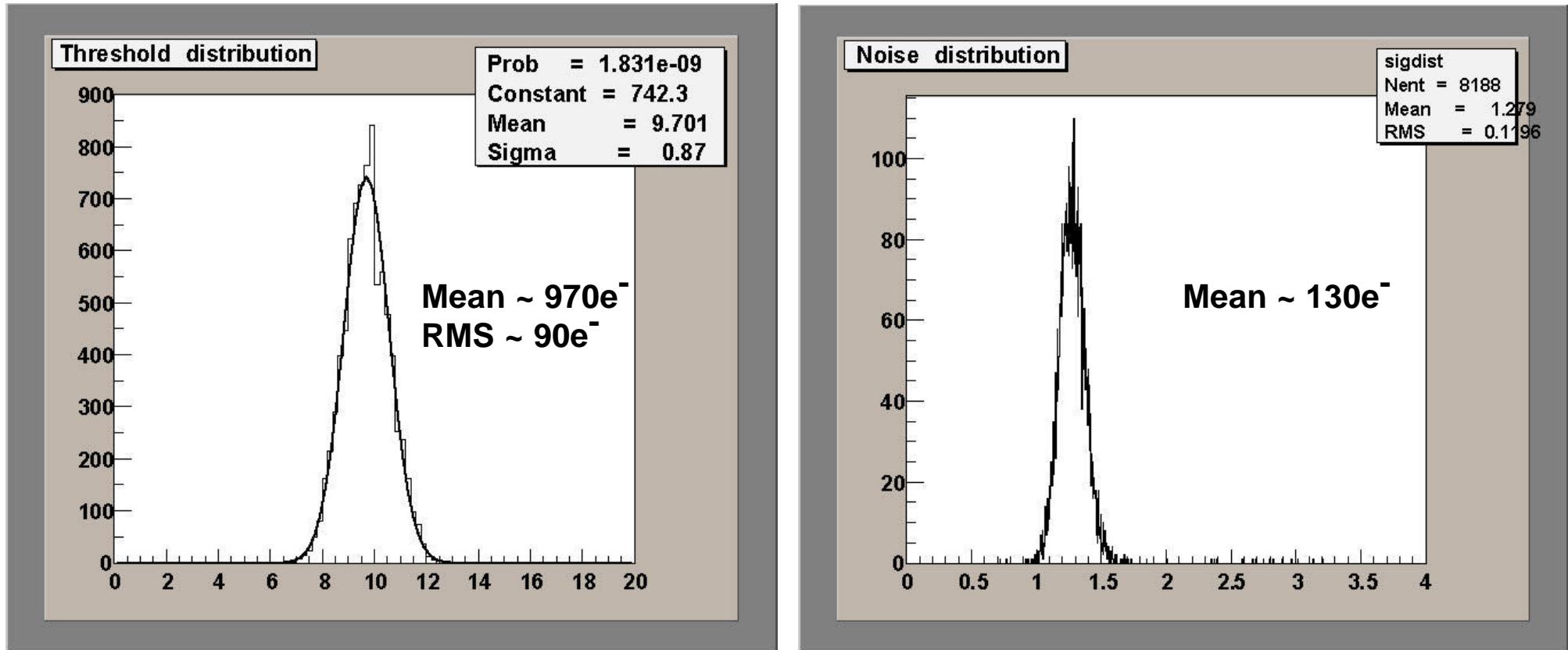
LHCPIX1: results 1

- ◆ Operation @ 40MHz clock freq ☺
- ◆ Power consumption = 1.7W @ 40MHz
- ◆ Analog front-end performance good ☺

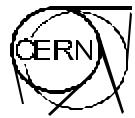




LHCPIX1: results 2



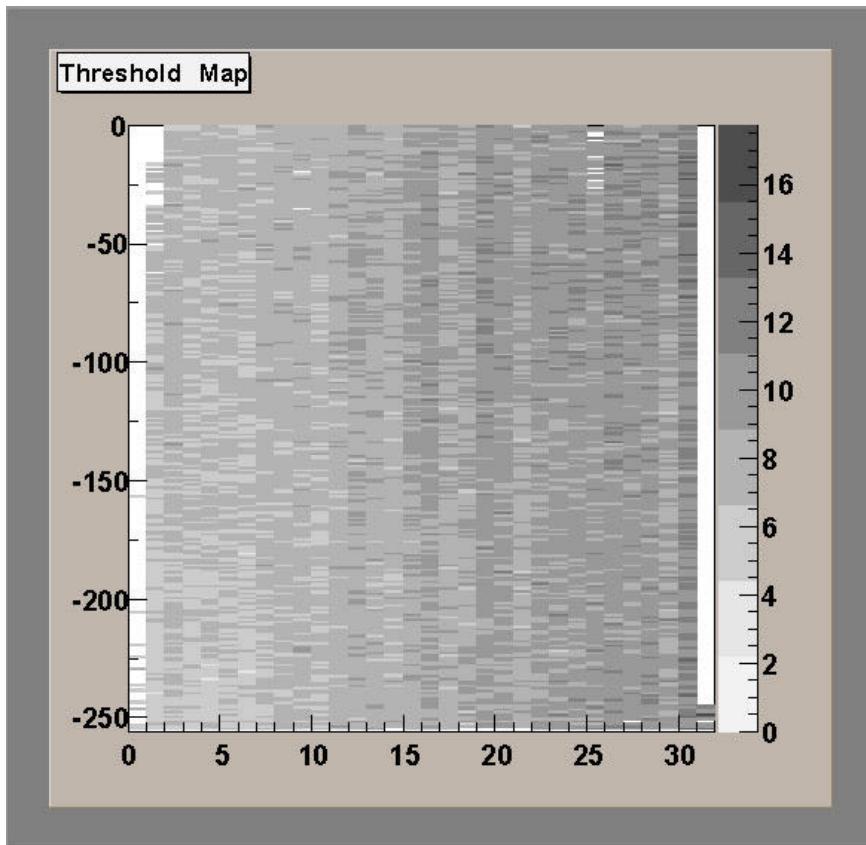
(Without individual threshold adjustment)



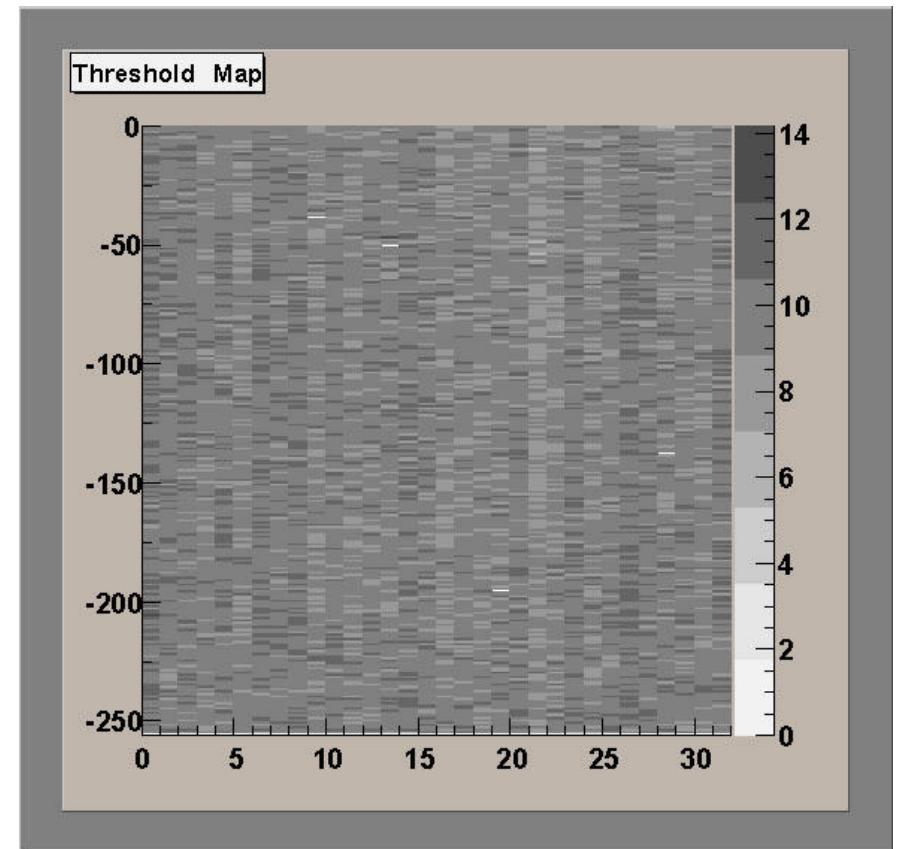
LHCPIX1: results 3

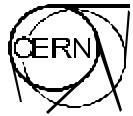
◆ Calibration pulse uniform ☺ – makes life easier!

ALICE1LHCB



LHCPIX1





Conclusion and Future Plans

- ◆ Architecture to meet requirements of ALICE and LHCb
- ◆ Version 1 (ALICE1LHCb):
 - Analog performance good
 - Digital limited in clock frequency
- ◆ Bugs diagnosed (problems of a BIG chip)
- ◆ Version 2 (LHCPIX1) satisfies LHCb specs

- ◆ ALICE1LHCb:
 - continuing tests of ALICE prototype modules
 - ALICE plans to use this chip
 - encapsulation in prototype HPDs
- ◆ LHCPIX1:
 - Bump-bonding planned for start 2003
 - Encapsulation in HPD in spring 2003
- ◆ Production runs for ALICE and LHCb