Flip Chip Hybridization of Pixel Detectors for the ALICE and LHCb Experiments

Jaakko Salonen, Jorma Salmi, and Ilkka Suni
VTT Center for Microelectronics
P.O. Box 1208, Tietotie 3
FIN-02044 Espoo, FINLAND

1 Introduction

VTT has been involved in flip chip technology since 1991. Some of our early activities were described in [1]. Our flip chip process is based on electroplated solder bumps. The solder material used for the work described in this paper is eutectic tin-lead (63 $wt-\%$ tin, 37 $wt-\%$ lead), which has a melting point of $+183^{\circ}C$. The wafers may be optionally thinned after bumping. After dicing, the detector and readout chips are aligned with respect to one another, and soldered together on a high-accuracy flip chip bonder.

In Sections 2, we describe VTT's bumping process in some detail. In Section 3, the chips used for CERN's ALICE and LHCb experiments are described, with an emphasis on the features related to the flip chip process. Section 4 discusses the post-bumping process steps. Section 5 outlines the considerations that will have to be taken into account, when designing a detector/readout chip pair for flip chip assembly. In Section 6 some test results on CERN's hybridized detectors are presented. Finally, a summary is given in Section 7.

2 Solder Flip Chip Process

In VTT's flip chip process, the bonding (soldering) is done without fluxes. To be able to do this successfully, some solder is needed on the pads of both parts to be bonded. This means that both the detector wafers and the readout wafers will go through more or less the same process. The main difference between the sides is that most of the solder volume (the actual bump) is deposited on one side, while the corresponding pad on the opposite side is coated only with a thin layer of solder. An overall process flow is shown in Fig. 1.

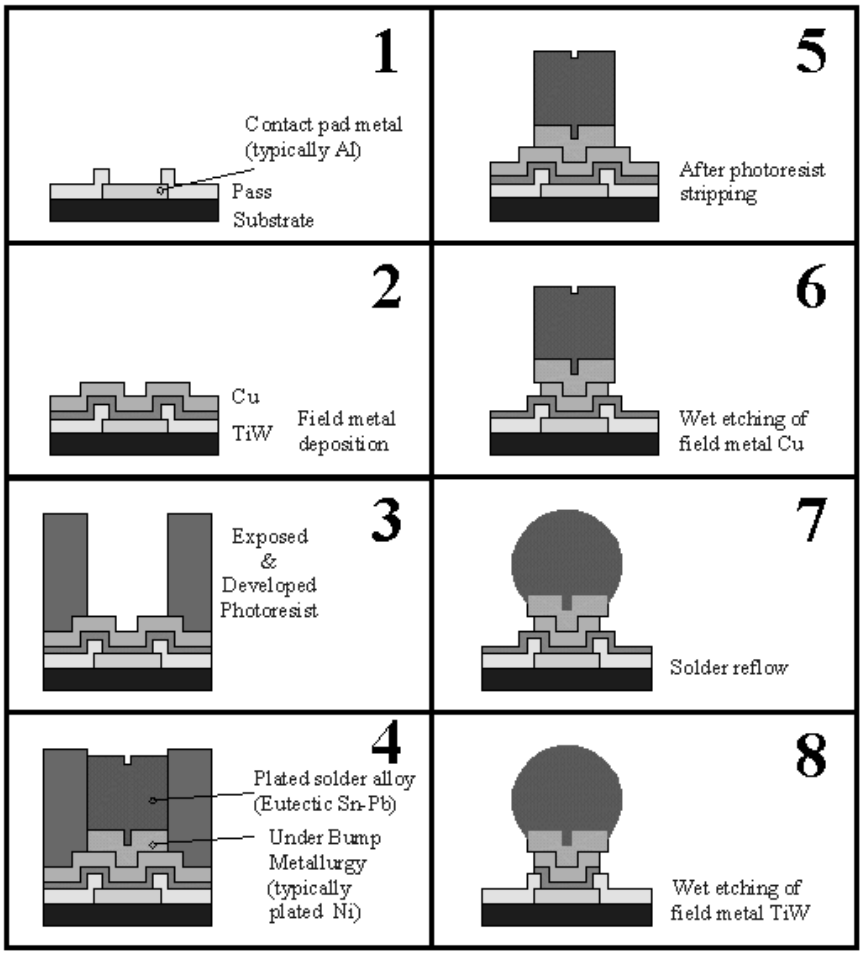

Figure 1: Overall process flow for VTT's bumping process.

The detector and readout wafers third-party come from third-party silicon foundries. VTT is able to process 100-mm (4"), 125-mm (5"), 150-mm (6"), and 200-mm (8") wafers. The wafers must have a passivation layer on them, with openings at the desired bump locations. The size of the passivation opening is dependent on the chosen bump size, as it is required that the bottom of the bump will cover the passivation opening with an appropriate safety margin for mask alignment and bump process variations. The size of the bumps may be limited by the desired pitch, as well as other design considerations such as stray capacitance. The bumping process is compatible with the bare aluminum pads that are used for wire bonding to connect the assembled detector to the outside world.

A blanket metallization is needed on the wafer to act as the cathode in the electroplating process. VTT's process uses a 38 nm thick Ti-W layer in combination with

675 nm of Cu, deposited by sputtering, before which a light sputter etching step is carried out to remove any native oxide from the aluminum pads. The Ti-W is an adhesion layer and a diffusion barrier between the aluminum and copper. Additionally, the Ti-W will protect the wire bonding pads during solder reflow. The copper layer is the cathode.

The electroplating is done through a suitably patterned thick photoresist in order to get solder only at the desired locations. For the CERN readout wafers, we use an 18.6-μm thick positive photoresist, while for the detector wafers a 7-μm thick photoresist is used. Depending on the wafer size, either a Suss MicroTec MA6 or a MA200CC mask aligner is used for the exposure. A solderable metal pad which is thick enough to be able to withstand the bonding step and any other heat treatments is required underneath the bumps. We use 3 μm of electroplated Ni for this purpose. 2 μm and 15 μm of solder are plated on the Ni pads on the detector and readout sides, respectively. The plating system is of our own design, in which special care has been taken to ensure that all parts of the wafer see an equal average electrolyte flow, to achieve a good uniformity across the wafer. RBS (Rutherford Backscattering Spectroscopy) is used to monitor the composition of the plated solder.

In the post-deposition reflow step, any voids as well as any oxides can be removed from the bumps, and they will also assume the characteristic spherical shape. We have done this in a glycerol bath, doped with zinc and ammonium chlorides as reducing agents, and heated to $+200^{\circ}C$.

The sputtered Cu layer is etched away before the reflow step, while the Ti-W layer is etched after it in order to protect the aluminum wire bonding pads during reflow. Wet etching is used for both metals. If the wafers have bare aluminum metallization on their back sides, an identical sputtered Ti-W/Cu layer is used on the back side of the wafers to protect the aluminum during bumping. These metals will then be removed simultaneously from both the front and back sides of the wafers.

3 CERN ALICE and LHCb Chips

The readout wafers are manufactured by IBM on a 0.25-μm CMOS process. Silicon wafers with a diameter of 200 mm and a nominal thickness of 750μm, or thinned down to 300 μm by the manufacturer, are used. The readout chip size is 13.74 mm x 15.89 mm. The wafers have a passivation layer of oxynitride with thickness of about 2 μm. The bumps are contacted with the underlying Al layer through octagonal vias in the passivation. The via diameter (side-to-side) is 24 μm. The layout has also wire bonding pads with bare Al, where contacting the bonded assemblies to the outside world is done later on. A majority of the wire bonding pads have been probed before bumping to map KGD's. The bump pad shape is octagonal with a diameter (side-to-side) of 29 μm, which again takes into account the mask alignment accuracy and

the underetching of the field metal layers.

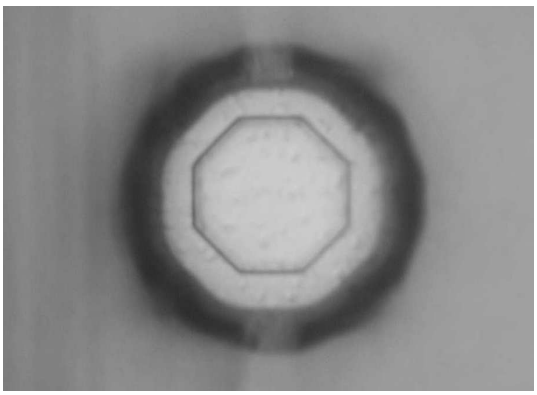

Figure 2: Microscope view of a bump site after exposure & development of thick photoresist on an ALICE readout chip. The diameters (distance between parallel sides) are 24 and 29 μm for the passivation opening and the bump mask opening, respectively.

After the photoresist has been stripped away, the field metal Cu is first wet etched, the solder layer is reflowed, and the Ti-W finally wet etched. The resulting bump foot diameter is 26 μm.

The solder volume for a single bump is $1.52{\cdot}10^{-8}$ m^3, the bump height (including the Ni layer) is 28 μm , and the solder bump diameter is 32.1 μm.

The detector chips come in two different sizes, 'singles' and 'ladders'. The chip sizes for single and ladder type detectors are 14.69 mm x 13.89 mm and 70.69 mm x 13.89 mm, respectively. A single detector chip has an array of 32 columns by 256 rows on a pitch of 425 μm in the x-direction and 50 μm in the y-direction. Each of the resulting 8,192 detector pixels is contacted with the readout chip using equal number of bumps on the readout side. The ladder detector has 5 fields of 32x256 pixel arrays, and is read with five separate readout chips bonded on one detector. The readout chip has an array of 32x256 pixels matching with detector layout. The nominal detector-to-readout chip gap for the flip chip bonded assembly is 20 μm.

The detector wafers are manufactured by Canberra on $\langle 111 \rangle$ Si wafers, polished on both sides, with a diameter of 125 mmm and a thickness of 200 μm or 300 μm. The front side to be bumped has 2-μm thick polyimide passivation. The bump pads are contacted with the underlaying Al layer through octagonal vias in the polyimide. The via diameter (side-to-side) is 24 μm. The back sides of the wafers have unpatterned (ALICE version) or patterned (LHCb version) Al contact metal layer.

The heating of the substrate during the sputtering of the Ti-W/Cu stack results in polyimide surface deformation due to a thermal mismatch between the polyimide

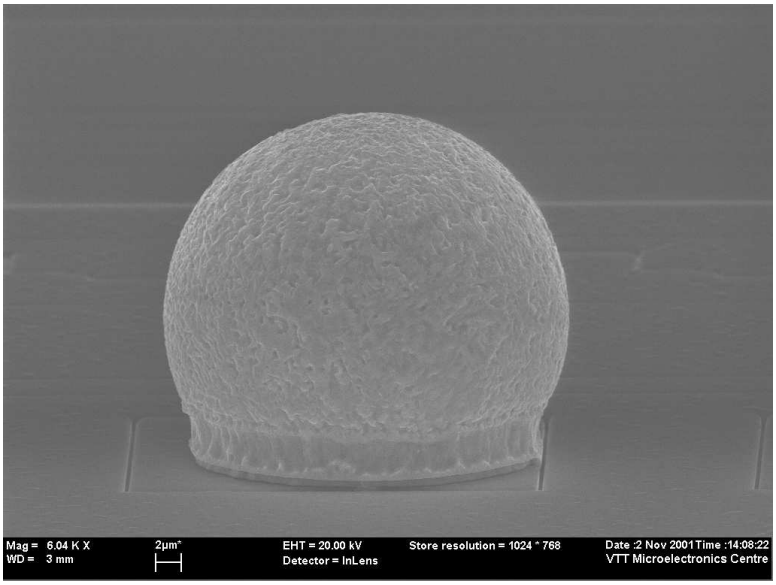

Figure 3: SEM view of a reflowed solder bump on ALICE readout chip after etching of field metals.

and the field metal stack. This effect can be avoided by using a low sputtering power, and by dividing the deposition into multiple steps with cooling periods in between.

The bump pad shape is octagonal with a diameter (side-to-side) of 29 μm, which takes into account the mask alignment accuracy, and the underetching of the field metal layers. The resulting post-process bump pad diameter is again 26 μm, which makes the bump structure symmetrical on both sides.

4 Thinning, Dicing, and Flip Chip Bonding

To minimize the interaction of the bulk Si of the readout ASIC with the radiation to be monitored, the non-active bulk Si may be removed by thinning the readout wafers. To maintain a high yield in the wafer bumping process it is better to do the wafer thinning after the bumping process. In this way, the risks involved in handling thin and fragile wafers can be minimized.

A laminated polyolefin tape with a UV-curable acrylic adhesive is used to planarize and protect the bumped wafer front side. The back-grinding is done on a Strasbaugh 7AF Intelligent Grinder. The grinding leaves a defect layer with a thickness of a few microns, which is removed by wet etching to improve the mechanical strength of the wafer. The wafer thickness can be controlled to within 10 μm, and the total thickness variation over a wafer is less than 5 μm. 200-mm wafers can be thinned down to 150

μm.

A photoresist layer is applied to protect the wafer surfaces during dicing, which is done on a Disco DFD651 saw. A UV-curable dicing tape is used to ease the picking up of large and thin chips. Because of the different crystal orientations, different blades and dicing parameters are used for the readout and detector wafers. A poor chip edge quality increases detector leakage currents. The photoresist used for surface protection is stripped away with solvents.

The flip chip bonding is performed on a Suss MicroTec FC150 flip chip bonder. This machine can handle chip sizes up to 50 mm x 50 mm, and the post-bonding alignment accuracy is less than 3 μm with the so-called thermocompression bonding arm, which has been used for the present work. Our flip chip bonder also has the so-called laser leveling option, which is used to adjust the parts to be bonded exactly parallel before alignment and bonding. The parts are held by vacuum on IR-transparent (halogen lamps are used for heating) silicon carbide tools in the flip chip bonder.

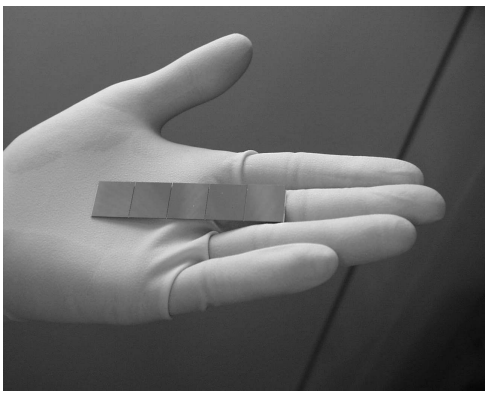

Figure 4: Assembled ALICE 'ladder'detector comprising five readout chips on a single detector chip.

5 Design Considerations for Flip Chip Assembly

Virtually all ASIC's today are made using steppers. Steppers have a very accurate alignment/registration within a field of exposure; however, the registration between fields is not necessarily very accurate. This can give rise to problems, if a 1:1 contact aligner is used to expose the photoresist used for bumping. If the foundry is contacted in advance and told that the field-to-field registration is important, the problem can usually be minimized.

A positive photoresist is used to define the areas for electroplating. This means that a dark-field photomask will be used for this step. For the bump size used in the work, it is impossible to align a dark-field bump mask directly to the bump sites on a wafer, if no alignment targets are available. During the electroplating step, solder will be deposited to all exposed areas, including the alignment targets, which will then be covered with ill-defined chunks of solder. To avoid interference at the bonding step, it is desirable that the actual chips have solder only at the desired bump sites. A practical way around this problem is to have exactly two alignment targets on the mask (with corresponding targets on the wafer). Convenient places for these targets are on the main diagonal, which is parallel to the tangent of the wafer at the main flat/slot, and reasonably close to the edge of the wafer, to enable the theta correction to be made with maximum accuracy.

The Suss MicroTec FC150 flip chip bonder uses laser leveling to adjust the detector chip and the readout exactly parallel before alignment and bonding. This requires three smooth and uniform (unpatterned) areas of at least 50 μm in diameter at three distinct places near the periphery of the parts. The area doesn't need to be polished; the system is able to use, for example, the kind of relatively rough surface that is usually on the unpolished backside of wafers.

The readout wafers are usually probed for KGD's (Known Good Dice) before bumping. Probes leave visible marks on aluminum pads; the exact size and nature of these marks depends on the quality of the probe tips and the planarization of the probes on the probe card. The probe marks and aluminum particles are a risk at the reflow stage, where the thin Ti-W layer is supposed to protect the bare aluminum wire bonding bonding pads. We haven't seen any undue problems because of this on the CERN wafers, which goes to show that it is possible to bump probed wafers succesfully.

Metal layers can affect dicing. Even if the back side of of the detector chip has an unpatterned metallization, it should be patterned at wafer level so that the dicing lanes are clear.

6 Test Results on CERN's ALICE & LHCb Detectors

According to tests carried out at CERN, the latest bonded detectors have typically between 5 and 10 dead pixels (out of 8,192). However, it must be kept in mind that according to CERN's classification readout chips with up to 1 per cent (0 to 82 pixels) are defined as 'good', so some of the dead pixels may be due to yield loss taking place before bumping and flip chip bonding. Figure 5 shows the response of a detector assembled at VTT to radiation from a strontium-90 source.

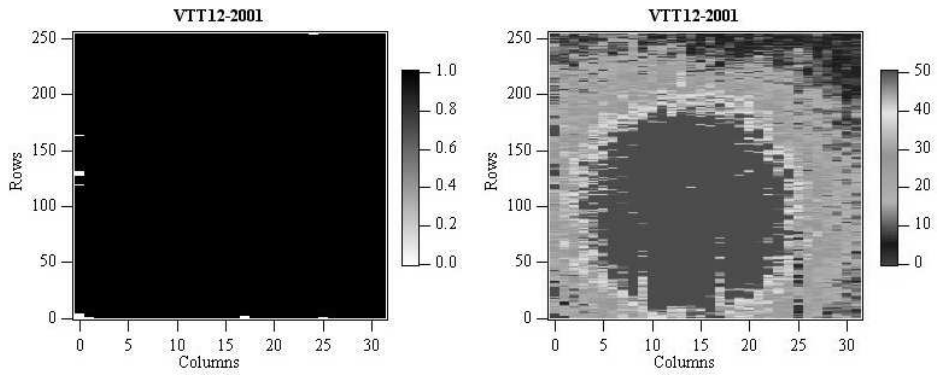

Figure 5: Test results on an early assembled ALICE 'single' detector, irradiated with a strontium-90 source. At left, the scale has been set to a maximum of 1 count to show dead pixels (14 out of 8,192). At right, the scale is set to a maximum of 50 to show the intensity distribution. The columnar imperfections are an artifact of the readout algorithm.

7 Summary

An overview of a flip chip process based on electroplated lead-tin solder bumps was presented. Process-related design considerations for implementing a design using flip chip joining were also described. Detector and readout chips designed at CERN, and bumped and flip chip bonded at VTT, were used as real-world examples of a functional application.

The authors wish to thank Michael Campbell, Petra Riedler, and Ken Wyllie of CERN for providing the test data presented in Section 6. The authors also wish to thank Tommi Riekkinen of VTT for the SEM image and sample preparation.

8 References

[1] J. Salonen & J. Salmi, "Test Chip and Process Design for Evaluating Flip Chip Technology", *Proceedings of the First International Symposium on Flip Chip Technology*, San Jose, California, February 15-18, 1994, pp. 87-93.