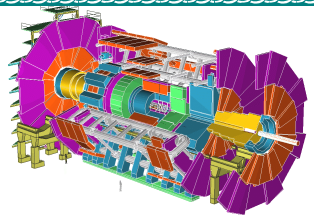
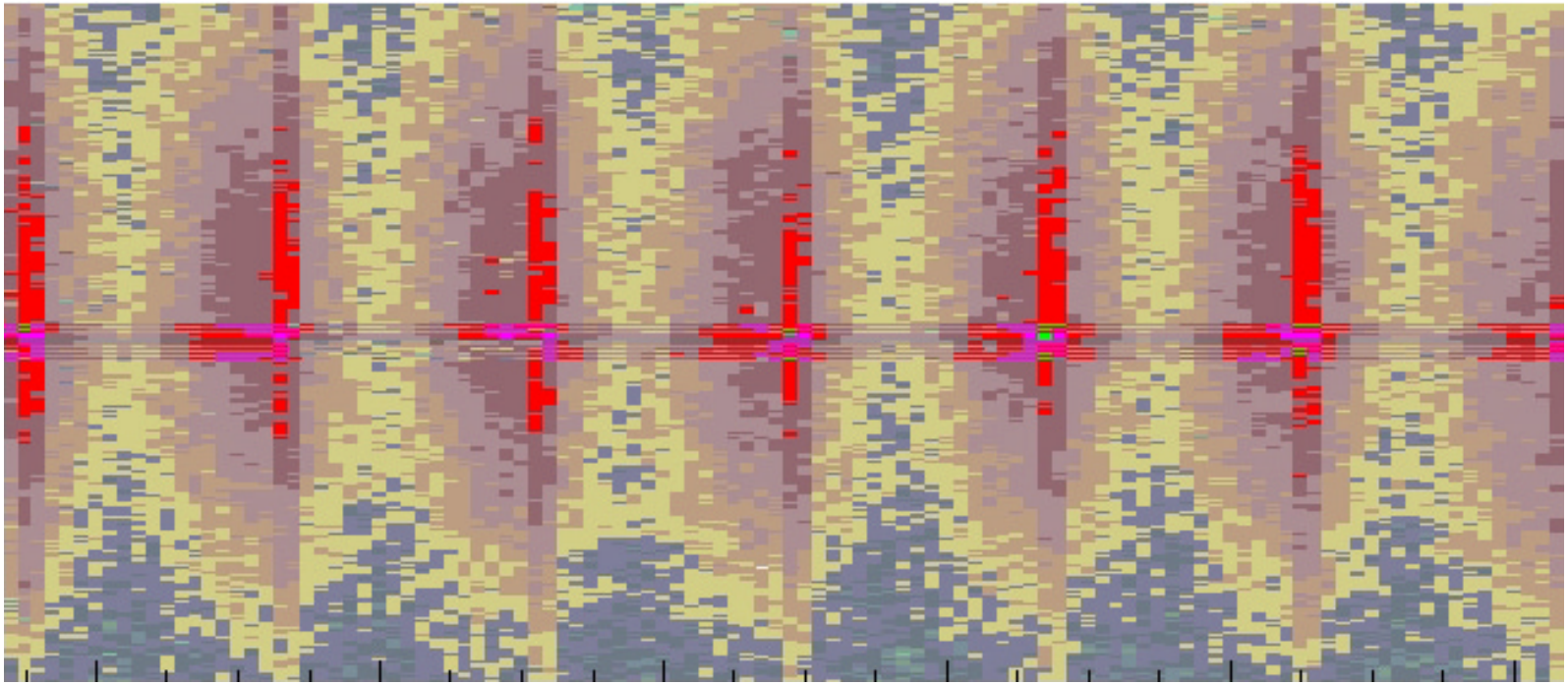


Laboratory Evaluation of the ATLAS Pixel Front End



Pixel 2002, Carmel CA, 10th September 2002

John Richardson
Lawrence Berkeley National Laboratory

Overview

- The TurboPLL Test System
- FE-I1: Studies using Digital Injection
- FE-I1: Threshold and Noise Performance
- FE-I1: Timewalk Evaluation
- FE-I1: Analogue Crosstalk Performance
- FE-I1: Time-Over-Threshold Calibration
- FE-I1: MONLeak ADC Feature
- Analogue Test Chip – Noise Measurements
- Fully Instrumented MCM Experience with FE-I1 and MCC-I1

The TurboPLL Test System

Introduction

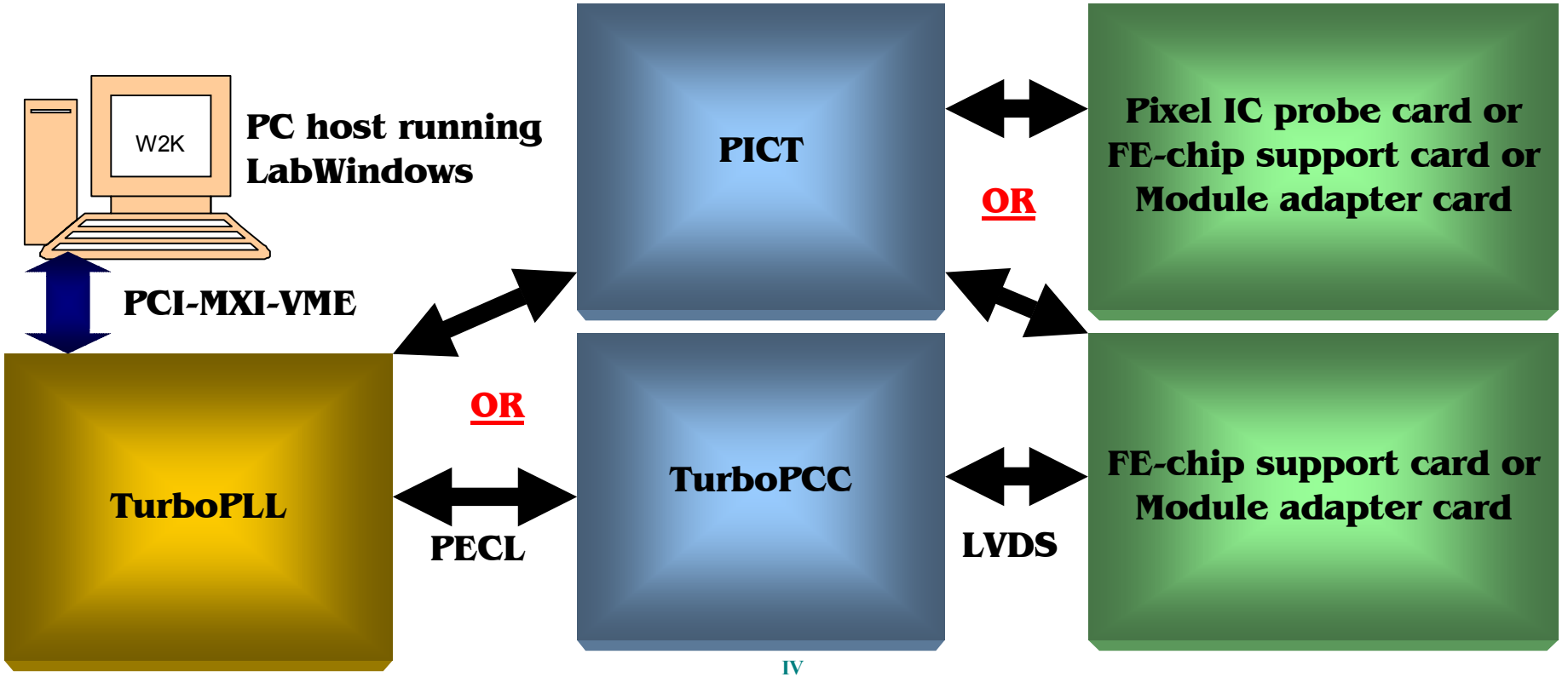
- **The official test system which will be utilised throughout the collaboration is 2nd generation of a system conceived in November '97 and realised in early '98.**
- **The full spectrum of test requirements is provided for by ~the same system e.g.:**
  - **Probe testing of bare electronics wafers (in order to identify 'known good die' prior to dicing) and diced, bumped chips prior to flip-chip.**
  - **Performing detailed analogue evaluations (threshold, ENC, timewalk, crosstalk TOT calibration etc.) of bump-bonded assemblies (single-chip and MCM) in the laboratory.**
  - **Being capable of performing comprehensive tests at intermediate steps in module construction e.g. probing bare modules prior to flex attachment.**
  - **Providing the readout system for testing single-chip assemblies and full-size modules in beam tests (e.g. SPS H8 at CERN).**

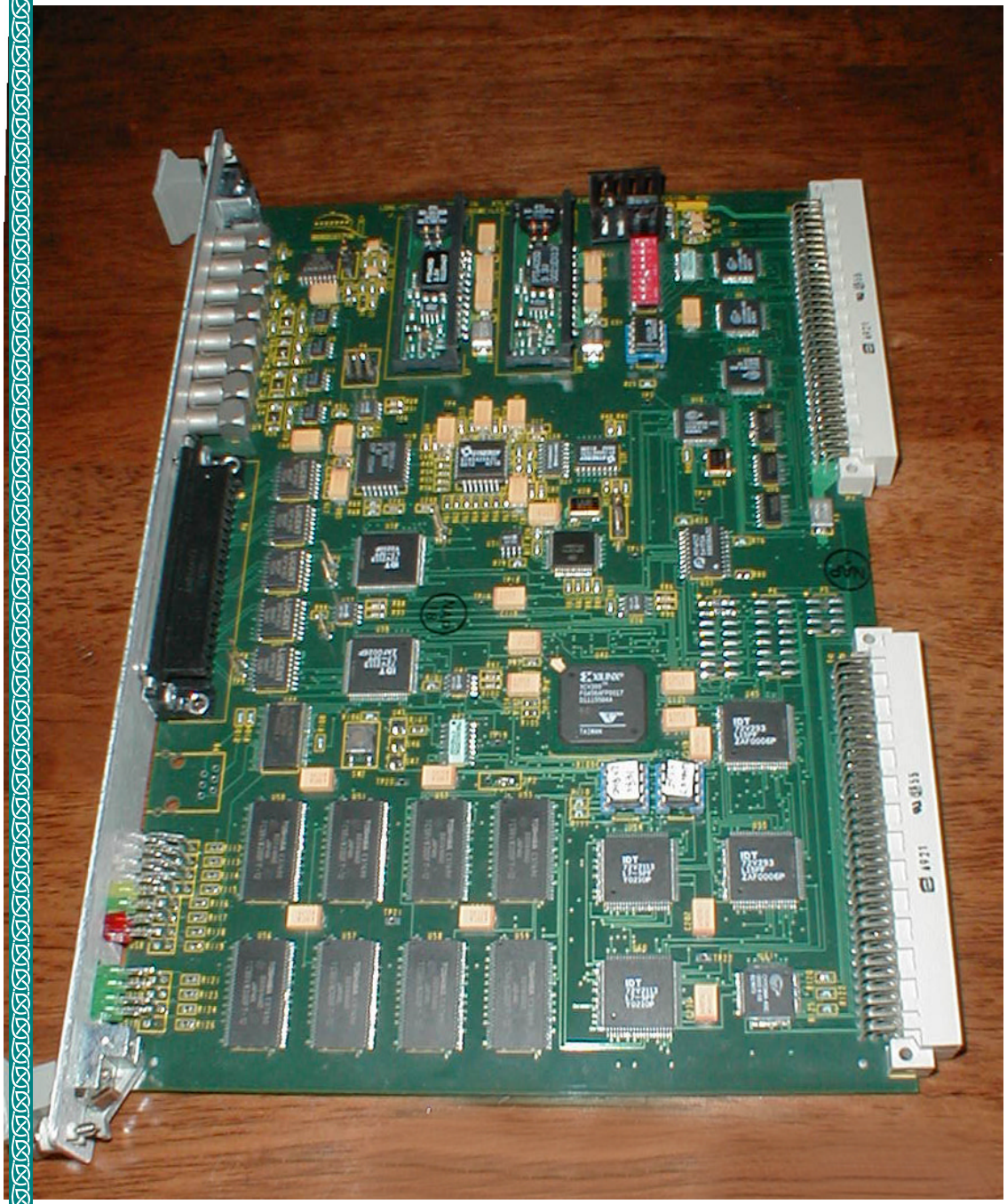
This 'fully integrated' approach in which identical hardware and software is used at all evaluation stages has proven extremely beneficial in terms of understanding what to expect from a particular device (in the testbeam environment e.g.), for a given configuration which has been arrived upon through detailed laboratory optimisation.

The TurboPLL Test System

System Architecture

- **Basis is 6U VME board (the 'TurboPLL'). Incorporates large Xilinx FPGA and input/output FIFOs for communication with the host PC.**
- **Pixel Control Card (TurboPCC) provides 2 DACs for setting the calibration pulse hi/lo levels. Also includes delay chips for varying the relative timing of the cal strobe and LV1 trigger and chopper circuitry for external charge injection.**
- **Software package is written in ANSI C in the NI LabWindows for NT environment – provides very useful GUI creation tools along with necessary VME libraries.**





The TurboPLL

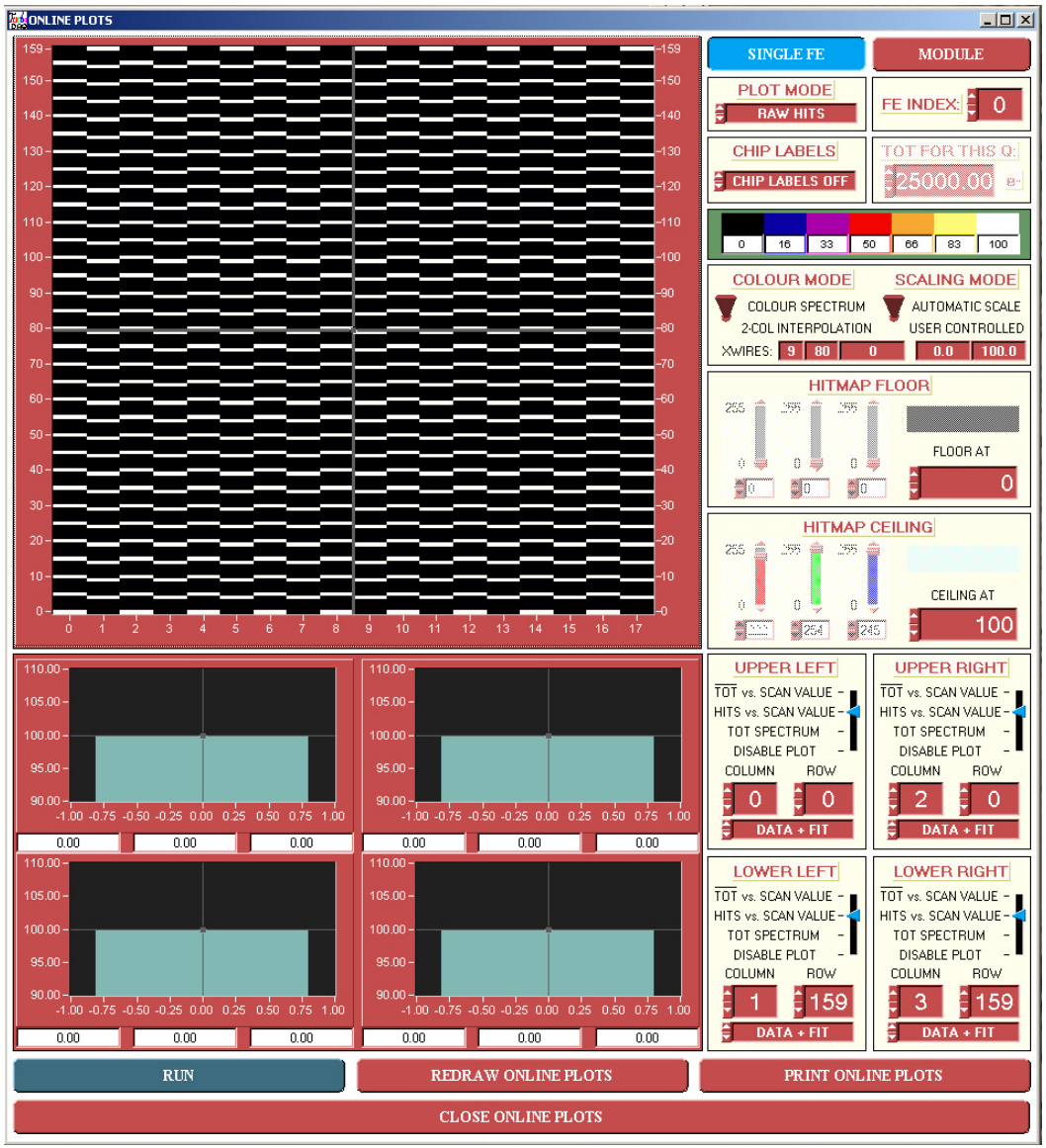
- **Purpose is to create waveforms for configuration of downstream entities (i.e. PCC, MCC, FE-chips) with various protocols. Also issue hit-strobes and triggers. Return data is word-aligned and sent either in raw form to output FIFO or histogrammed on-board.**
- **Level-1s either generated internally (for threshold scanning etc.) or provided externally via a LEMO connection. Fast-OR (hitbus) signal from the FEs may be used as the source of LV1 trigger creation (introducing a programmable delay).**
- **Other LEMO connections allow the TPLL to be controlled via an external 40MHz clock (for testbeam use etc.) along with providing strobe and hitbus monitoring.**

The TurboPLL

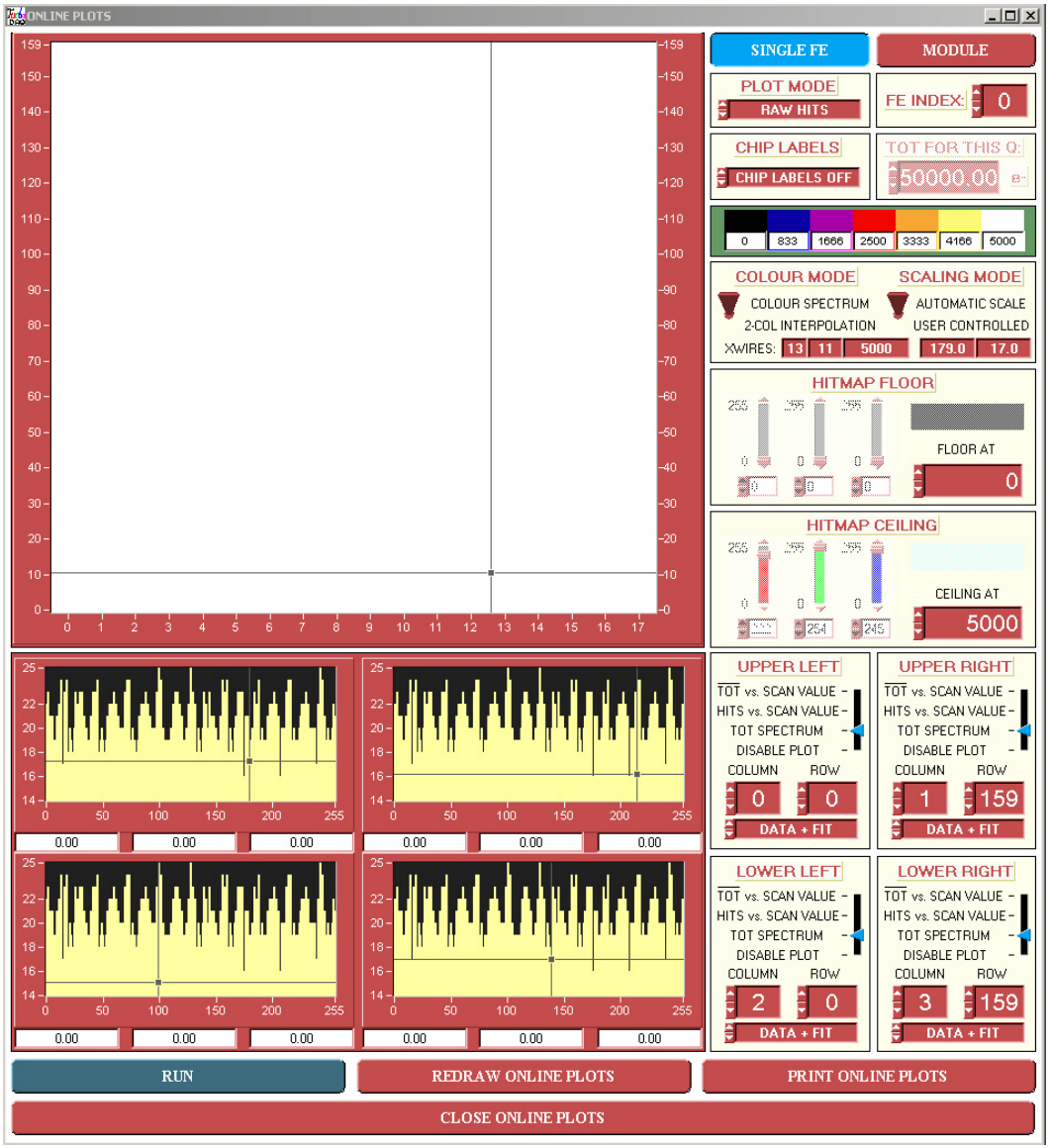
- Expect on-detector electronics to slow with irradiation, therefore desirable to test die at elevated operation frequencies pre-irradiation..
- Can determine how likely they are to meet the specifications when they have been exposed to >50Mrads ionising dose.
- Key feature of TurboPLL part of the test system is a programmable clock generator offering a broad range of module/chip operation frequencies from ~15MHz to 125MHz.
- This necessitated the implementation of two 512k-deep front-end FIFOs which serve to divorce the signal transmission and reception from the FPGA control clock (which always operates at 40MHz).
- TPLL incorporates 16MBytes of on-board SRAM in order that calibration data may be histogrammed for an entire module at once (with up to 256 scan points).

FEI1: Studies using Digital Injection

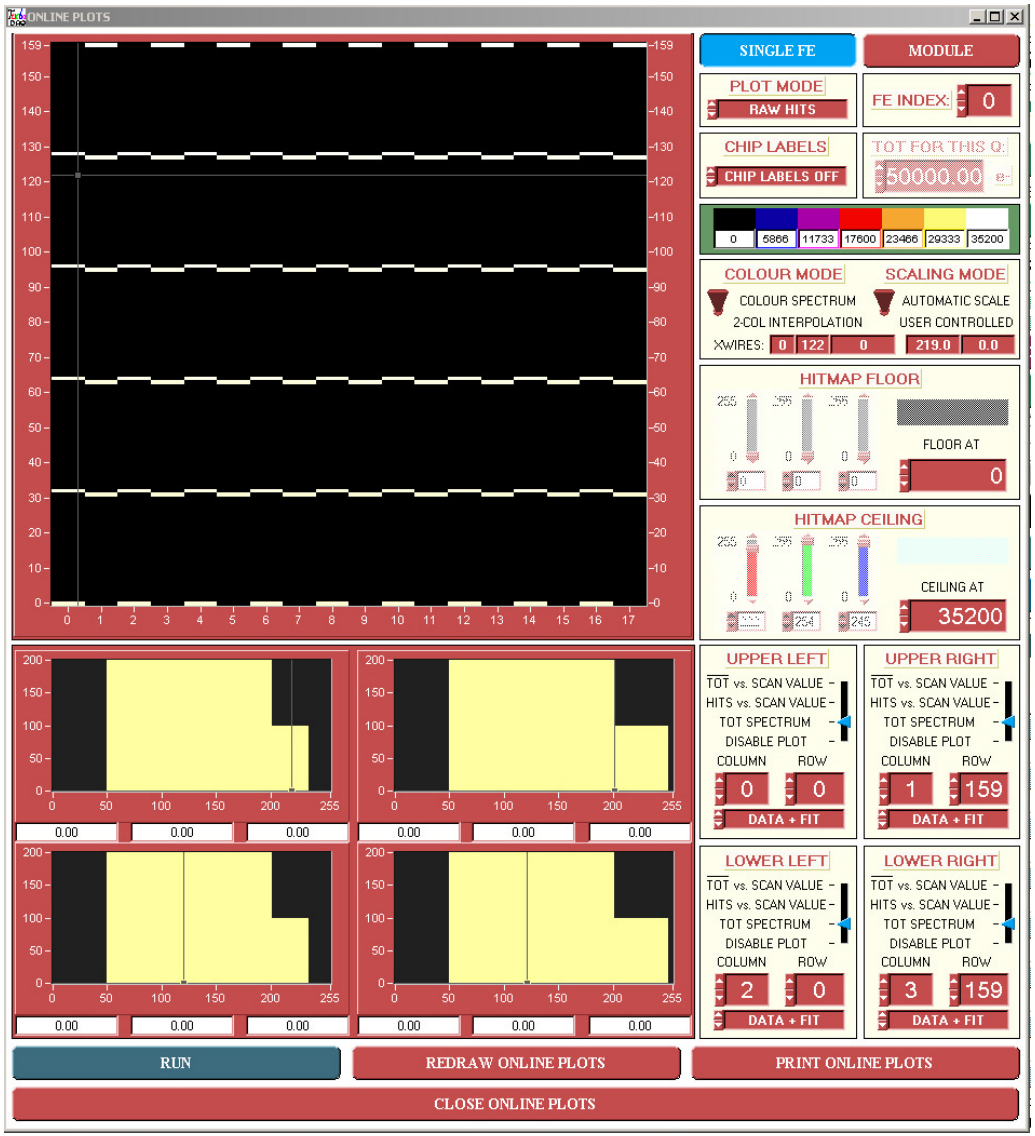
- **FE-I1 readout architecture provides ability to mimic hit creation using a digital strobe.**
- **Provides a means of comprehensive testing of the digital readout logic without playing 'analogical games'.**
- **Important test is to simultaneously inject a digital hit into every 5th pixel. This results in 64 hits per column-pair (since 160 rows per column) and thus utilises every end-of-column buffer location.**
- **This online plot shows the return data from FE-I1 in which such an test is repeated 100 times and the whole readout logic is used to strobe the resultant data off the chip. All of the hits are returned perfectly. Readout logic works to ~86MHz clock speed.**



- **In digital inject mode the effective time-over-threshold (TOT) is derived from the width of the strobe used to generate the 'hits'**
- **Optionally FE-I1 may be operated in a mode where the 8-bit leading-edge timestamp information is selected for the 'TOT' hit field in the output serial data stream.**
- **In this example 100-event digital scan has been looped through the array 50 times (to accumulate stats) and for 4 arbitrary pixels the TOT spectrum option is used to show the distribution of LE values**
- **The expected flat distribution is seen with values from 0 to 255**
- **The structure which is visible is a consequence of the PLL and the Grey generator not being truly asynchronous**

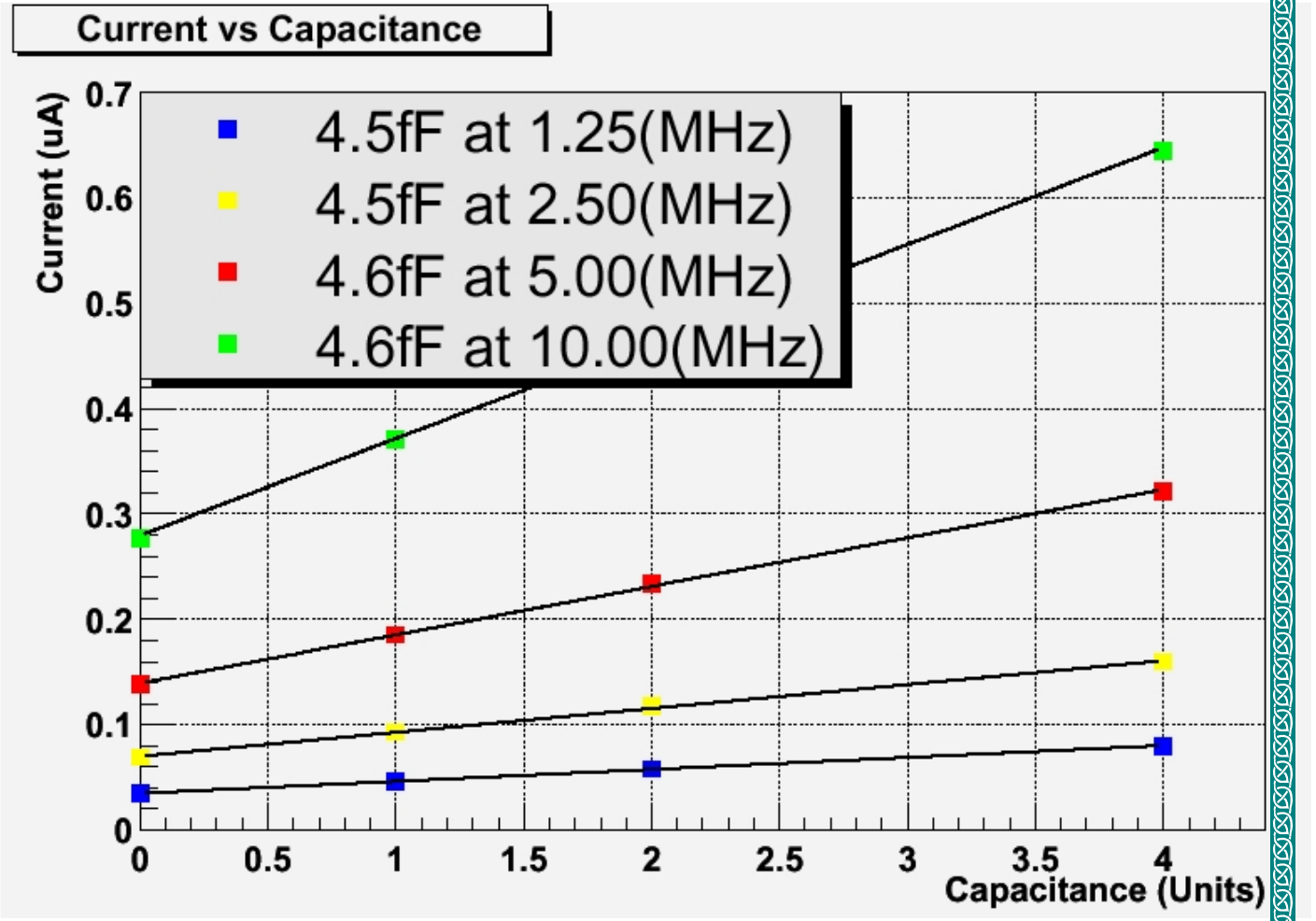


- **Here digital injection is again utilised to verify the 'TOT threshold' operation.**
- **FE-I has two TOT thresholds, one of which can be used as a timewalk correction (hits doubled up in 2 consecutive BCOs); the other may be used to reject hits which have too small a TOT**
- **Strategy here is to scan the strobe duration from 0 to 255 in steps of one and to plot the TOT spectrum**
- **The chosen thresholds are 50 for the minimum TOT before which no hits are seen to come out of the chip; and 200 for the digital timewalk correction below which the occupancy is double**
- **Above this the hits are returned once as expected (as long as there is time to get them into the buffers)**



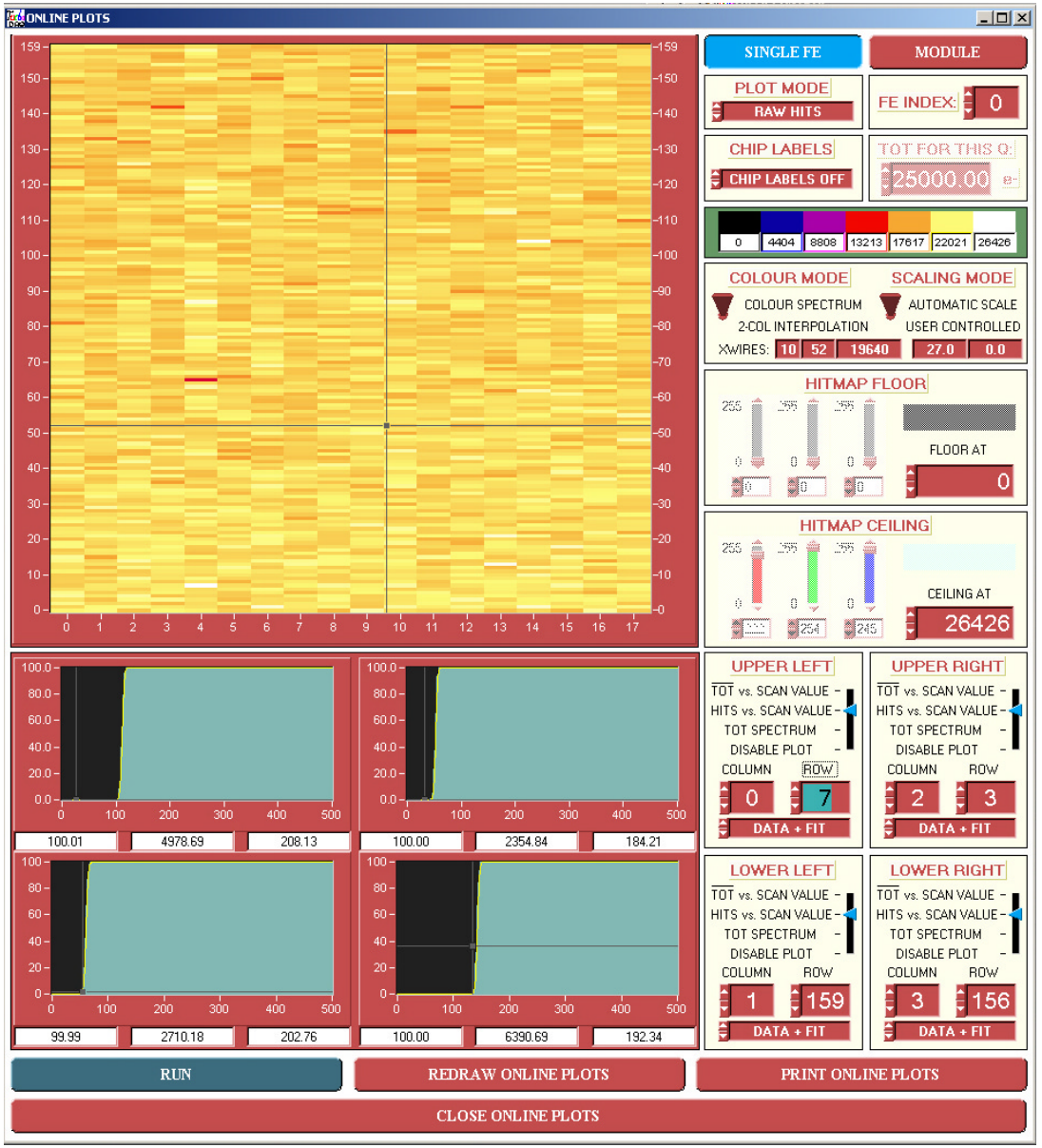
FEI1: Capacitance Measurements

- **Using capacitance arrays & charge pump circuits of FE-I1 the values of C_inj-lo, C_inj-hi and C_feedback are able to be determined simply and accurately.**
- **Can dial-up frequency from XCK/4, XCK/8, XCK/16 or XCK/32 and a number of capacitors from n = 0,1,2 or 4 (of each type), then the measured current gives the capacitance according to: C = dQ/dt . dt/dV = Δ(I/Vf)/Δ(n)**
- **Example shows the measurements of C_inj_low from a 'B' chip, 4.5fF is ~consistently measured using all 4 frequencies (giving 44.7 e- per VCAL DAC count).**



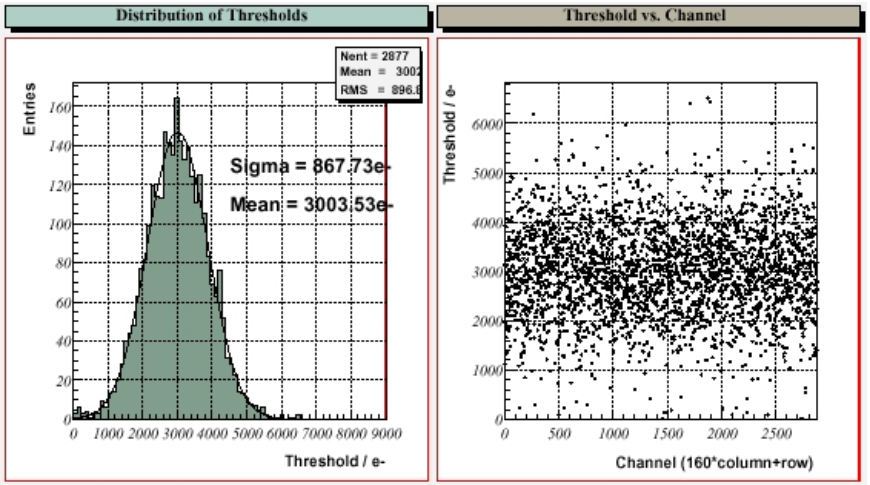
FEI1: Threshold and Noise Performance

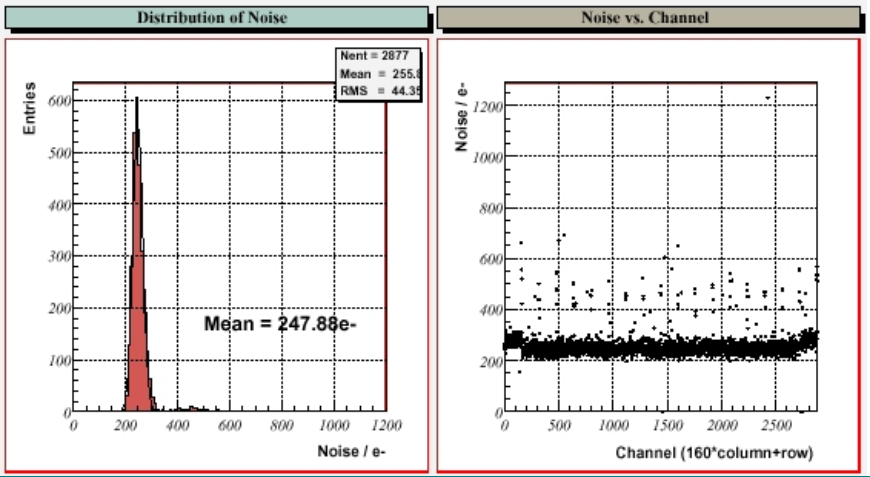
- Example of a threshold scan in which the 9-bit VCAL DAC of FE-I1 is scanned and the small injection capacitors are used in order to derive the usual 's-curves' of occupancy versus injected charge.
- This two dimensional online hitmap illustrates the integral of all hits over the scan per pixel.
- The 1D plots show individual s-curves for 4 arbitrary channels; here the 5-bit threshold trim DACs haven't been tuned in order to reduce the dispersion.
- Note that every single pixel is working; this is our normal experience for FE-I1 chips which have no major pathologies when probed at the wafer level.

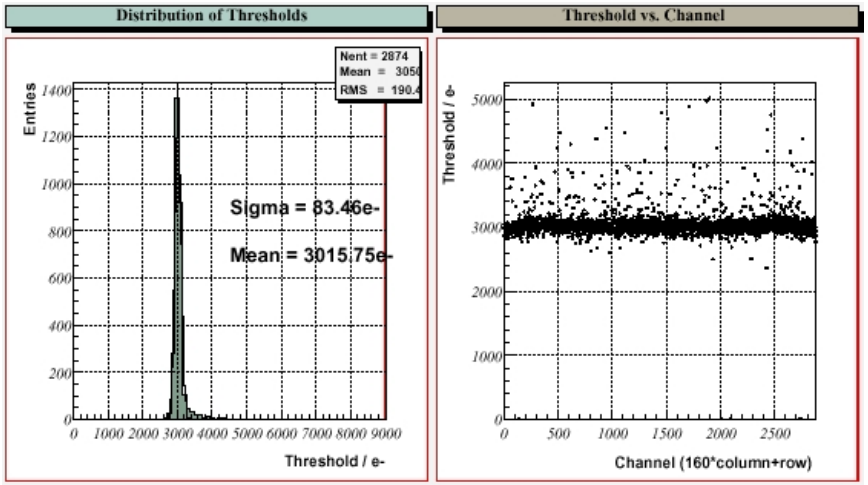


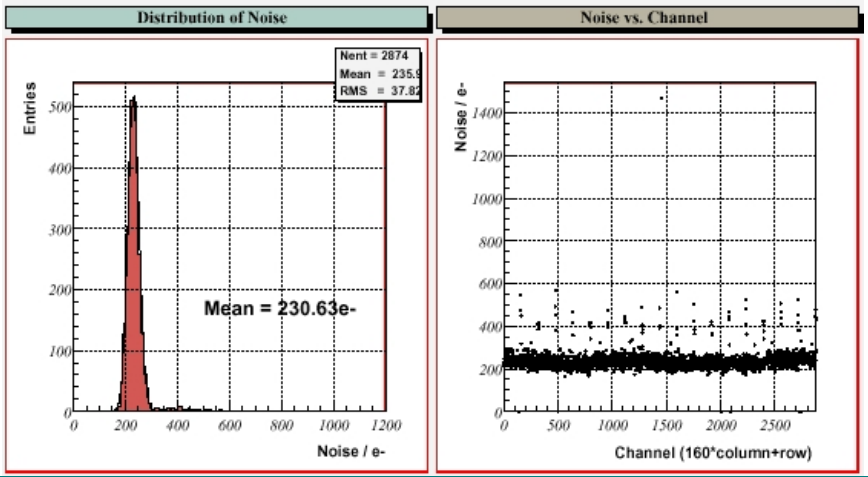
FEI1: Threshold and Noise Performance

- **Example threshold scans for an FE-I1 single-chip assembly (with preproduction sensor) before and after the 5-bit trim DACs have been tuned to minimise the threshold dispersion.**
- **Initial dispersion of 868e- (B-flavour) reduced to 83e- sigma with slight upper tail.**
- **Mean ENC of 247e- slightly reduced when all of the pixels are tuned.**







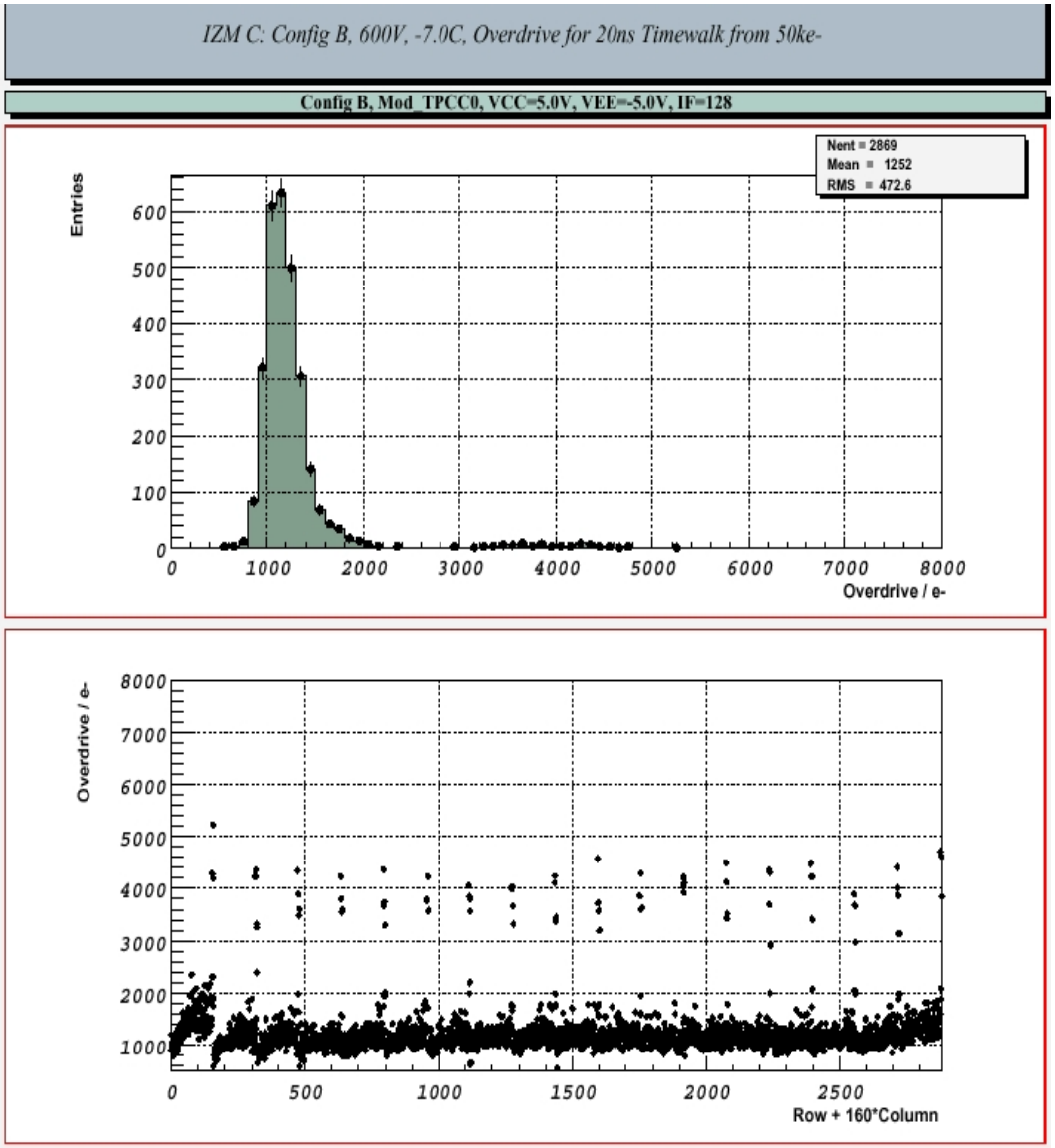


FEI1: Timewalk Evaluation

- Critial to correct operation of the pixel tracker in a 25ns BCO machine is degree of timewalk exhibited by the front-end (in order that hits are correctly tagged to their originating interactions).
- After irradiation it is of particular concern (if forced to operate the sensors partially depleted when already, trapping starts to have a significant effect on the charge yield).
- Strategy for studying timewalk with the TurboPLL system is to scan a large range of injected pulse amplitude and to determine the precise time at which the discriminator was seen to fire for each.
- TurboPCC and PICT provide means to delay the timing of the strobe (relative to the LV1 trigger) on a very fine scale with 8-bit resolution.
- For each value of charge, strobe delay is scanned and the precise delay which pushes the hit 'to be in-time with the trigger' is determined (by making an s-curve fit to the derived histogram of occupancy versus strobe delay).
- Magnitude of the timewalk defined to be amount of charge above threshold (overdrive) which results in 20ns of timewalk relative to a large injected charge (e.g. 50ke-).
- 'In-time threshold' is then the sum of the actual threshold and this figure.
- Other sources of timing uncertainty (e.g. trigger jitter) are accounted for by selecting 20ns in this definition.

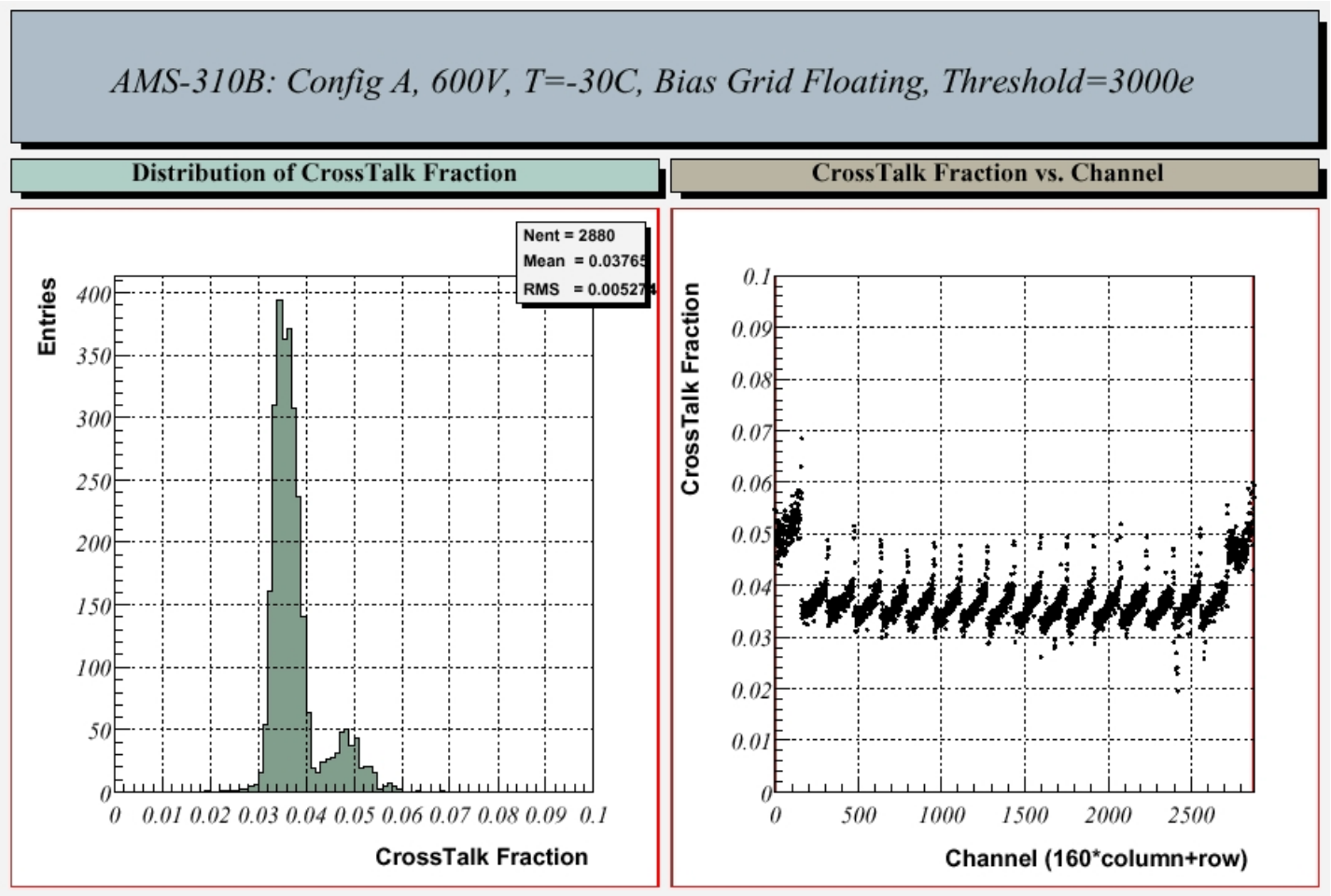
FEI1: Timewalk Evaluation

- Example of overdrive for 20ns of timewalk for FE-I1 (plotted as a distribution and per pixel).
- Data is from a single-chip assembly sample which has been irradiated to beyond the full ATLAS fluence (65MRad).
- Timewalk = a little over 1000e- giving an in-time threshold of ~4000e-. Slight degradation relative to the unirradiated case; likely reason is that the load presented by the sensor increases (due to overcompensation of the moderated p-spray.).
- Ganged pixels clearly stand out as outliers in the distribution. In FE-I2 these will be provided with extra power to speed up their preamp response.



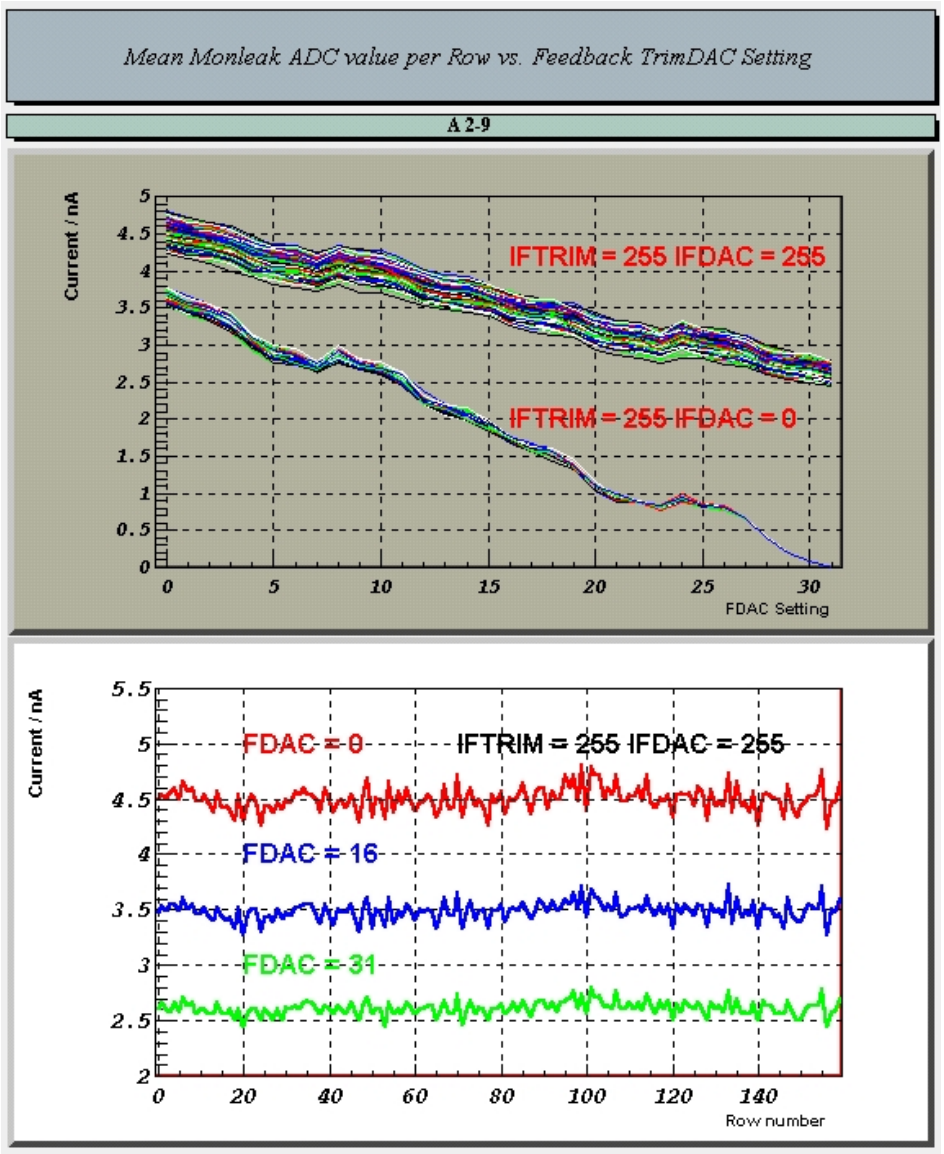
FEI1: Analogue Crosstalk Performance

- **In order to determine the degree of charge loss due to analogue crosstalk, for each pixel a very large range of charge is injected into its two neighbours (in rphi) and the point at which its discriminator fires is determined.**
- **Percentage charge loss then is simply the ratio of the charge for turn-on (divided by 2) and the threshold of the pixel in question.**
- **Example of the distribution of crosstalk for an irradiated assembly (65MRad). The regular pixels exhibit 3.5% charge loss to rphi neighbours.**



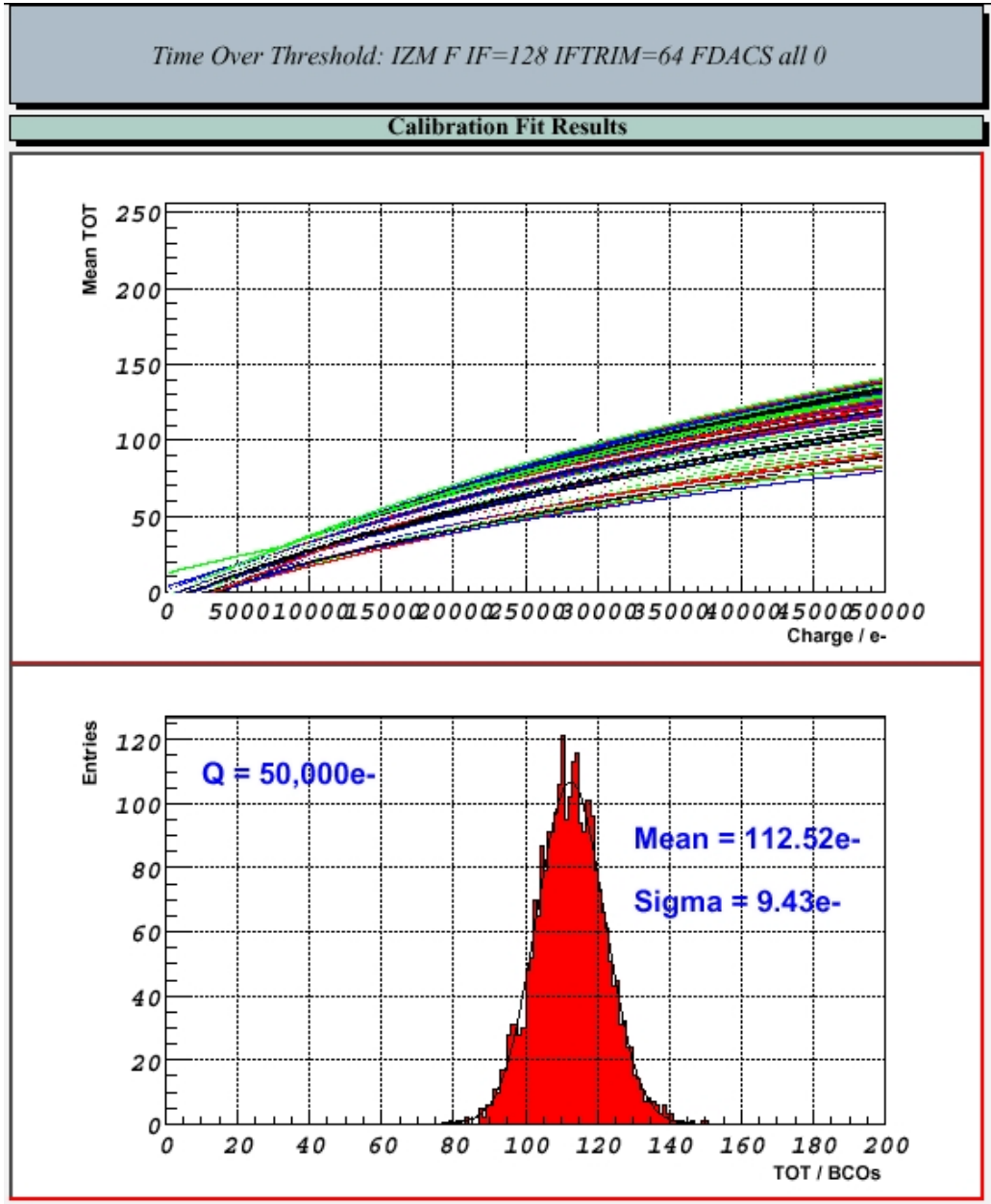
FEI1: Time-Over-Threshold Calibration

- FE-I1 provides 8-bit charge measurement which is derived using Time-Over-Threshold (TOT).
- The gradient of the recovery phase of pulses at the preamp output depends on the magnitudes of the feedback capacitance and the feedback current (provided by an 8-bit global DAC).
- Each individual pixel has a 5-bit trim-DAC fo the purpose of matching these feedback currents. Thus a global calibration can be applied once tuned.
- However even in the absence of any attempted tuning, the feedback currents are found to be very well matched.
- These plots show direct measurements of the feedback current for 160 pixels within a column versus the local trim DAC setting..



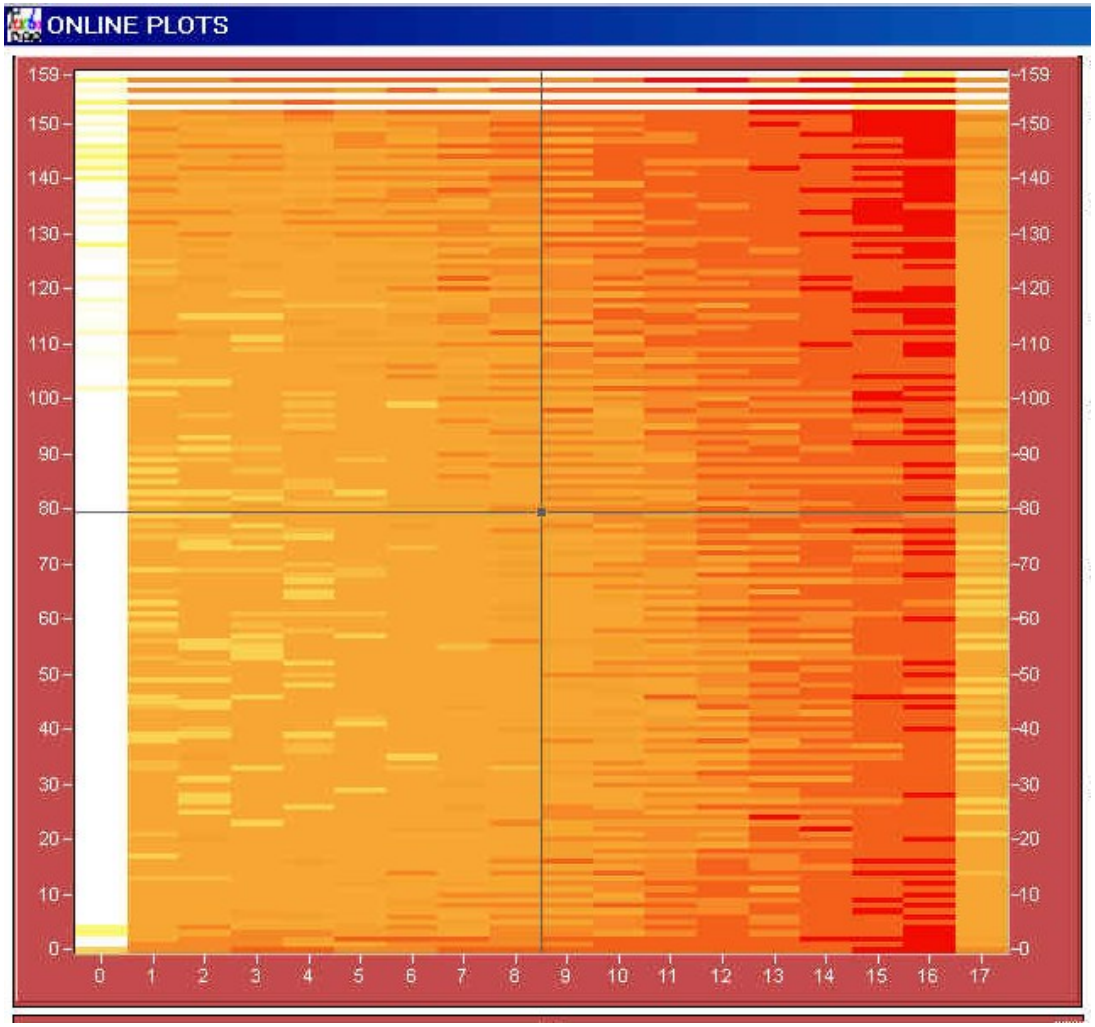
FEI1: Time-Over-Threshold Calibration

- **This excellent feedback matching translates directly into very good TOT matching.**
- **Upper plot shows calibration curves (mean TOT versus input charge) for all pixels within a single-chip assembly.**
- **In the lower plot the distribution of derived TOTs for a charge of 50ke- shows better than 10% agreement without any tuning…**



FEI1: MONLeak ADC Feature

- **Unique feature of FE-I1 is ability to measure the leakage current in each pixel using the MONLeak 'ADC'. Hitbus control mask may be used to select any combination of pixels to take part in the measurement.**
- **Threshold of single discriminator is selected using 9-bit DAC, status of which is stored in the global register. Binary search is performed to determine magnitude of leakage current at the 'ADC'.**
- **Before irradiation, leakage current in an individual pixel is negligable compared with the feedback current; observed current correponds to 3/2 X I_{fback}**
- **In this online plot example a single-chip assembly has been irradiated to ~0.3MRad and is at T=30C. Colour scale shows the leakage current in each pixel; White=25nA, Red=12nA. The PS beam profile is clearly visible!**

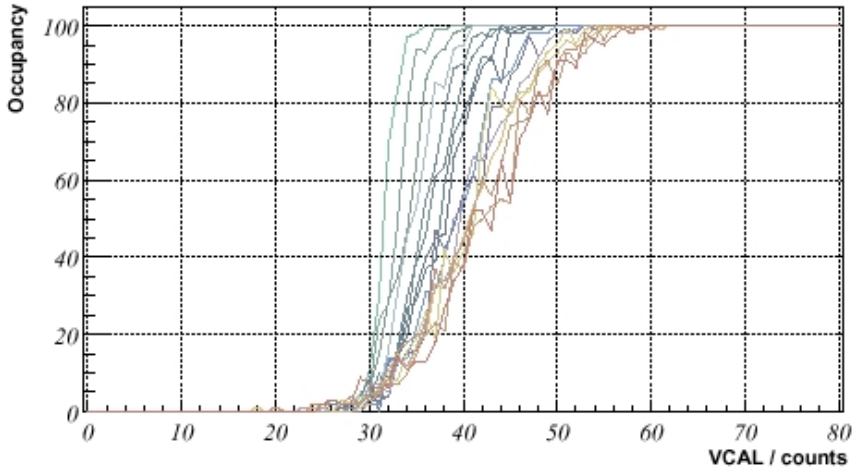


Analogue Test Chip: Noise Measurements

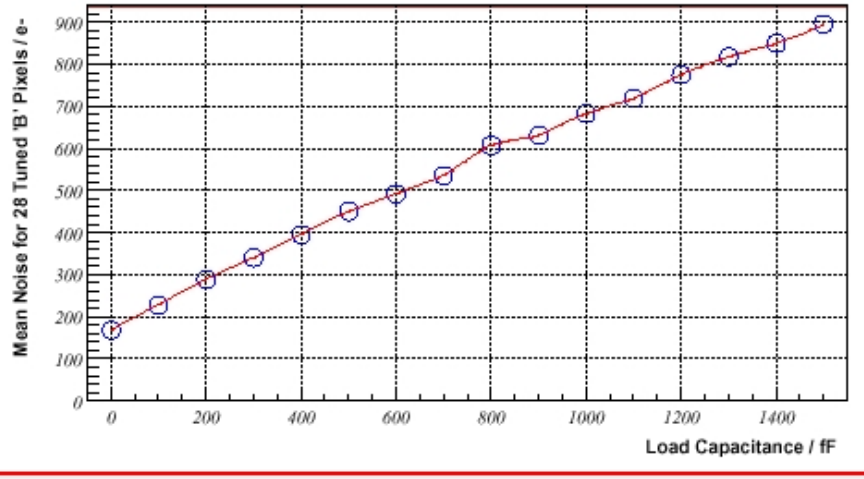
- The FE-I1 Analogue Test Chip has an array of 56 pixels (28 A flavour and 28 B flavour) and has the facility to artificially inject leakage current (from a DAC) and apply a load capacitance from 0 to 1500fF in steps of 100fF.
- These features are used in order to characterise the noise performance of the FE-I1 front-end.
- Here the mean noise for the 28 'B' pixels is plotted versus the applied capacitive load....
- Noise slope ~50e-/100fF

FE-I1 ATC: Load Capacitance Scan with ILKDAC=0

Single Pixel S-curve Data for 16 Values of Load-C, Pixel 30



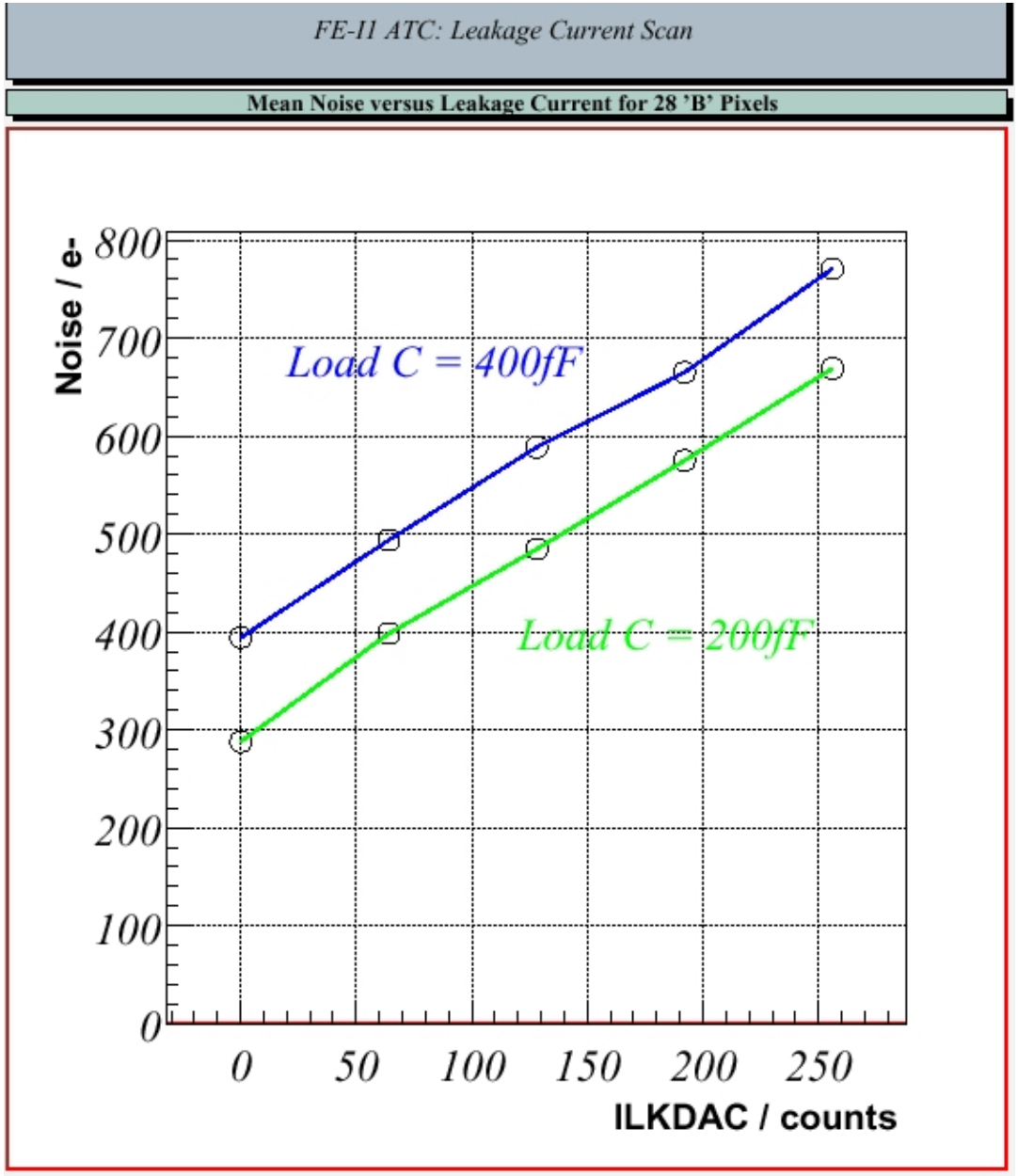
Mean Noise vs. Load-C for 28 'B' Pixels



Analogue Test Chip: Noise Measurements

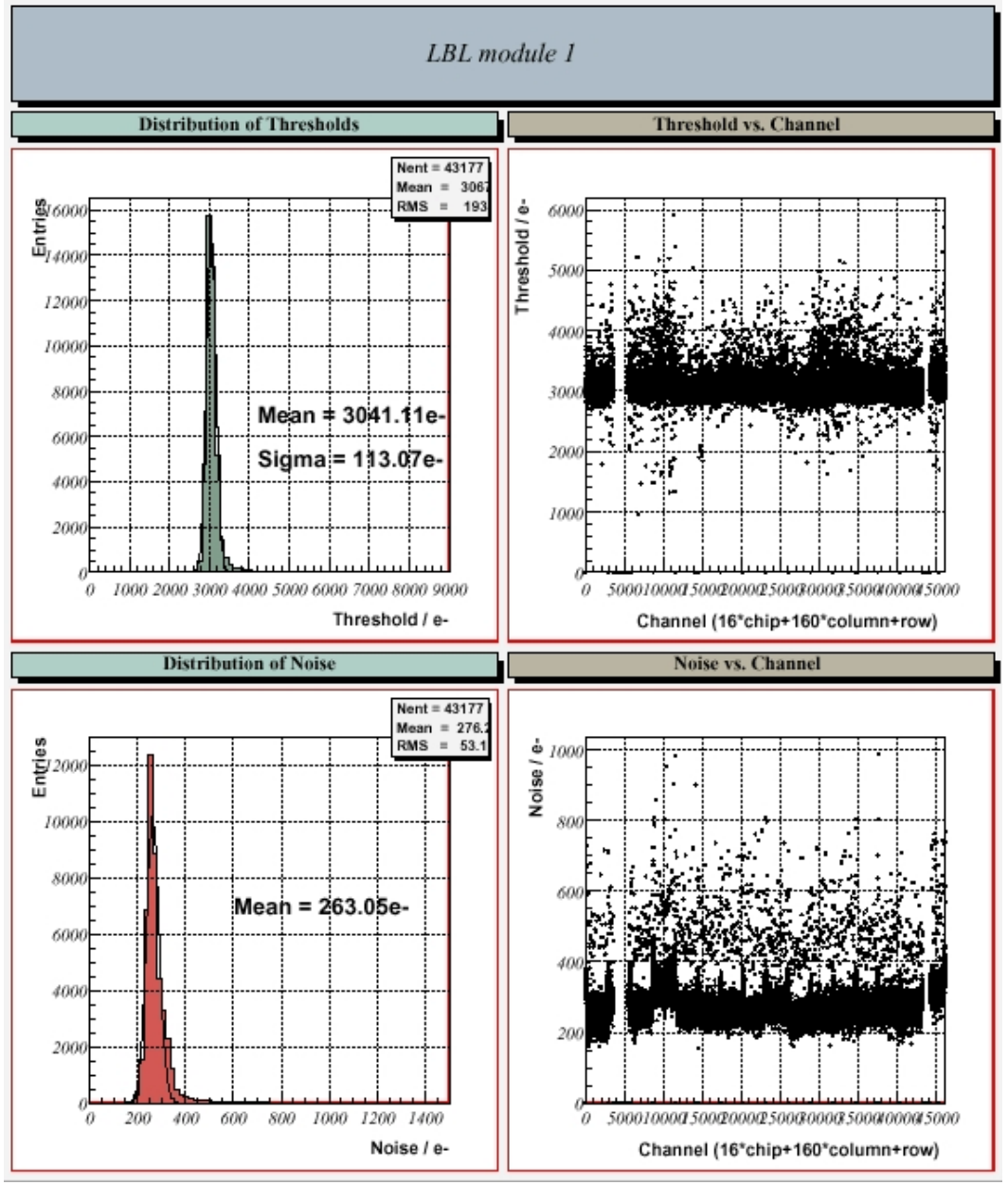
- **Here the injected leakage current is scanned in order to assess the sensitivity of the FE noise for two values of load capacitance.**

- **An ENC of ~400e- is observed for 25nA of leakage per pixel when the load capacitance is predicted to be 200fF (based on the comparison between non-irradiated data and the previous plot).**

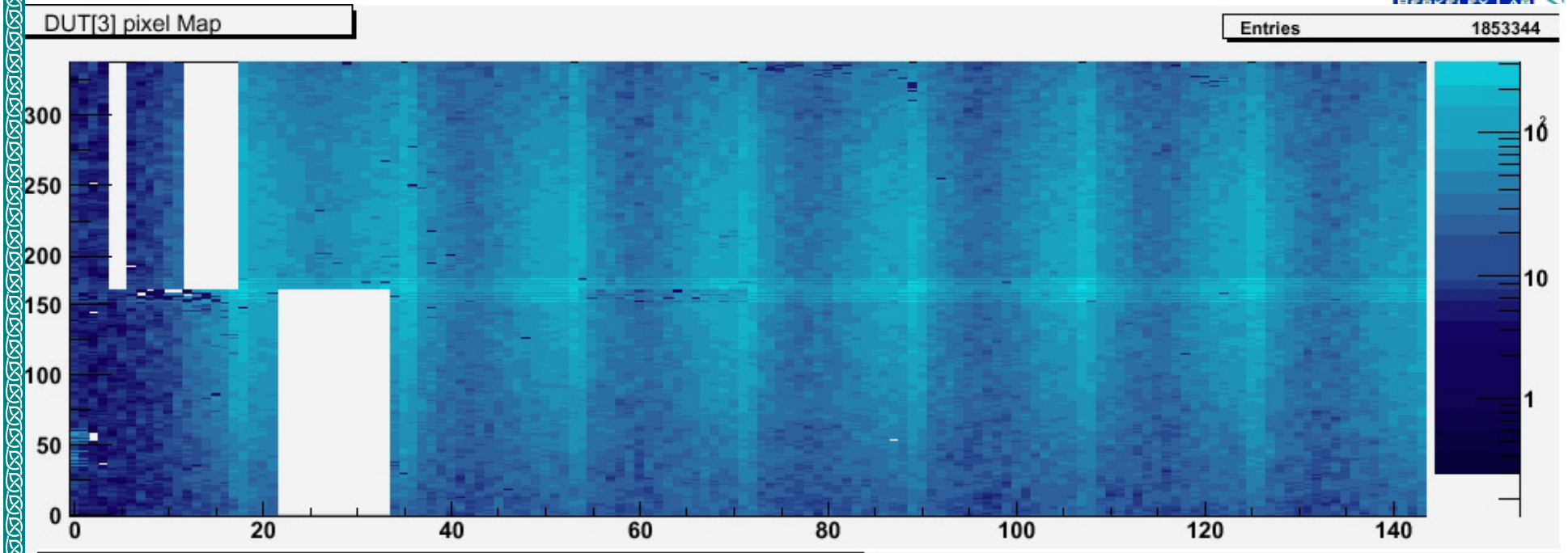


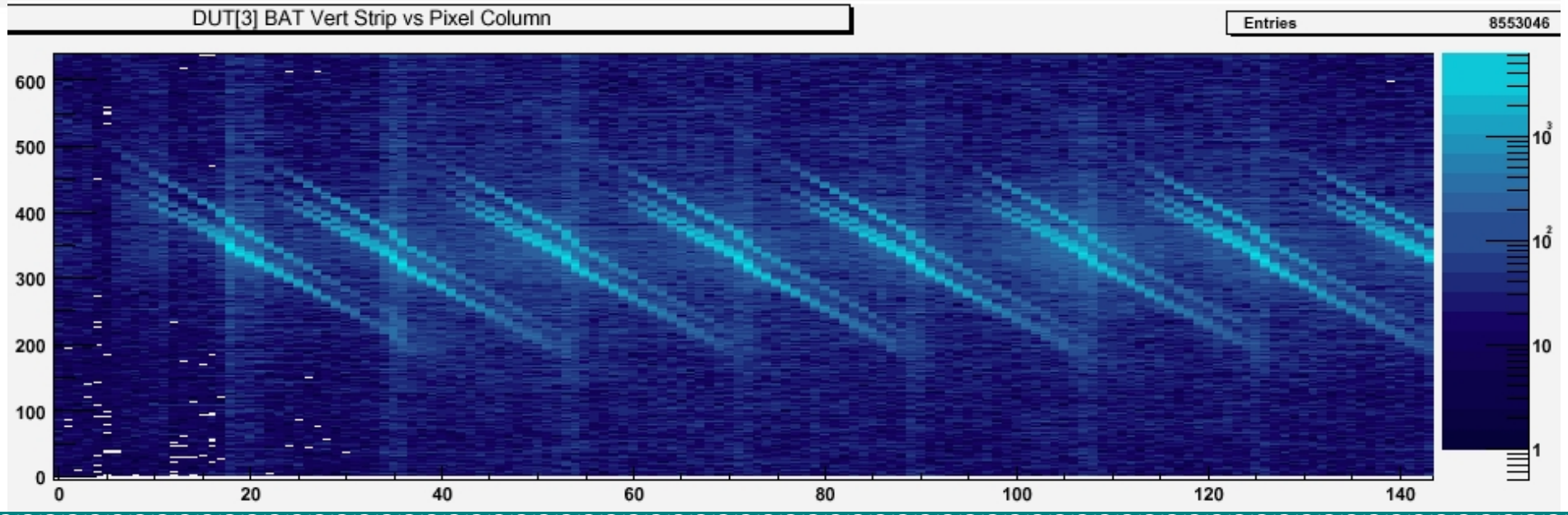
Fully Instrumented MCM Experience with 16 X FE-I1 + MCC-I1

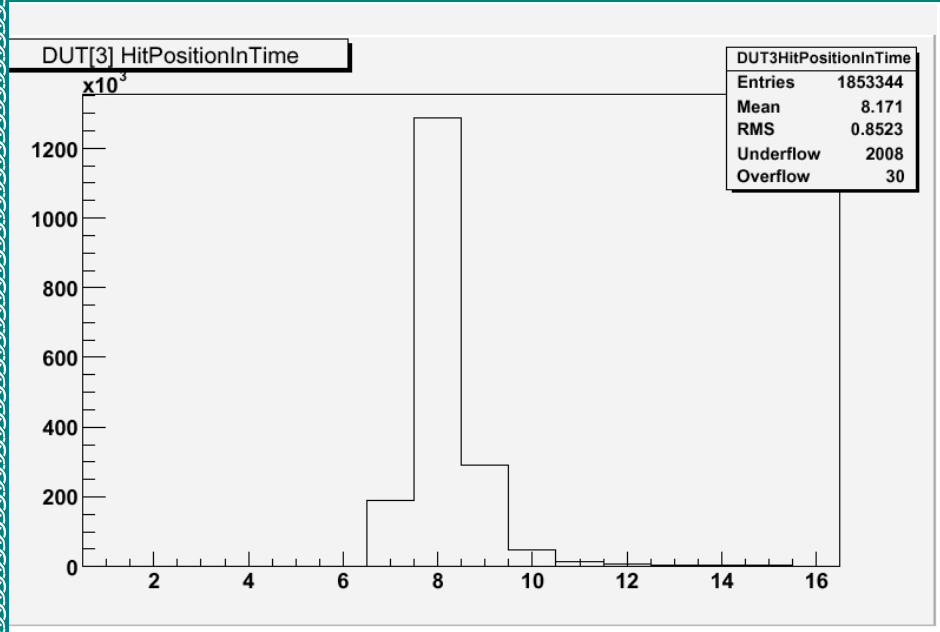
- Example of a threshold scan from an entire 16-chip module with all FE chips reading out concurrently through an MCC-I1.
- With careful TrimDAC tuning an overall threshold dispersion not dissimilar to the single FE assembly case is obtainable; 113e-.
- The noise performance is very encouraging; peak of the distribution is at 263e- compared with a typical single chip assembly ENC of 250e-.

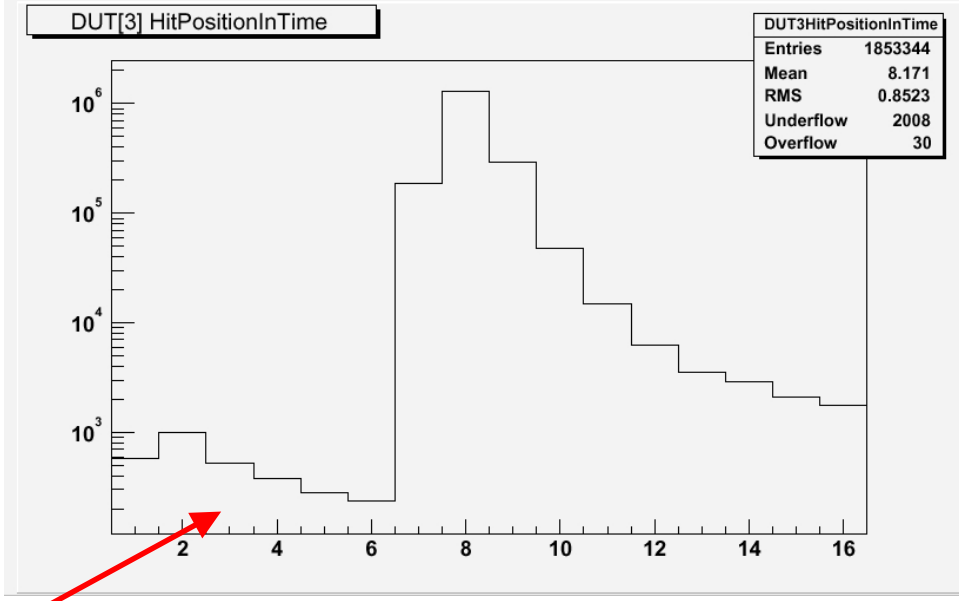


August 02 H8 Testbeam: FE-I1 Module Highlights (online monitor).....

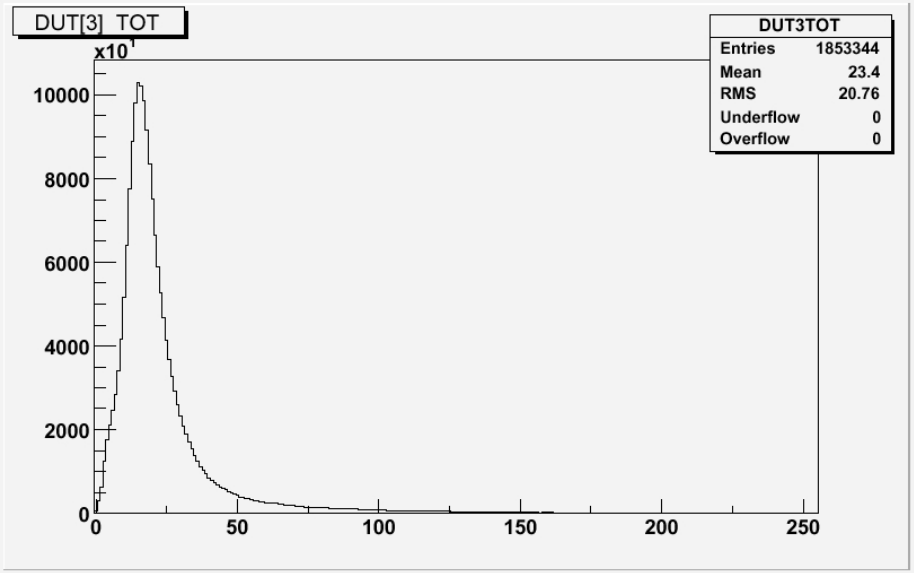


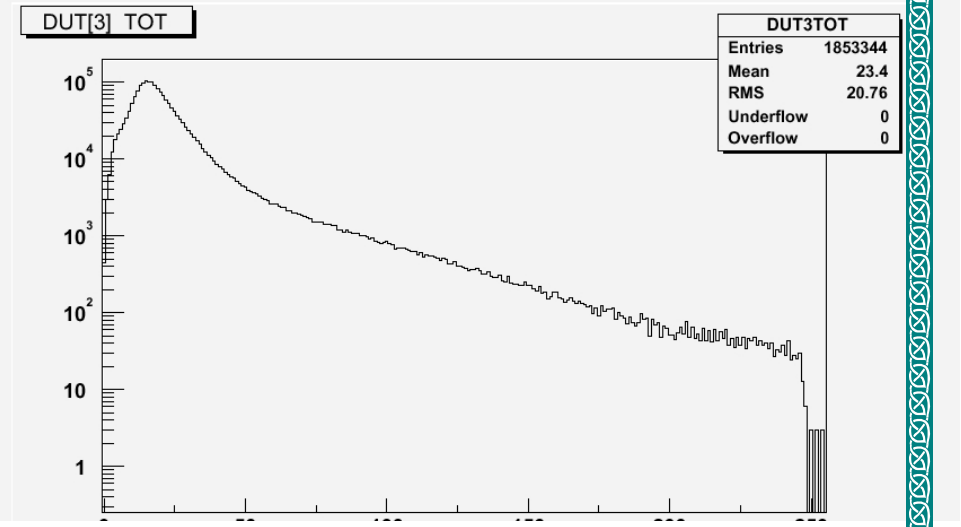






Noise Occupancy ~3X10^{-4} per module, translates to 6X10^{-9} per pixel!





Conclusions

- The first realisation of the ATLAS pixel front-end in Deep Submicron, FE-I1, generally performing very well
- Digital readout logic works ~as expected
- Initial untuned threshold dispersion is high but with 5-bit trim capability this may be reduced to ~100e-. There are several problems with the FE-I1 trimming scheme (non-monotonic DACs, distribution of trim current along columns etc.) which make the tuning procedure lengthy and difficult. These issues will be resolved in FE-I2.
- Studies of the timewalk indicate an overdrive of ~1200e- gives 20ns shift relative to 50ke- input charge; results in 4200e- effective threshold for 3000e- nominal threshold to be in time (after irradiation). The load introduced by the ganged pixels increases this to ~4000e- but in FE-I2 they will have enhanced preamp power.
- Analogue crosstalk is well below spec. for normal pixels and ~on spec for elongated pixels (after irradiation).
- TOT matching looks extremely good even without any tuning of the 5-bit feedback current trim DACs
- Aspects of observed single chip assembly performance translate ~directly to the multi-chip module scale