Multi-Element Si Sensor with Readout ASIC for EXAFS Spectroscopy[1]

Gianluigi De Geronimo[a], Paul O'Connor[a], Rolf H. Beuttenmuller[b], Zheng Li[b], Antony J. Kuczewski[c], D. Peter Siddons[c]
[a]*Microelectronics Group, Instrum. Div., Brookhaven Nat. Lab., Upton, NY, USA*
[b]*Semiconductor Detector D&P, Instrum. Div., Brookhaven Nat. Lab., Upton, NY, USA*
[c]*National Synchrotron Light Source, Brookhaven National Lab., Upton, NY, USA*

1 Introduction

Extended X-ray Absorption Fine Structure (EXAFS) experiments impose stringent requirements on a detection system, due to the need for processing ionizing events at a high rate, typically above of 10Mcps/cm^2, and with a high resolution, typically better than 300eV.
The detection system here presented is being developed targeting these stringent requirements. It is the result of a cooperation between the Instrumentation Division and the National Synchrotron Light Source (NSLS) of the Brookhaven National Laboratory (BNL). The system is composed of a multi-element Si sensor with dedicated per pixel electronics. The combination of high rate, high resolution and moderate complexity makes this system attractive when compared to other multi-element solutions [1,2]. In sections 2, 3 and 4 the sensor, the interconnect and the electronics are briefly described. Section 5 reports on the first experimental results.

2 Multi-element Si sensor

The Si sensor is composed of 384 square pixels, each having a 1mm^2 area, arranged in four quadrants of 12×8 elements (Figure 1) and it was fabricated at the Semiconductor Detector Lab. in the Instrumentation Division of BNL. The pixels are formed using p$^+$ boron implant (≈ 10^{14}/cm^2 at 40keV) on high resistivity (4-6kΩcm) n-type 250µm thick wafer with (111) orientation, with a planar n$^+$ ohmic contact on the back side using phosphorous implant (≈ 10^{14}/cm^2 at 150keV). A 100µm × 100µm aluminum bond pad was deposited in correspondence of each pixel. The pattern of the bond pads was studied for optimum wirebond to the front-end ASICs.

[1] Work supported by the US Department of Energy, Contract No. DE-AC0298CH10886.

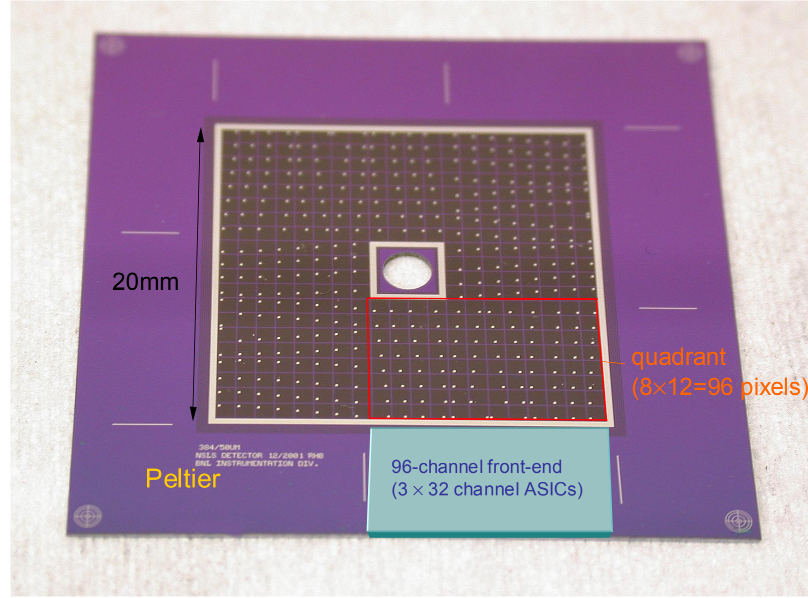

Figure 1: Photo of the Si sensor. Electronics sits off the long side of each quadrant; the Peltier cooling elements sit on the remaining passive area. The center is opened for beam through operation.

Versions characterized by different pixel spacing ranging from 10µm to 50µm were built and will be tested. An empirical approach will be used for selecting the spacing, depending on the effect of inter-pixel charge trapping on the spectra [3].

3 Interconnects

Three pixel-to-electronics interconnect solutions were considered: (i) metal traces integrated with the sensor to bring the wirebond pads edges to the closest electronics, (ii) low capacitance ball grid array, and (iii) direct wirebond of each pixel to an input of the front-end electronics. Major drawback of the first solution was the contribution to the ENC of the dielectric losses of the available dielectrics (polyimide, SiO_2, Si_3N_4), given by:

$$\delta ENC \approx \sqrt{2kTC_p \, tan(\delta)} \quad (1)$$

where C_p is the parasitic capacitance associated with the interconnect and $tan(\delta)$ is the dielectric loss of the material. For example, in the case of Si_3N_4 (assuming $\varepsilon_r \approx 6.5$, $tan(\delta) \approx 0.001$) with dielectric thickness 2µm, for a 6mm × 10µm interconnect the parasitic

capacitance would be C_p≈1.2pF with a contribution δENC≈20 rms electrons (the increase in ENC due to C_p is an additional issue). Drawbacks of the second solution were the ball grid material which could lead to anomalous fluorescence peaks in the measured spectra, the obstacle to illuminating the detector on the pixel side for test purposes, and constraints on ASIC area and layout. The third solution was selected for this prototype, considering tolerable the parasitic capacitance of the bond, on the order of 50-200fF.

4 Electronics

An Application Specific Integrated Circuit (ASIC) targeted to this application was designed at the Instrumentation Division and fabricated in 3.3V, 0.35μm CMOS DP-4M process. It is composed of 32 channels for a total of 180,000 MOSFETs, dissipating about 8mW per channel. The layout, optimized for minimization switching noise, measures 6.3×3.6mm^2 (Figure 2).

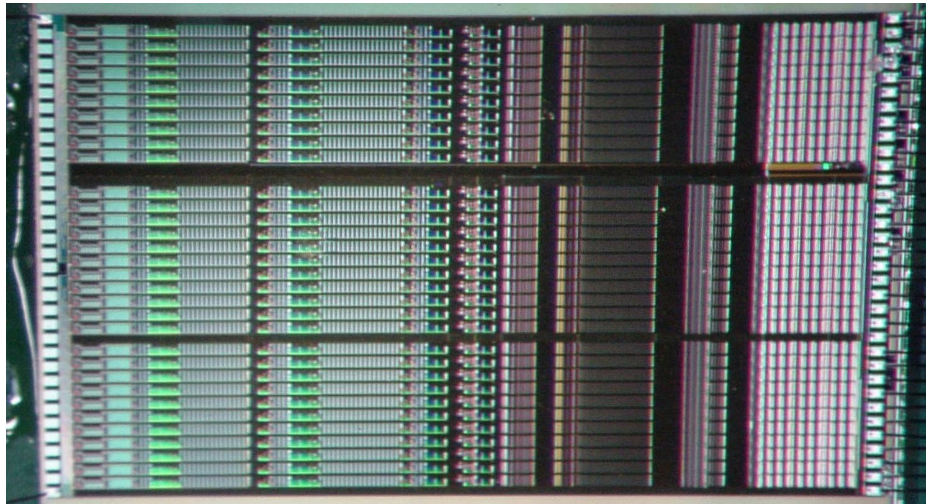

Figure 2: Photo of the 32 channel ASIC, composed of 180,000 MOSFET. Three chips will serve one quadrant (96 pixels) of the SI sensor.

Each channel implements (Figure 3) a low-noise preamplifier, a high order shaper, a baseline stabilizer, threshold and two window comparators with DACs for fine adjustment, a bank of counters, SPI interface. A brief description of the integrated electronics is reported below.

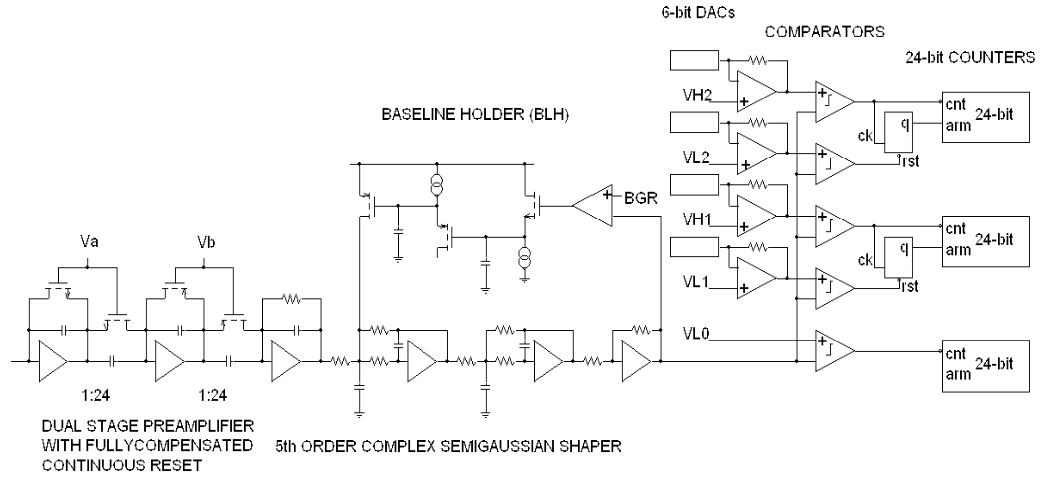

Figure 3: Simplified schematic of one channel of the ASIC.

The preamplifier has a p-channel input MOSFET with W/L=400/0.35, I_d=850µA, V_{ds}=800mV, g_m=8.6mS and C_g=620fF. The input parasitic capacitance (pad plus wirebond) is about 450fF. The two-stage preamplifier has a fully compensated continuous reset system [4] and provides a current gain of 576.
It is followed by a 5th order complex semigaussian shaper with bandgap referenced baseline holder (BLH) [5]. The overall analog processing chain has configurable peaking time (0.5, 1, 2, 4 µs) and gain (750, 1500 mV/fC), per channel calibration capacitor and masking, pixel leakage current monitor. Both the shaper output and leakage measurement can be multiplexed into a diagnostic monitoring analog output.
One threshold comparator and two window comparators follow each the shaper output. The five threshold levels are coarsely set through external voltages common to all channels. Each threshold level of the two windows can be finely adjusted per channel through a 6-bit DAC having ≈ 1.6mV step. Each comparator is followed by a 24-bit counter (three counters per channel) and, during the data readout, the counters of all 32 channels are cascaded for serial reading.
A serial peripheral interface is included for global settings, monitor enabling, channel masking, DACs setting, and counters readout. The channel layout area is 5854µm×102µm, with 1929µm for the windows and DACs and 690µm for the counters.

5 First experimental results

First measurements show at room temperature a pixel capacitance of 0.8pF, a pixel leakage

current of 60pA, an electronic resolution at 2µs peaking time of 14 rms electrons without the detector and of 40 rms electrons (340eV) with the detector connected and biased.
Cooling at -35°C a 200eV FWHM (167eV=20e$^-$ from electronics) was measured in a single channel at the Mn-Kα line of ^{55}Fe with all channels enabled and counters disabled (Figure 4).

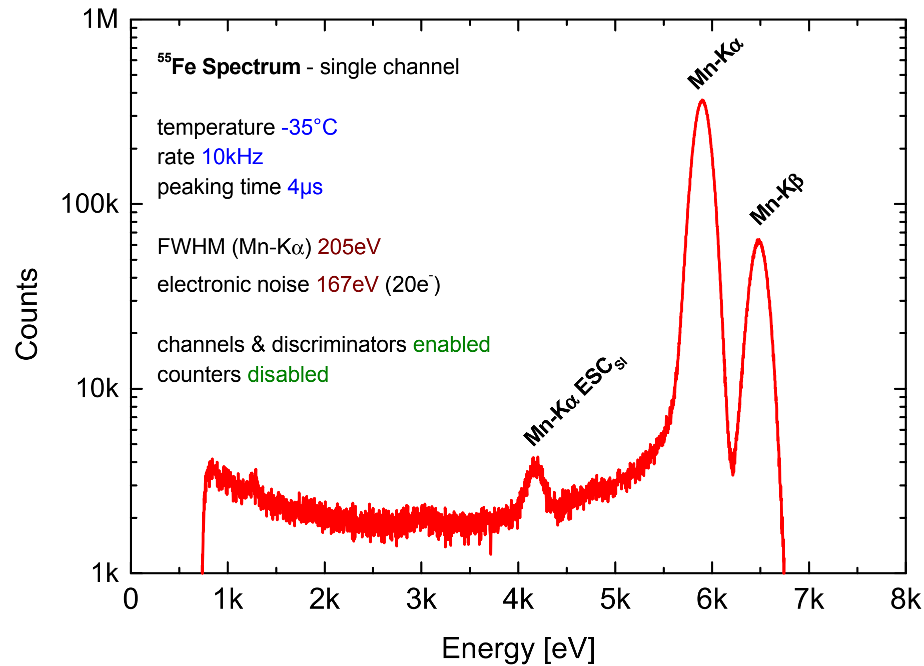

Figure 4: Spectrum of ^{55}Fe measured on a single channel cooling at -35°C. A few eV increase in FWHM was observed with all counters enabled.

At -20°C a 250eV FWHM (220eV=26e$^-$ from electronics) was measured with all channels and counters enabled. A 300eV FWHM was also measured at -20°C for rates above of 100kcps/cm^2 per channel, corresponding to an overall rate capability in excess of 40Mcps on a sensitive area of about 400mm^2.
The channel-to channel threshold dispersion before and after DACs adjustment was measured (Figure 5). The standard deviation after adjustment corresponds to 2.5 rms electrons at maximum gain. Noise measurements made with threshold scans, direct measurement of the analog monitor output, and X-ray resolution were in good agreement.

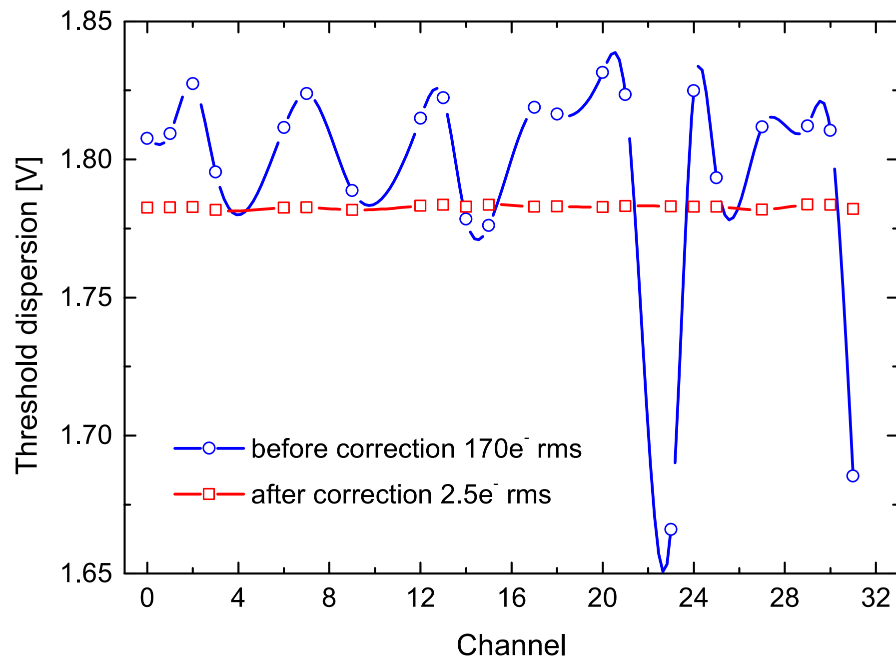

Figure 5: Measured threshold dispersion before and after DACs adjustment. Corresponding standard deviations are $170e^-$ and $2.5e^-$.

References

[1] P. Lechner, C. Fiorini, R. Hartmann, J. Kemmer, N. Krause, P. Leutenegger, A. Longoni, H. Soltau, D. Stötter, R. Stötter, L. Strüder, U. Weber, "Silicon drift detectors for high count rate X-ray spectroscopy at room temperature", *Nucl. Instr. Meth.*, vol. A458, pp. 281-287, 2001.

[2] A. D. Smith, J. E. Bateman, G. E. Derbyshire, D. M. Duxbury, J. Lipp, E. J. Spill, R. Stephenson, "A gas microstrip X-ray detector for soft energy fluorescence EXAFS", *Nucl. Instr. Meth.*, vol. A458, pp. 281-287, 2001.

[3] C. Rossington Tull, B. A. Ludewigt, D. Lewak, "Spectral response of multi-element Silicon x-ray detectors", *IEEE Trans. Nucl. Sci.*, vol. 45, pp. 421-427, 1998.

[4] G. De Geronimo, P. O'Connor, "A CMOS fully compensated continuous reset system", *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1458-1462, 2000.

[5] G. De Geronimo, P. O'Connor, "A CMOS baseline holder for readout ASICs", *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 818-822, 2000.