Studies on ATLAS pixel modules

Pixel 2002, Carmel, USA
Sept 09-12, 2002

Fabian Hügging – PI, Universität Bonn
Outline

Introduction

ATLAS pixel modules
- requirements
- concept
- assembly process
- serial powering of pixel modules

Results on prototype modules
- optical readout
- thermal behaviour
- modules with DSM electronics (FE-I)

Conclusions
Introduction

Modules basic building unit of pixel detector:

- 3 barrels at different radii
  - staves with 13 modules
- 2x3 disks in forward region
  - disk sectors with 6 modules
- 80 millions channels, 2000 modules
ATLAS pixel module

- size 63.0x18.6 mm$^2$
- 60.8x16.4 mm$^2$ active silicon
- 46080 pixel of 50 x400 µm$^2$
- 16 FE-chips with 2880 readout cells (160 rows, 18 columns)
- Module Control Chip (MCC) controlling the 16 FE
- Flex-Hybrid circuit for routing the signals/powers

- flex-hybrid
- MCC
- barrel pigtail
- 8 FE on each side
Requirements

**Electrical performance**
- **3000 e⁻** threshold with a dispersion of **200 e⁻**
- **noise** **200-300 e⁻**
- **efficiency** > **98%**

**Reliability**
- **10 years operation** in ATLAS, almost no maintenance
- **thermal tolerance** between **−30°C and +25°C**
- **radiation tolerance** up to **$10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$**, **500 kGy** (for B-layer)
- **high position stability** (vertex/tracking detector)

**Production**
- **testability during all assembly steps**
- **high yield production**
- **material** less than **3% $X_0$**
Concept

Components

- 1 double sided silicon sensor
- 16 thinned FE chips
- 1 4-layer flex-hybrid circuit with passive components
- 1 thinned MCC
- 1 2-layer flex-hybrid (barrel/disk-pigtail) with micro-connector for cable connection

Interconnections

- chip-sensor: fine pitch (50µm) PbSn or Indium bump bonding
- chip-flex: wire-bonding small wires (17.5µm)
- flex-pigtail: wire-bonding thick wire (50µm)
- Different gluing connections: sensor-flex, MCC-flex, pigtail-flex, micro-connector-pigtail

Atlas pixel modules are a complex mixture between sensible components and advanced interconnections techniques
Assembly process

Test sensor
Bump & cut sensor wafer into tiles

Test FE on wafer
Bump, thin & cut FE-wafer

Test FE-chips

Flip bare module
Test bare module

Test & Character module

Glue flex-hybrid to bare module
Bond FE-chips to flex-hybrid

Test equipped flex-hybrid
Glue & bond pigtail
Test equipped flex-hybrid +pigtail

Equip flex-hybrid
Clean flex-hybrid & glue to support
Bond to support
Glue & bond MCC on flex-hybrid

Test flex-hybrid
reject

Test sensor
reject

Test FE on wafer
reject

Test FE-chips
reject

Test bare module
reworking

Test & Character module
reworking

Glue flex-hybrid to bare module
Bond FE-chips to flex-hybrid

Test equipped flex-hybrid
reworking

Glue & bond pigtail
Test equipped flex-hybrid +pigtail
reworking

Fabrication process
Module assembly

so far 15 hot modules have been assembled in Bonn using different sensors, FE chips, flex-hybrids, pigtails:

• 4 FE-A/C, 8 FE-B, 1 FE-D2s, 2 FE-I

Many dummy modules have been assembled to learn/train the various production steps

• gluing procedures, wire-bonding, pigtail mounting, cable connection, ....

The module assembly procedure is now nearly clear

• e.g. time to assemble one module from bare module, fully loaded flex without MCC and pigtail is less than a day

But module assembly still remains a complex process with ~50 single production steps!

• Quality control during production is very important
An old story: 'Serial Powering'

The Problem:

- **Supply voltages in DSM decrease** (we are at 1.6V-2.0V). At constant power dissipation in the chip the supply currents increase.
- Because the cross section of the cables is limited, we dissipate a lot of power in the cables (in ATLAS: roughly half of the total power!) ⇒ cooling problems, material...
- If supply current changes (digital activity), chip voltage will have dips.
- Connecting modules in parallel does not help.

A possible solution, already proposed for other applications (e.g. CMS silicon tracker):

- Connect modules in series
- Supply the string of modules with a constant current $I_0$
- Every module uses a shunt regulator to generate it's digital supply
- The analog supply voltage is generated with a linear regulator from vddd
- Data transmission is via optical links ⇒ no problem with potentials
- Power wasted is $(I_0-I_{\text{module}}) \times V_{\text{module}}$

If this worked, it would save a lot of

- power, ... cables, connectors, ... cooling, material, power supplies, ... money
Circuitry on chip/modules

- Shunt regulators have 'soft' turn-on to distribute lost power equally on chips
Tests with FE-I single chips

- Shunt regulators and linear regulators are implemented in FE-I as testing option
- Regulators have some minor design errors but they work
- First tests with single chips show no difference to parallel powering
- Further investigation on modules are ongoing

1 + 2 chips in series

(4780 ± 105)e⁻ thres./ (268 ± 30)e⁻ noise
Optical module readout

Sensor 16 chips MCC

1 Sensor
16 FE
1 MCC

barrel modules: twisted pair microcables

2 VCSEL driver chips (VDC)
1 PIN diode receiver (DORIC)

Opto Reveivers
Readout Drivers (ROD)
Readout Buffers (ROB)
Timing Control (TIM)
Slow Control, Supplies

Power supplies

Opto Card
ROD
ROB
CTRL
Setup for optical readout

PLL opto interface (Siegen)

Clock return (XCKR) generated on this card

PCC

Pigtail

Sync, MCC TM, power...

PLL

Opto Board (OSU)

Microcable (LVDS)

Standard test setup

LVDS driver card

Flex support card

BPM

DRX

DORIC (D3)

VDC (D2)

LVDS

Standard test setup
Setup for optical readout

- microcables
- PLL opto interface (Siegen)
- opto board (OSU)
- FE-B module with pigtail
- optical fibres
Results: Module with full optical readout

- at 40µA PIN current
- untuned threshold distribution of a FE-B module shows no difference to standard test setup

threshold \((4470 \pm 380)e^-\)

noise \((340 \pm 50)e^-\)
Results: chip #4 optical readout

- no significant change visible
- all changes are usual fluctuation seen in FE-B modules

![Graph showing ENC and PIN current](image)

- measured with standard test setup
# Thermal behaviour of a hot module

Module 12: FE-B module with pre-production Tesla sensor and Flex2.x glued on carbon structure in flex frame

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<tr>
<th>Test Scenario</th>
<th>Temperature Range</th>
<th>Notes</th>
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<td>9 x cycled between 25°C and -10°C measured on the flex under full power</td>
<td>25°C to -10°C</td>
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<tr>
<td>1 x cycled between 25°C and -25°C by switching off the power</td>
<td>25°C to -25°C</td>
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<td>Testbeam August 2001</td>
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<td>20 x cycled between 25°C and -30°C without power</td>
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<td>Testbeam October 2001</td>
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<td>Source measurement January 2002 with Am$^{241}$</td>
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</tbody>
</table>
Source measurement

- nearly all pixel of the initially 25,600 pixel are still working

- FE-B has only 10 of 18 columns working

- 1 dead chip
Source measurement

- 1 pixel with low statistics
- 1 with a bump failure (merged bump)
- 1 candidate of a broken bump due to thermal or mechanical stress

3 pixels without hits
FE-I modules

- Some FE-I (A/B) modules have been assembled
- Bumped with Pb/Sn at IZM or Indium at AMS
- Using CiS/Tesla preproduction sensors
- With FH v4.1 (Compunetics) or with FH v4.2 (Dyconnex)
- 2 modules work via barrel pigtail and microcable prototypes
- First modules operated in last testbeam (2 weeks ago)
**FE-I modules: threshold and noise**

**Module before tuning (Mod2):**
- Threshold: (3400 ± 1200)e⁻
- Noise (290 ± 30)e⁻

**Module after tuning (Mod1):**
- Threshold: (3000 ± 120)e⁻
- Noise (280 ± 30)e⁻
FE-I module: source measurement

- three big capacitors shadowing the source
- 1 chip disabled (only 2 columns working)
- 12 non working columns

Am$^{241}$ source scan of Mod1

- only 36 of 41280 pixel don’t see hits!
Conclusions

- A lot of experience of pixel module assembly with different chips, sensors, flex-hybrids, bumping techniques exists now.
- The ATLAS pixel prototype modules show to fulfill the challenging requirements of 10 years operation in ATLAS:
  - No degradation with thermal cycling observed.
  - Full optical readout without performance loss possible.
- Modules with DSM FE-I chips successfully assembled and operated in lab and testbeam.
- Serial powering of modules seems to be interesting option but needs further studies.