Studies on ATLAS pixel modules

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For the ATLAS Pixel Collaboration [1]

1 Introduction

The Pixel Detector of the ATLAS experiment at the LHC, which is currently under construction at CERN, Geneva, is the crucial part for good secondary vertex resolution and high b-tagging capability. Therefore high spatial resolution and fast read-out in a multi-hit environment is needed and leads to the use of a hybrid silicon pixel detector. This detector will consist of three barrel layers and three disks in each forward direction to have at least three space points up to $|\eta| = 2.5$ for particles with a transversal momentum greater than 500 MeV [1].

The smallest detector unit will be a module made of one silicon pixel sensor and sixteen readout chips connected with high density bump bonding techniques to the sensor. Each module consists of about $50,000$ pixel cells with the size of $50\mu m \cdot 400\mu m$ to reach the required spatial resolution of $12\mu m$ in $r\phi$-direction. For the connection of signal and power lines between the readout chips and further readout electronics a two layer flex capton is used which is glued to the backside of the sensor and carries besides different passive components also a module controller chip (MCC). The main requirement for the ATLAS pixel modules is high radiation tolerance of all components in a harsch radiation environment close to the interaction point. The integrated design fluence is $10^{15} cm^{-2}$ 1 MeV neutron equivalent coming predominantly from charged hadrons over ten years for the outer barrel layers and disks and five years for the innermost layer.

Secondly the total need of about $2,000$ modules requires very good testability of all components before assembly and high fault tolerance in long term operation as they are not supposed to be exchanged during the whole foreseen ten years lifetime of the ATLAS experiment. The material budget for the whole pixel detector is very strict to affect the later detector parts as less as possible. This leads to a total amount of material less than 1.2 % of one radiation length per module not including further services and support structures.

2 Module Concept

A cross-section of an ATLAS pixel module can be seen in figure 1. The module basically consists of a so called bare module which meant the sixteen readout chips bump bonded to the silicon pixel sensor. The size of the module is roughly given by the size of the sensor $18.6 \cdot 63.0$ mm^2. The readout chips with 2880 readout cells and a size of $11.0 \cdot 7.4$ mm^2 each are placed in two rows of eight. The front-end chips are slightly longer than the sensor width to be able to reach the wire-bond pads of the chips. The interconnection techniques using fine pitch bump bonding is either done with Pb/Sn by IZM[1] or with Indium by AMS[2]. The total active area of one module is $16.4 \cdot 60.8$ mm^2 with 46080 pixel.

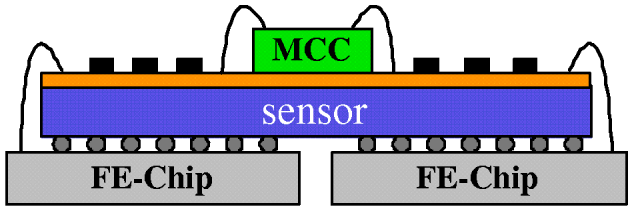

Figure 1: Cross-section of an ATLAS pixel module.

For routing the signals to the MCC and further to off-module electronics and providing the analog and digital supply powers to the readout chips a two layer high density interconnect (flexible capton cable) is used [2]. Also the flexible hybrid carries the MCC chip which performs control and clock operations. It is glued to backside of the sensor and has roughly the size of the sensor tile. To connect the flex hybrid with the frontend chips and with the MCC standard wire bond techniques are used; altogether around 350 wire-bonds are needed for a complete module. The module is glued chips down to the mechanical support which also serves as cooling structure. The whole power consumption of about 4 W per module has to be dissipated through the readout chips to allow an operation of the module at -6°C.

The modules for the barrel and for the disks of the pixel detector are almost identically. The only difference between those modules is a different shape of the pigtail which provides the power and connects the modules with off-module readout via the opto-link for high speed data transmission. The disks modules use a short flex hybrid along the long side of the modules with micro-welded cables on it to connect to the patch panel 0 (PP0) where the opto-link is located. The barrel modules in contrast have a slightly more complicated design. Due to the limited space in the

[1] Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany.
[2] Alenia Marconi Systems, Roma, Italy.

barrel region the pigtail has to be bent to the backside of the module on the support structure. Therefore the pigtail is mounted perpendicular to the disk pigtail; also it contains a micro-connector to plug in the twisted pair aluminium cables for the PP0 connection. The needed cable lengths are between 600 and 1300 mm depending on the location of the module in the barrel. A photo of such a barrel module can be seen in figure 2.

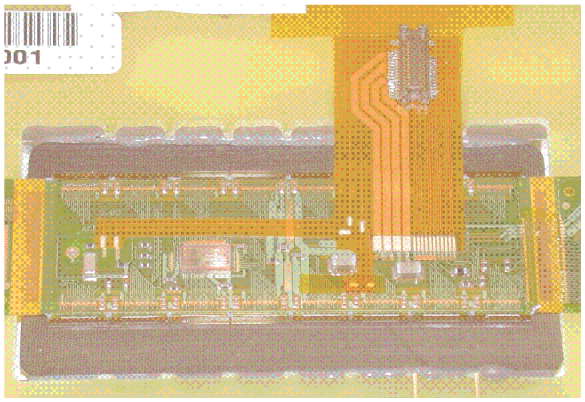

Figure 2: Photograph of an ATLAS pixel module with a barrel pigtail.

3 Module readout

Due to the fact that the MCC controls the 16 FE-chips on a module only three signals are needed for the module readout: These signals are the 40 MHz system clock (XCK), one Data input signal (DCI) and two Data output lines (DO, DO2). The readout chips as well as the MCC are the results of a prototype phase about three chip generations using various technologies. The latest version is fabricated in a five metal 0.25 μm technology (DSM) on 8″ wafers. This technology allows a radiation tolerant design by using specially developed design rules and transistor layouts. More details about the design and performance of these FE-I chips can be found elsewhere [4, 5].

For the special need of higher data transfer rates of the b-layer modules a second Data Out line can be used on each module. Using the two output signal lines a maximum data transfer rate of about 160 Mbits^{-1} can be achieved with ATLAS Pixel modules. All these signals are provided as LVDS[3] signals to reduce the cross-talk and pickup noise risk. The signals and voltages can be transferred either via the pigtail and micro-cables as it will be later in the experiment or via a card-edge

[3]Low Voltage Differential Signal

connector directly to the handling frame which holds the module during the assembly process and also carries a fan-out of the signals to flex capton.

In the used test setup the signals together with two supply voltages, one digital and on analog, are connected to a dedicated daughter card which serves as an interconnection to the standard ATLAS Pixel testsystem. This testsystem is a PC controlled VME-based system basically consisting of two cards, one for controlling the whole readout and one providing the needed supply voltages to the device under test. This testsystem provides not only basic test and readout functions of modules but also serves as powerful configuration tool in a laboratory environment allowing easy and fast tuning steps like threshold tuning. All later on shown results have been measured with this testsystem. More information about the functionality of this system can be found elsewhere [3].

4 Assembly process

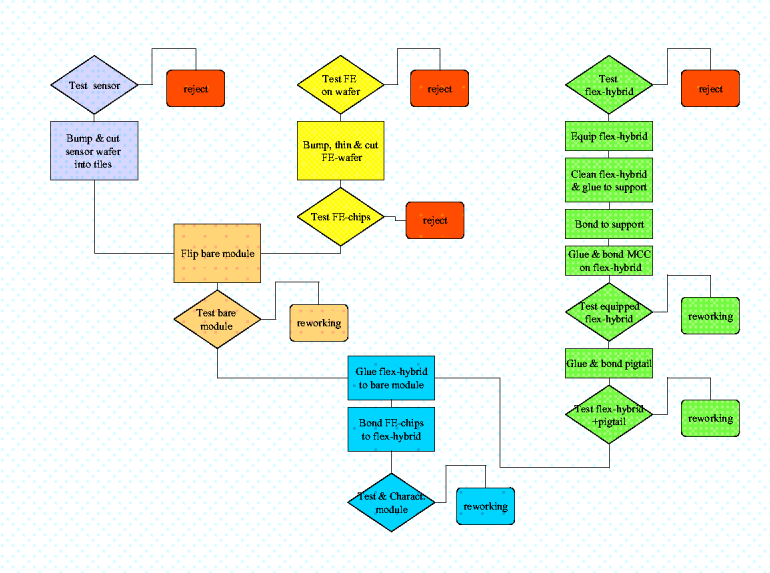

Figure 3: Assembly flow for building ATLAS pixel modules.

A flow chart of the assembly process of ATLAS pixel modules is briefly shown in figure 3. As one can see there it consists of many single production steps followed by many testing steps of individual parts to guarantee a high production yield. The three basic parts of a module are the silicon sensor, the readout chips and the high density interconnect (Flex capton). All these parts will be produced commercially by different vendors and will be put in the production chain after initially acceptance tests.

The sensors as well as the readout chips are delivered as full sized wafers because the following step of fine pitch bump bonding requires a wafer level process. Each sensor tile is flip chipped to 16 readout chips building a so called bare module by a commercial firm. The bump bonding is further complicated by the fact that the readout chips have to be thinned from the thickness of about 700 μm to approximately 180 μm after bump deposition but before flip chip to reduce the material of the modules inside ATLAS. An additional testing step of the readout chips is included directly prior the flip chipping to increase the yield of the bare modules significantly by using only known good dies after bumping, thinning and dicing. This testing of diced FE-chips needs a special test and transport carrier which holds the chips during probing and does not damaged the bumps during transport. Such a carrier has been successfully developed for this purpose.

After delivery the flex capton will be laminated to a support frame which serves as a handling and transport structure during the following assembly steps not only for the flex itself but also for the module once the flex is glued to the bare module. After lamination of the flex to the support they are loaded with passive components and tested concerning the signal and power traces and the high voltage stability. For testing purposes the flex capton will be wire bonded to support frame allowing easy access to the signal and power traces via a card-edge connector which is simply plugged to one side of the frame. Further assembly steps now include the mounting and wire bonding of the MCC and the gluing and wire bonding of the pigtail later used as outer world connection.

The most important step in module assembly is the connection between the fully equipped flex capton hybrid and the bump bonded bare module. An individual test of both parts can be performed. Therefore each FE-chip of the bare module will be probed like before on wafer level. Also the flex can be tested by probing each chip position with a dedicated probe card carrying a packed FE-chip. Next the flex is glued with a soft silicon glue to the backside of sensor and cured at room temperature for 8 hours. Because the pitch for wire bonding the chips to the flex is only 150 μm a precise alignment of the flex to the bare module is necessary. Four alignment marks on the backside of sensor located in each corner are used for this purpose. The next assembly step is the wire-bonding of all 16 readout chips to the flex hybrid with a 17.5 μm aluminium wire using a full automatic wire-bonder. The final assembly step is the wire-bonding of the HV to sensor's backside through a hole in the flex. For all these described assembly steps special tooling is used which has been developed, built and optimized in the last years. To this tools belongs special vacuum chucks for testing and wire-bonding of bare modules, gluing tools allowing a precise and reliable gluing of modules to flex hybrids and a semi automatic wire-bond test facility.

5 Results on prototype modules

Several modules with FE-I readout chips were successfully assembled in the described way using different bump bond techniques and different flex capton supplier. Prototype modules were successfully operated in lab environment and at the testbeam facility at CERN where the modules are tested with 180 GeV pions allowing detailed resolution and timing measurements. The analysis of the results of the testbeam studies is still underway so the main scope of the following concerns a selection of lab measurements.

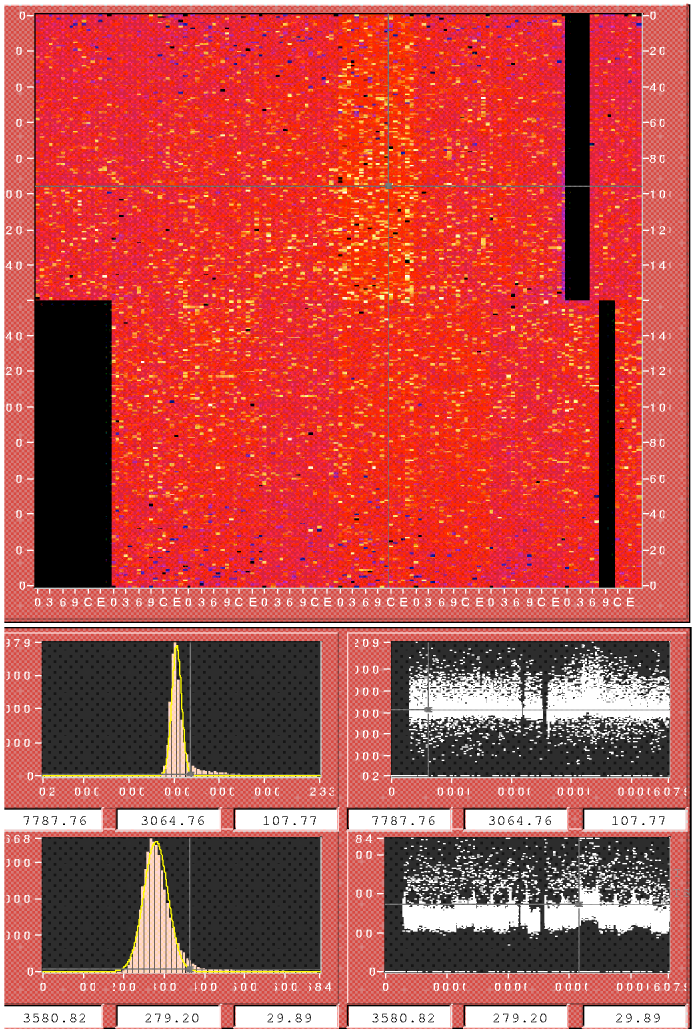

Figure 4: Threshold map and threshold and noise and distributions of an ATLAS pixel module with FE-I readout chips. The dead regions seen in the hitmap are due to three known non-perfect readout chips.

After assembly the modules are tested in detail with the ATLAS pixel testsystem. First the digital functionality of the module is tested by simple register tests and injecting test pulses directly into the digital part of the readout chips. More sophisticated tests like threshold and noise measurements are done using the on-chip capacity and chopper to inject a known amount of charge in each pixel of the module. For a module usually an initial threshold dispersion of $1000 - 1200$ e^- at a threshold between $3000 - 4000$ e^- is achieved whereas the noise is typically about $270 - 290$ e^-.

To reduce the huge initial threshold dispersion to reasonable values a individual 5-bit threshold trim for each pixel is applied. The result of a threshold measurement of one module after such a tuning procedure can be seen in figure 4. The threshold of this module is tuned to a value of 3000 e^- in three steps: First for each readout chip the threshold is tuned next to the target value, then the chip-to-chip variation are equalized manually to achieve the same threshold for the whole module. Afterwards the individual chip threshold tuning is done again to minimize the threshold dispersion per chip. This leads finally to a module threshold of 3000 e^- with a dispersion of 120 e^-. The noise of the module is not affected by this tuning and remains at (280 ± 30) e^-. Both values, threshold dispersion and noise, are well below the requirement of about 400 e^- as quadratic sum of threshold dispersion and noise. Comparing these noise and threshold dispersion with single FE-I chips bump bonded to dedicated sensors no extra noise source for full modules can be seen.

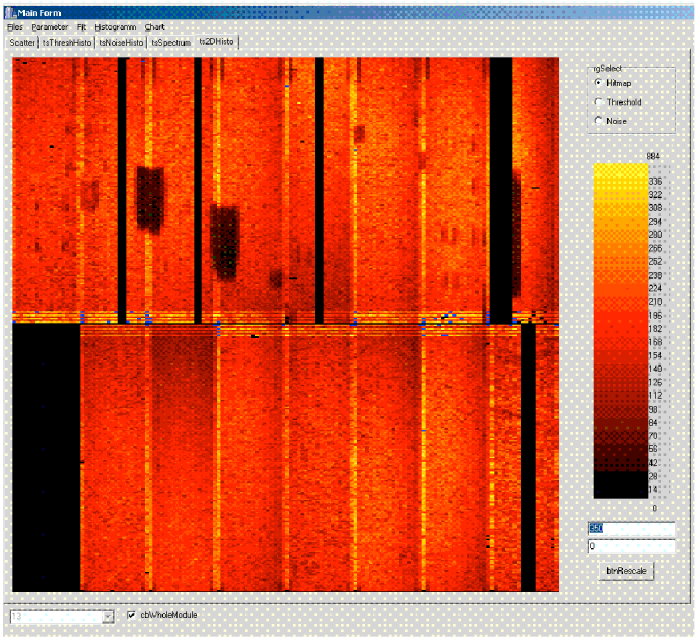

Figure 5: Source scan of tuned FE-I prototype module irradiated with Am^{241}.

To investigate the overall bumping yield and number of dead channels the above shown module was irradiate with a Am^{241} gamma source. A special self triggering circuit on the FE-I readout chip allows an easy and convenient way of such source tests without any extra trigger system. So a complete source scan of a whole module with sufficient statistics can be done in less than 4 hours. Masking out all the noisy channels of a module - in this case 9 noisy pixel has been turned off - a noise occupancy of better than 10^{-7} is achieved during the source scan. The result of this source scan can be seen in figure 5.

Altogether only 36 out of 41271 pixel don't see any hit. Most of these channels are located in regions where three big voltage decoupling capacitors on flex capton (see also figure 2) shadowing the penetrating gamma particles. Taking all the dead and noisy channels together this result corresponds to upper limit of the pixel efficiency of 10^{-3} per module which is acceptable for ATLAS pixel modules.

6 Conclusions

A pixel module design dedicated to the demanding requirements of operation in the ATLAS Inner Detector has been successfully developed and tested during the last years. This concept consists of a compact module with a n^+-n sensor bump bonded to 16 readout chips and a 2-layer flex capton glued to the backside of the sensor. A whole assembly process together with the needed tooling for a mass production of about 2000 modules during the next $2-3$ years have been installed within different institutes of the ATLAS pixel collaboration. Prototype modules demonstrate to meet the challenging electrical requirements like a low noise operation with a small threshold dispersion of all 48060 pixel. Also the modules show to cope with demanding mechanical requirements like robustness and thermal compliance due to low temperature operation.

References

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