



Token Bit Manager for the CMS Pixel Readout

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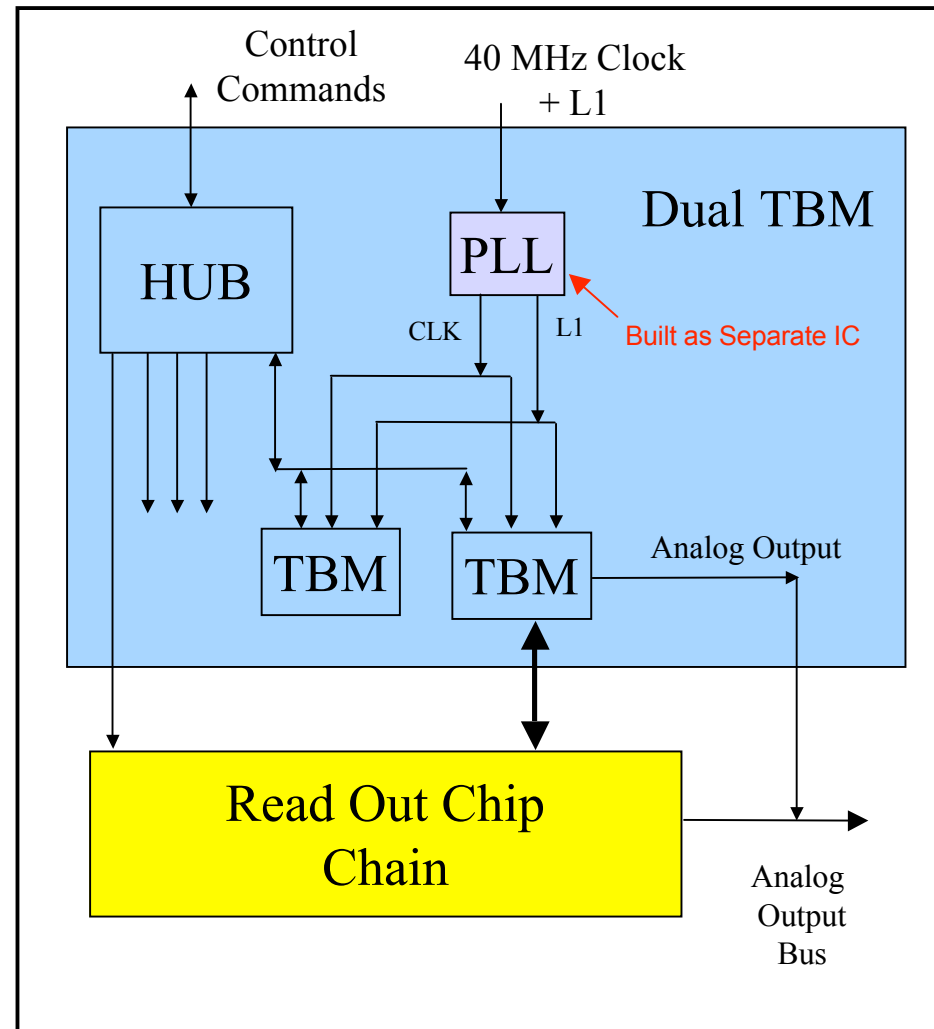
TBM Overview

- Orchestrate the Readout of Several Pixel Chips on a Single Analog Output Link
 - Write Header/Trailer Info in Data packet on Analog Output Link
- Custom, Mixed Mode, Rad-Hard, IC Mounted Near Pixel Readout Chips

Dual TBM Chip

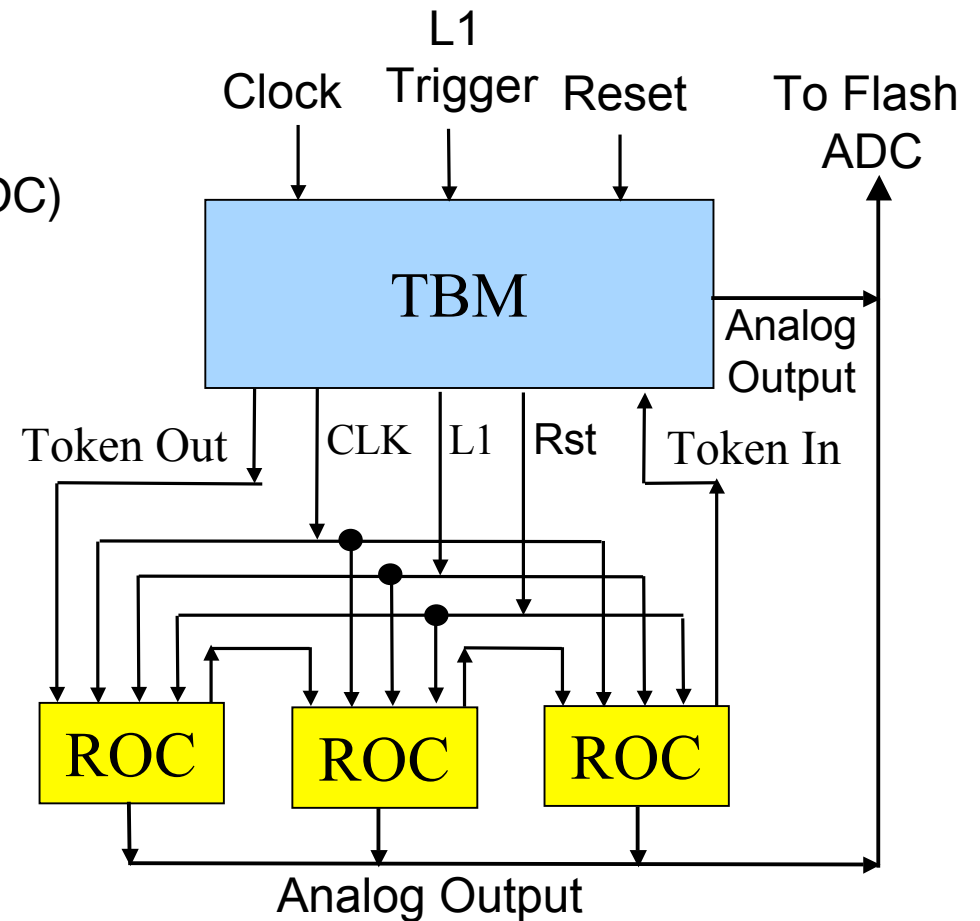
Dual TBM Chip

- Two Token Bit Manager's
 - Each TBM Controls one ROC Chain (4 to 24 ROC's per TBM)
- Control Network Hub
 - Port addressing for control commands
- Phase Locked Loop
 - Separates trigger and clock



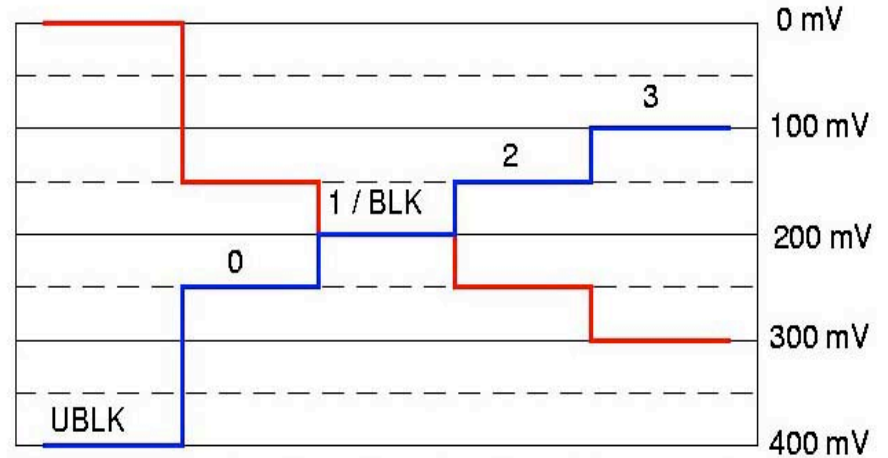
TBM Functions

- Write header and trailer (2 bit analog encoded digital)
 - 8 bit Event Number □ Header
 - 8 bit Error status word □ Trailer
- Distribute to Pixel Readout Chip's (ROC)
 - L1 triggers (2 Outputs/TBM)
 - Clock (2 Outputs/TBM)
 - Reset (2 Outputs/TBM)
- Control readout through token pass
- Stack triggers awaiting token pass
 - 32 event deep
 - No readout after 16 deep

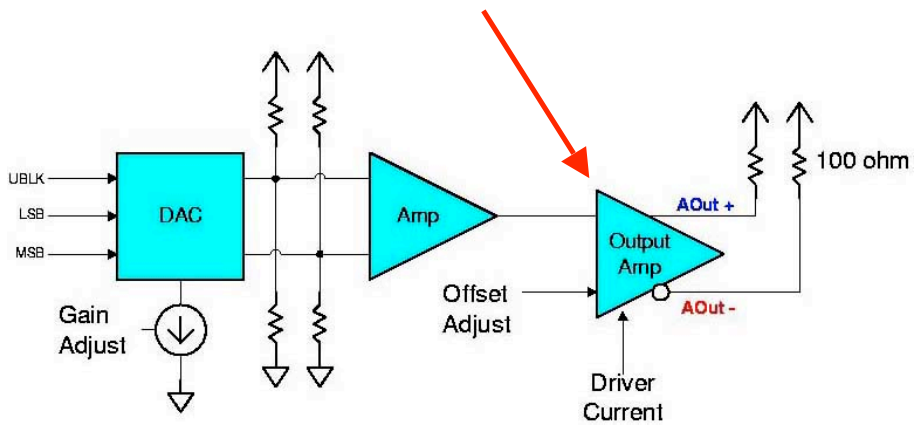


Analog Output

- Levels Chosen To Match ROC
- Output Levels Fully Adjustable
 - Gain Adjustment
 - Differential Offset Adjustment
 - Driver Current Adjustment
- Output Driver Identical to ROC



** Note: Voltage Levels are based on 4 ma driver current and 100 pull up resistors on analog output pins.



Signal	Differential Voltage
UBLK	-400 mV
0	-100 mV
1 / BLK	0 mV
2	+100 mV
3	+200 mV

I²C Control Features

- **Analog Adjustments**
 - Adjust Analog Levels
 - Disable Analog Output
- **Trigger Control**
 - Inject Any Trigger Type
 - Ignore Incoming Triggers
 - Disable Trigger Outputs
- **Token Passing**
 - Disable Token Passing
 - Reset Token Out
- **Stack Control**
 - Read Number of Events on Stack
 - Read Stack Contents (non-destructively)
- **General Control**
 - Switch Readout to 40 MHz or 20 MHz
 - Disable TBM Clock
 - Reset TBM

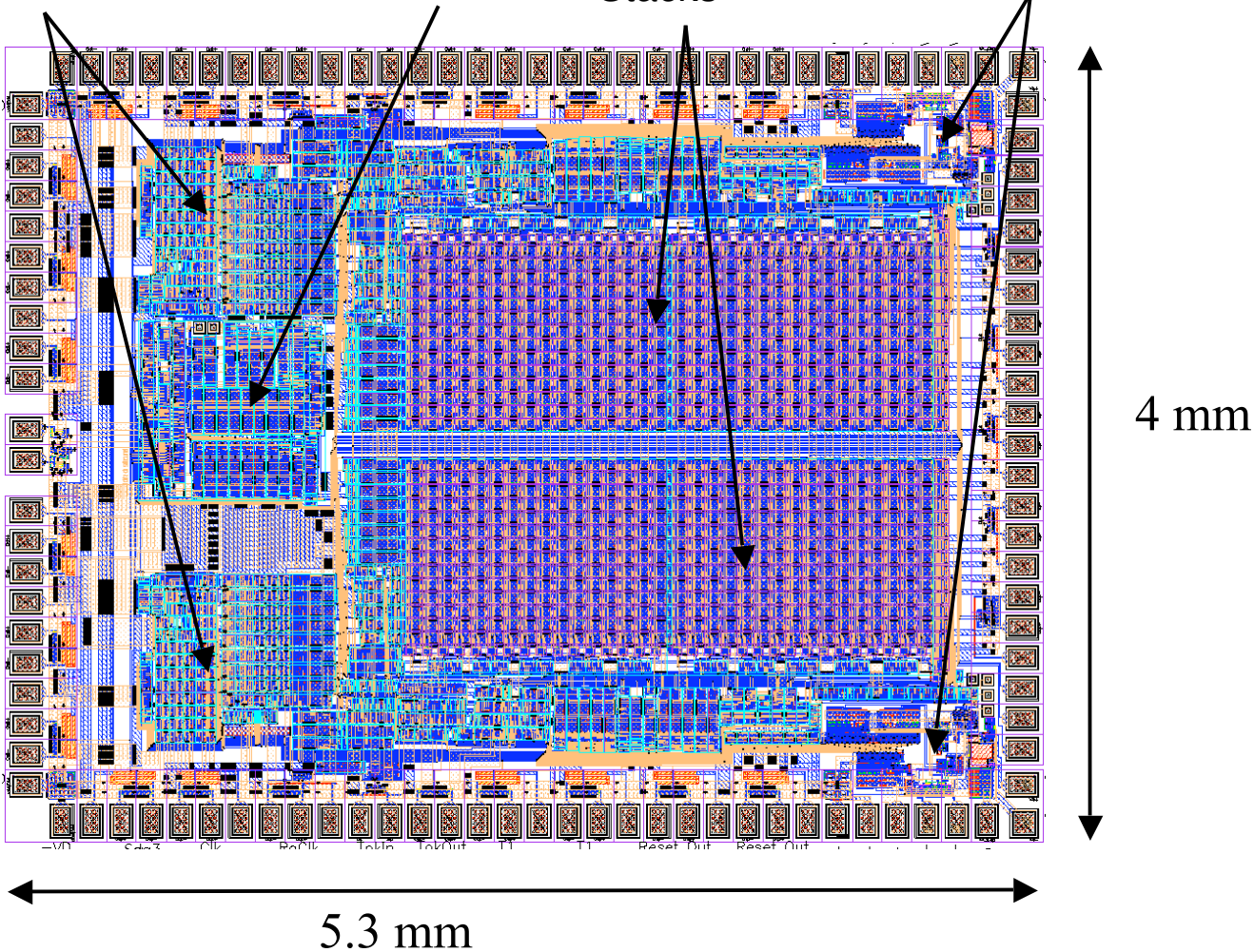
DMILL Dual TBM

Control sections

Hub

Stacks

Analog sections



TBM Test Fixture

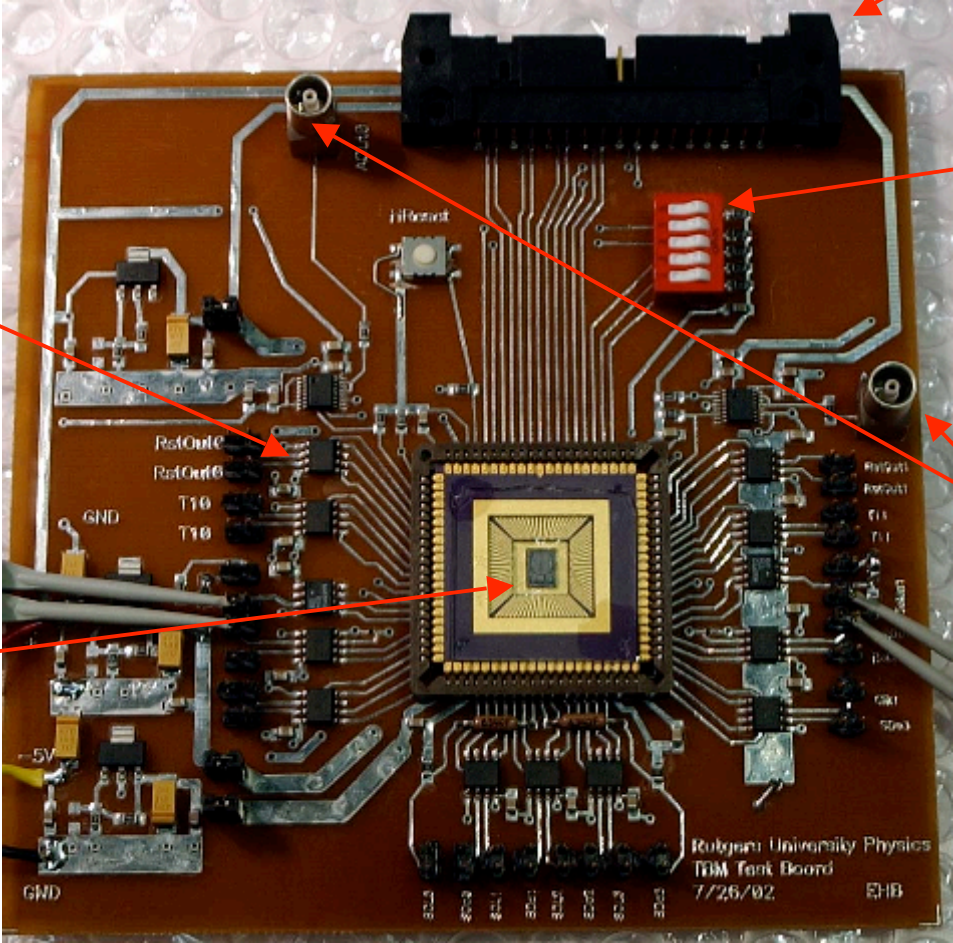
Computer Control
+ 40 MHz Clock + L1

Hub Address

Differential
Drivers
& Receivers

Analog Output
(Single Ended
50 ohm)

TBM



TBM Test Program

test31.tcl

Mode Help

Hub Address: 0 Token Bit Manager Select: TBM1 TBM2 Loop Read Read Stack

Disable Analog Output	Disable Trigger Out	Stack Readback Mode	Ignore Incoming Triggers	Pause Readout	Enable Auto Reset	Reset On Stack Count =24/32	Disable Token Passing	WRITE
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	READ
	Stack Empty	Stack Count Bit 5	Stack Count Bit 4	Stack Count Bit 3	Stack Count Bit 2	Stack Count Bit 1	Stack Count Bit 0	READ
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	READ
Stack D7 Event Num Bit 7	Stack D6 Event Num Bit 6	Stack D5 Event Num Bit 5	Stack D4 Event Num Bit 4	Stack D3 Event Num Bit 3	Stack D2 Event Num Bit 2	Stack D1 Event Num Bit 1	Stack D0 Event Num Bit 0	READ
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	READ
	Clear Token Out	Clear Stack	Hard Reset TBM	Inject PreCalibrate Trigger	Inject Reset Trigger	Inject Sync Trigger	Inject Normal Trigger	WRITE
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	WRITE
Disable TBM Clock	40/20MHz Readout	Stack D13 No Token Pass	Stack D12 Sync Trigger	Stack D11 Sync Error	Stack D10 Reset	Stack D9 Stack Full	Stack D8 PreCalibrate Trigger	READ
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	READ
Disable TBM CLK	40/20MHz Readout							WRITE
<input type="checkbox"/>	<input type="checkbox"/>							WRITE

Reset Analog Registers to Nominal

Differential Offset Voltage adjustment 128

0 50 100 150 200 250 WRITE

Analog Output Gain Adjustment 128

0 50 100 150 200 250 WRITE

Analog Output Driver Current 128

0 50 100 150 200 250 WRITE

SCI output:

SDa output:

SDa input:

Fast Trigger:

VIcolOr (uA) 420 Set

ReadOut:

VBias_sf (uA) 32.0 Set

VnPix (uA) 49.4 Set

VoffsetOP (V-) 2.20 Set

VSumCol (uA) 126.0 Set

Calibration:

Vcal (offset to vee) 0.948 Set

CalDel (uA) 0.0 Set

Digital Registers:

40MHz Readout Speed:

DAQ Stop:

Set ctrl_reg

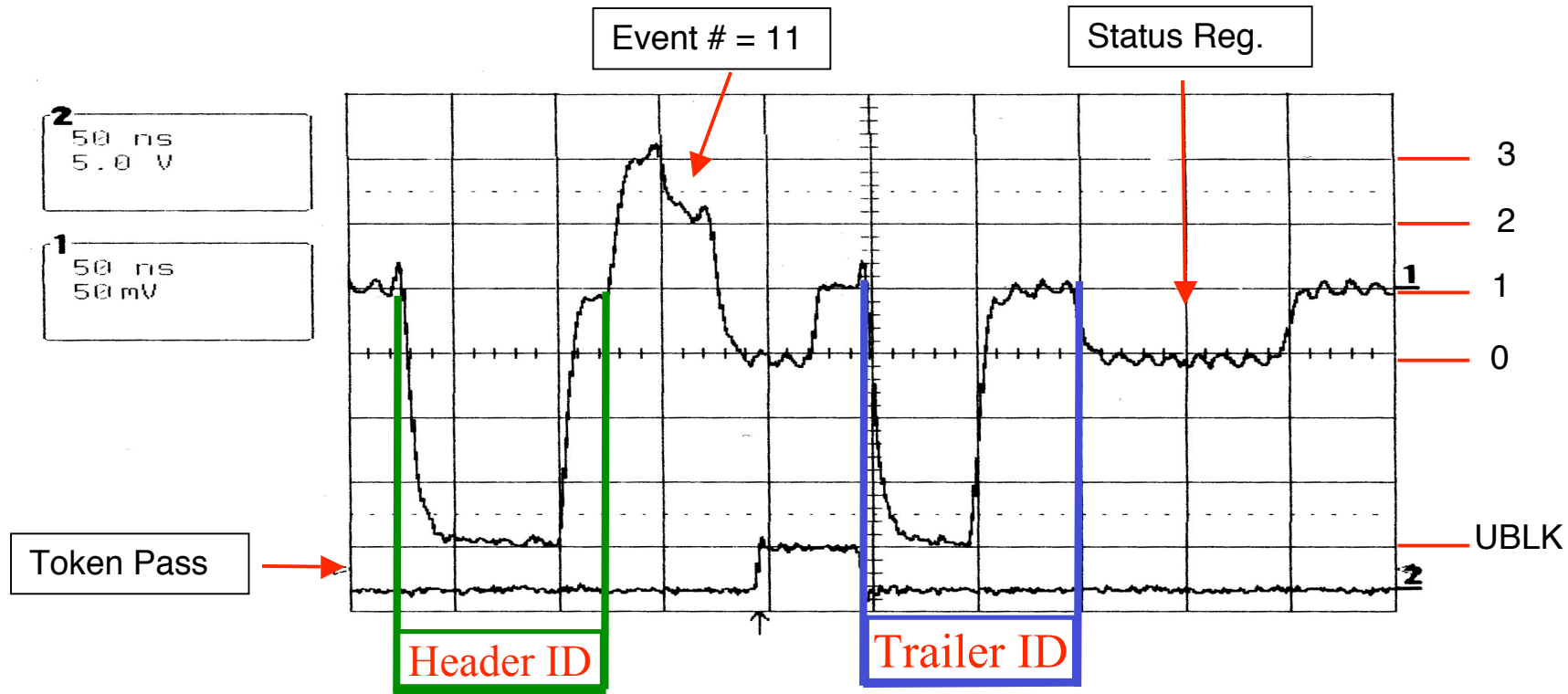
WBC (trigger latency): Set WBC

0 + - Reset Inject

Dismiss window

Set DAC values

TBM Test Results



- Header marker 3 "UBLK" + "1"
 -8 Bit Event Number (4 Clocks)
- Trailer marker 2 "UBLK" + 2 "1"
 -8 Bit Status Word (4 Clocks)

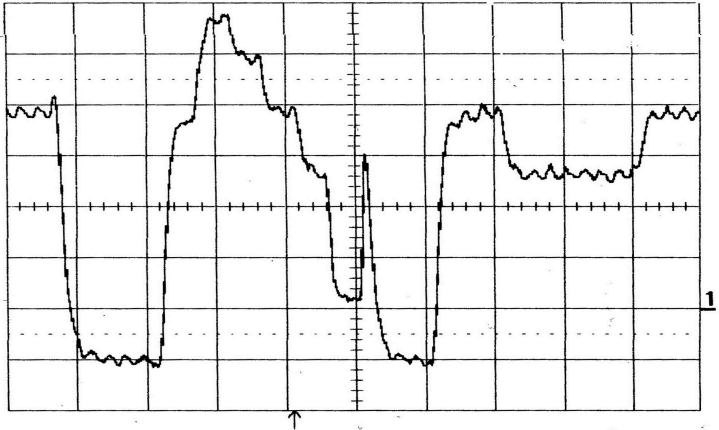
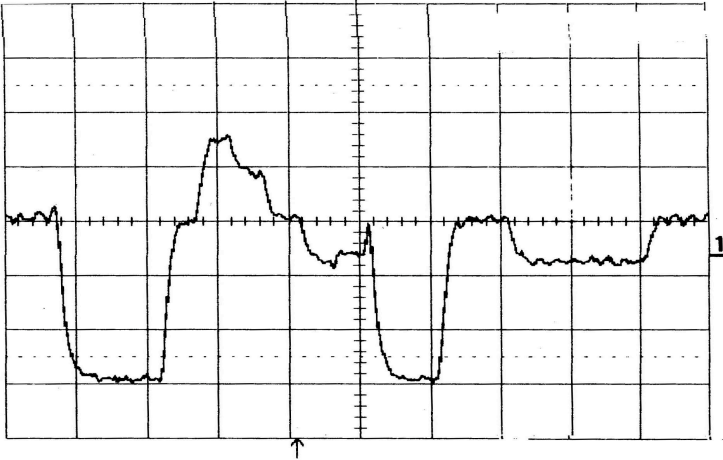
- Power consumption 600 mW
 -core 140 mW
 -Differential Drivers 460 mW
- 6 Tested / 5 Fully Functional

Analog Adjustability

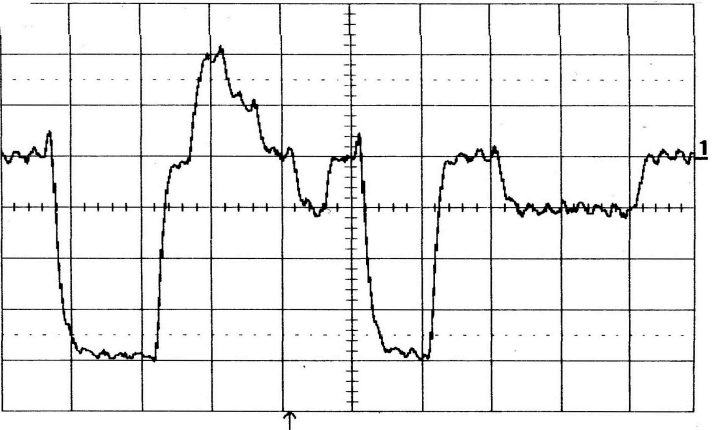
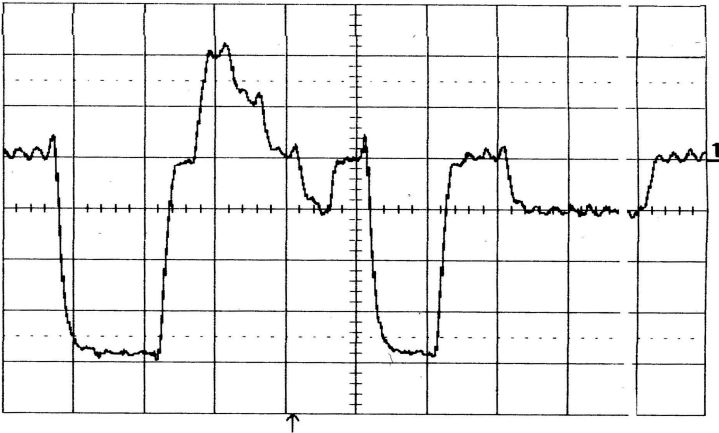
TBM 1

TBM 2

Before Adjustment

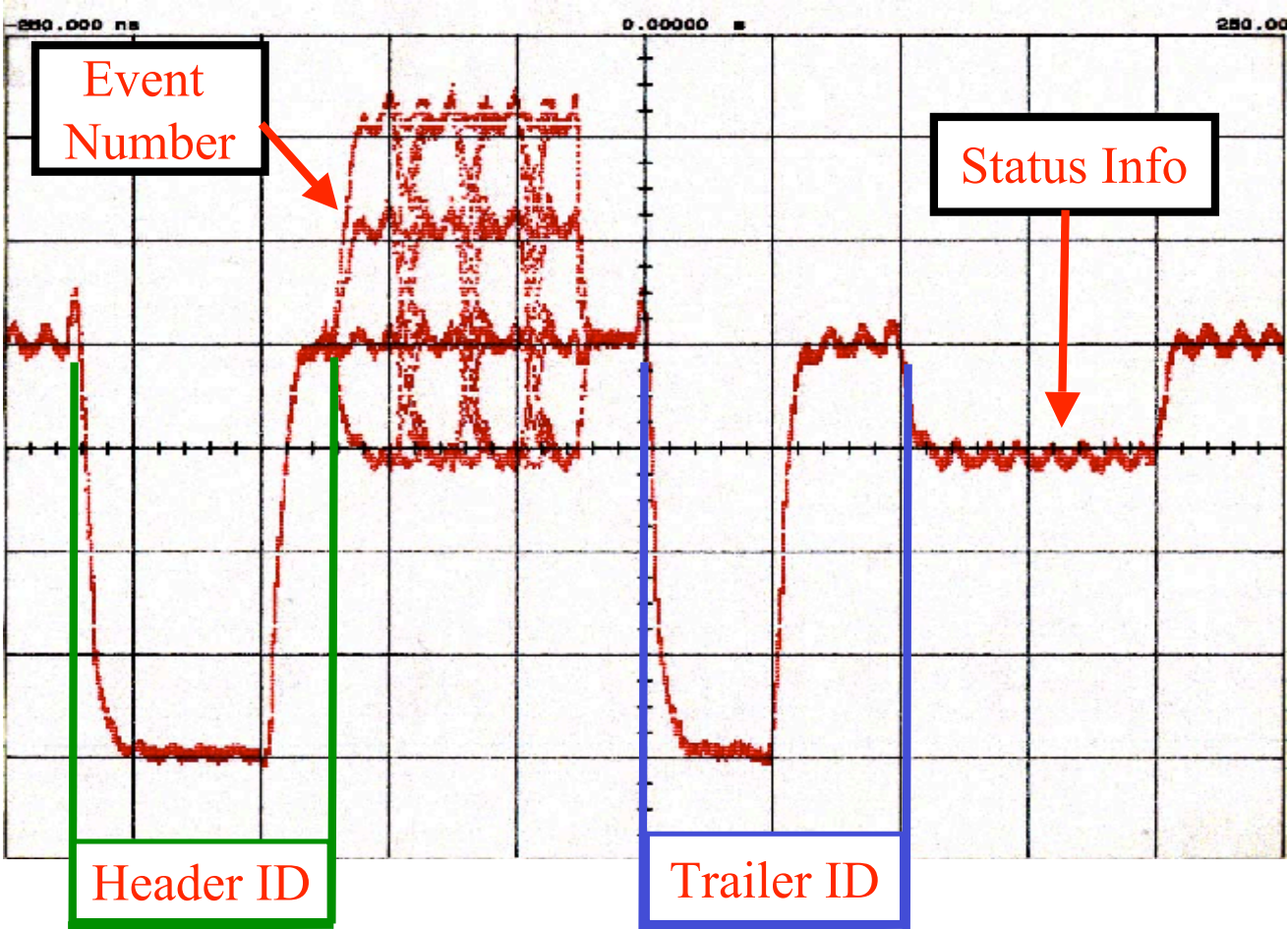


After Adjustment



1 MHz Trigger Rate

Expected Max CMS Trigger Rate = 100KHz

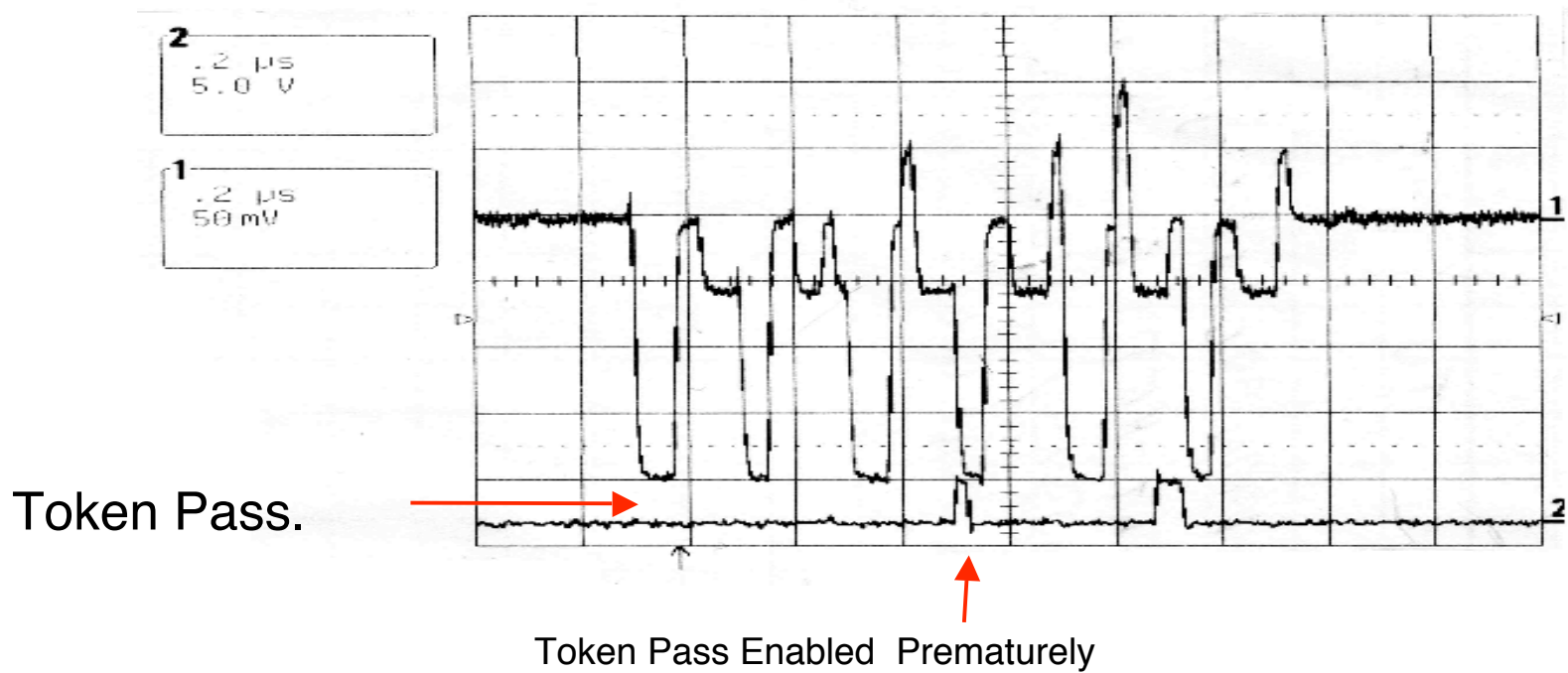


One Problem

Minor Glitch: Token Control Circuit.

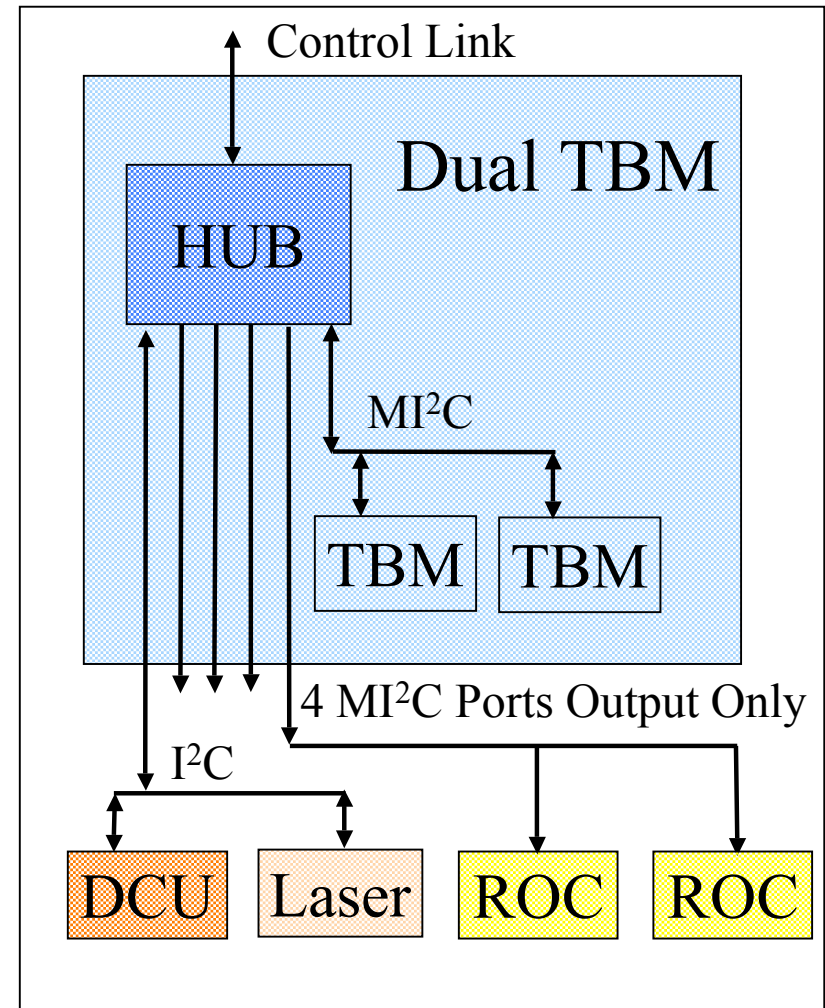
Result: Premature Reload of Trailer Status Output Reg. when multiple events on stack.

Fix: Addition of two transistors (2 input Or \square 3 input Or).



Control Network Hub

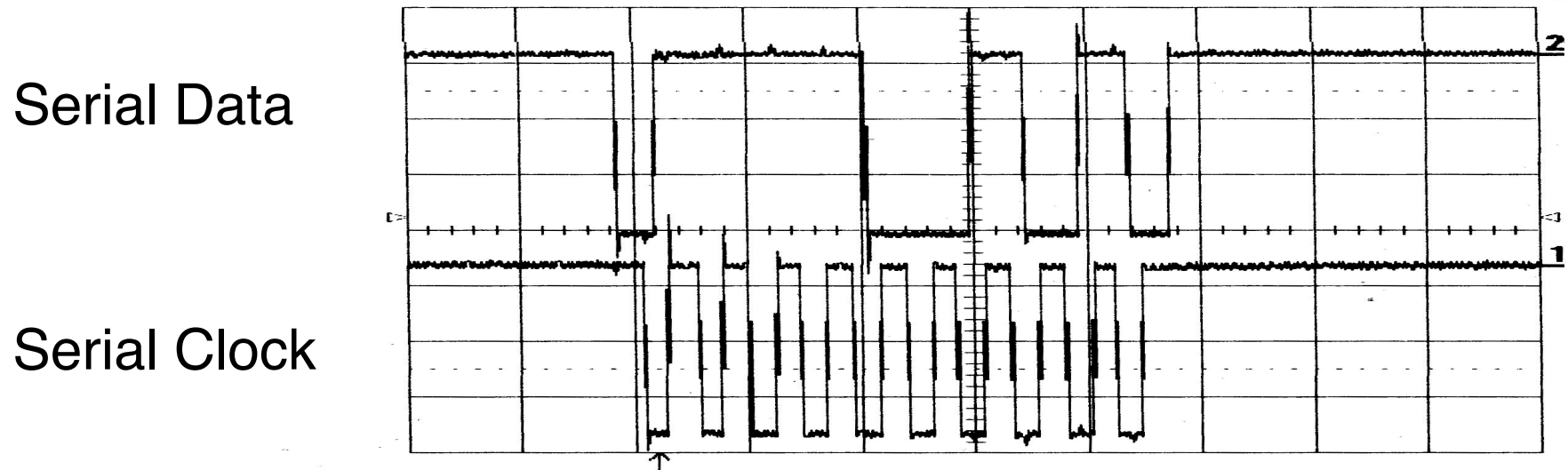
- Up to 32 hubs addressable.
- 6 Ports per hub.
 - 4 MI²C (40 MHz) external □ ROC's.
 - 1 MI²C (40 MHz) internal □ TBM's.
 - 1 Standard I²C (310 kHz) external.
- Functions of addressed hub.
 - Selects addressed port.
 - Selects fast/slow clocking depending on port.
 - Strips off byte containing hub/port address. Passes remainder.
 - Reflects data back to Front End Controller.



Hub Testing

- Internal fast port - fully tested and functional
- External fast ports - fully tested and functional
- External slow port - yet to be tested

MI²C Command Output From Port 0



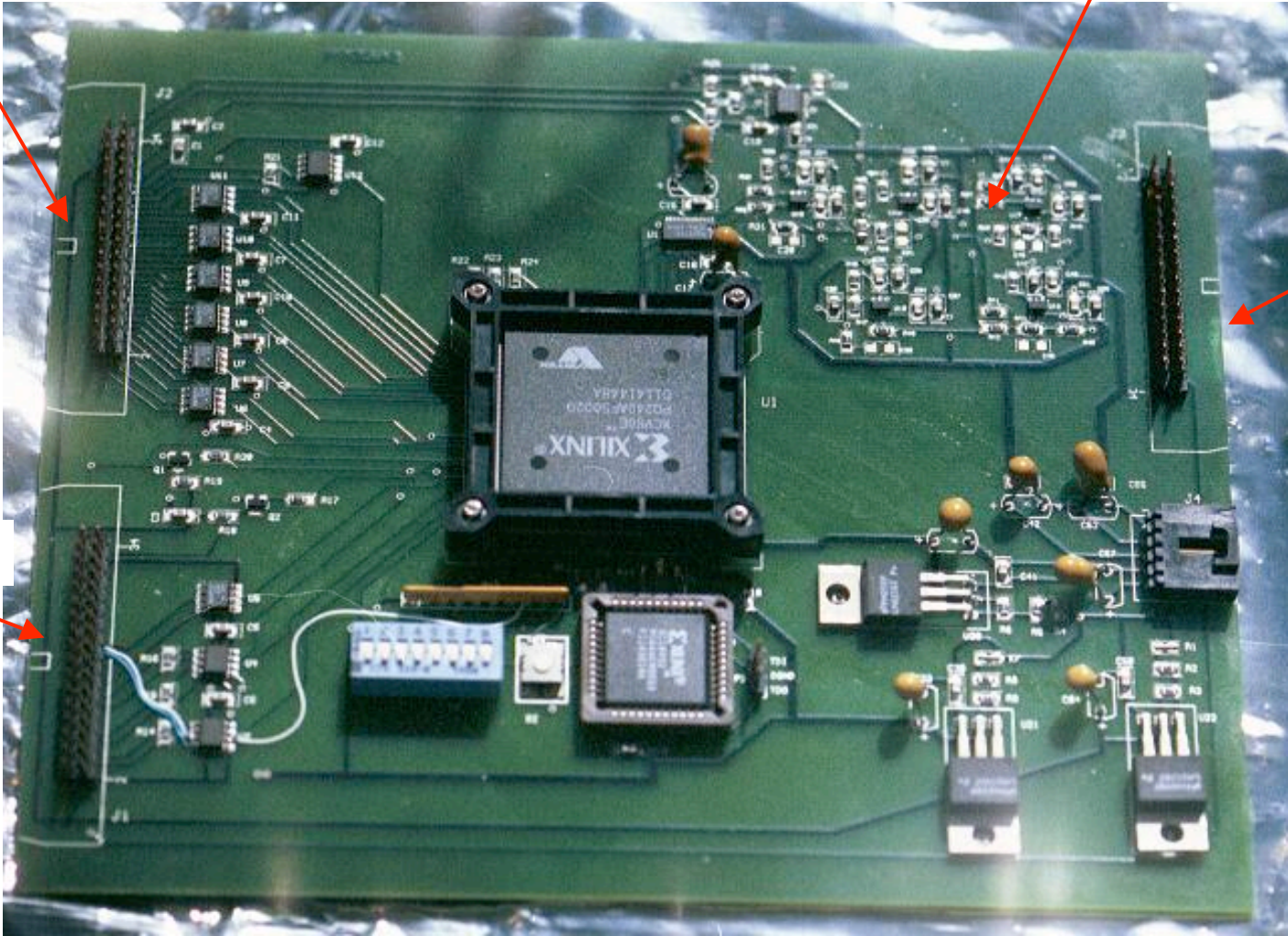
FPGA TBM

To Readout Chip

Analog section

To DAQ

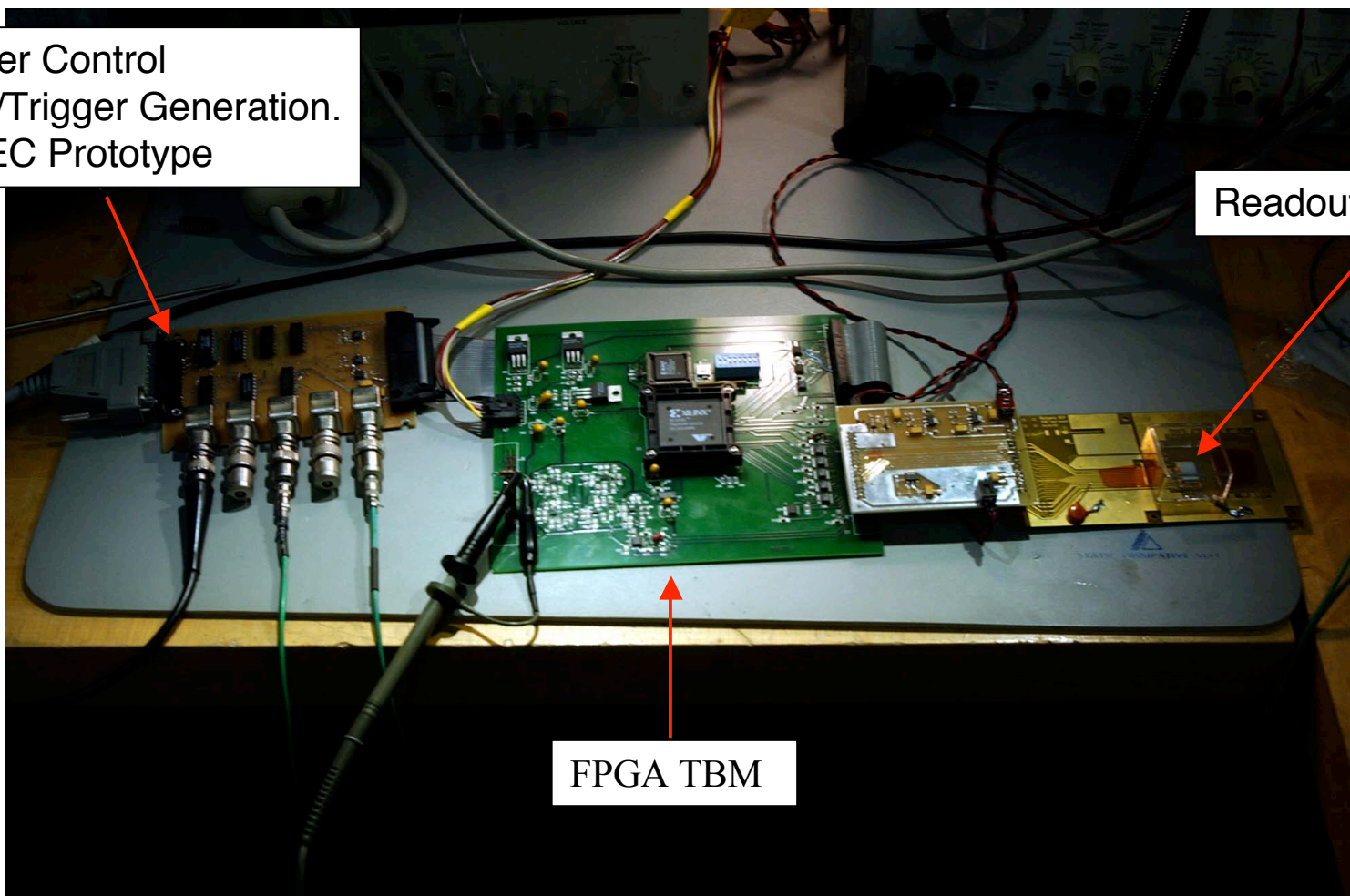
To FEC



ROC Test Setup

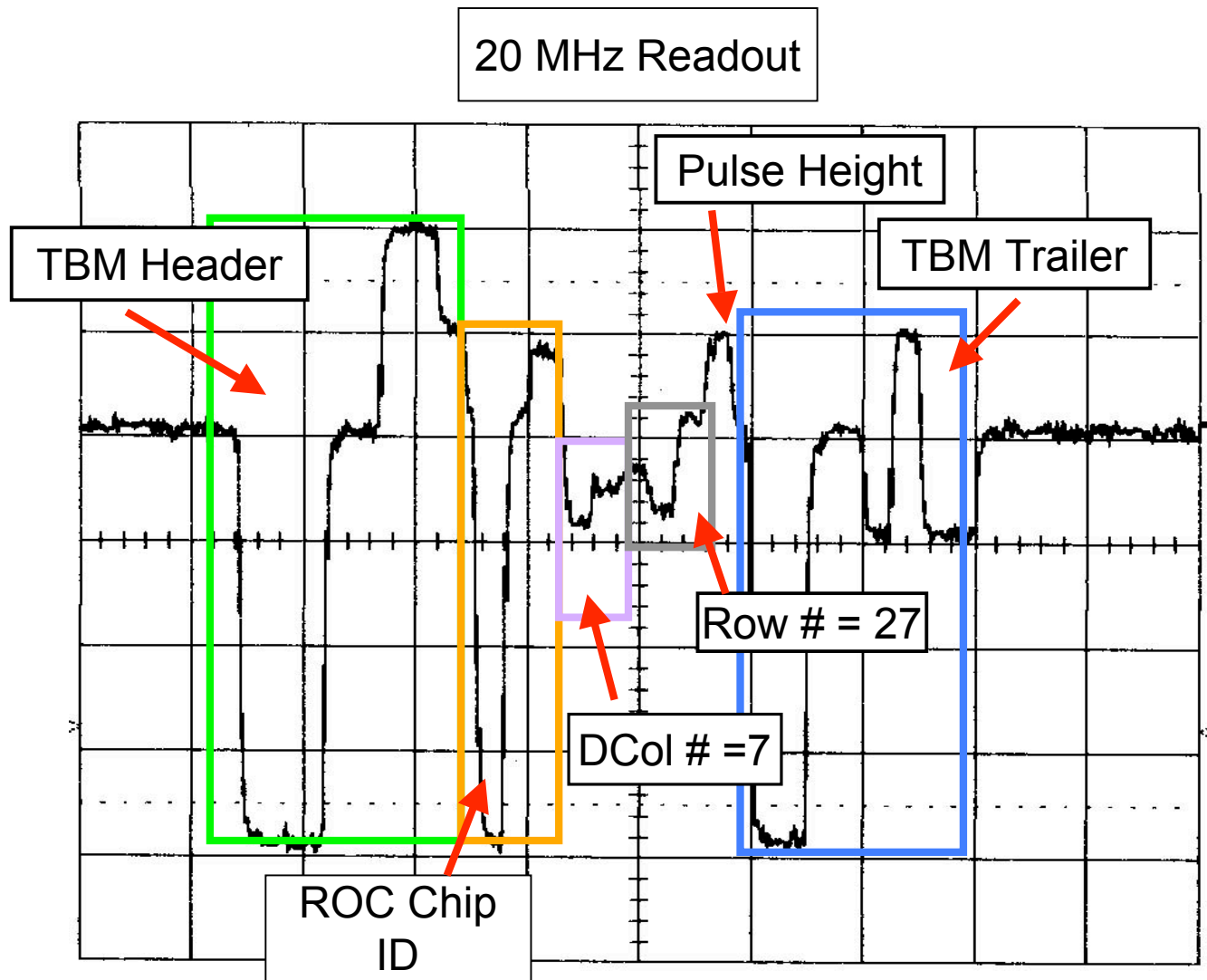
Computer Control
& Clock/Trigger Generation.
Early FEC Prototype

Readout Chip

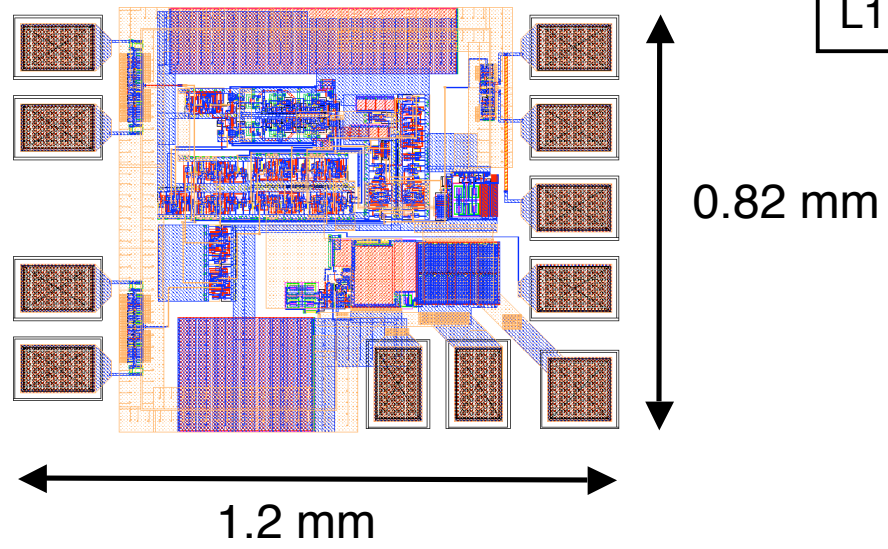
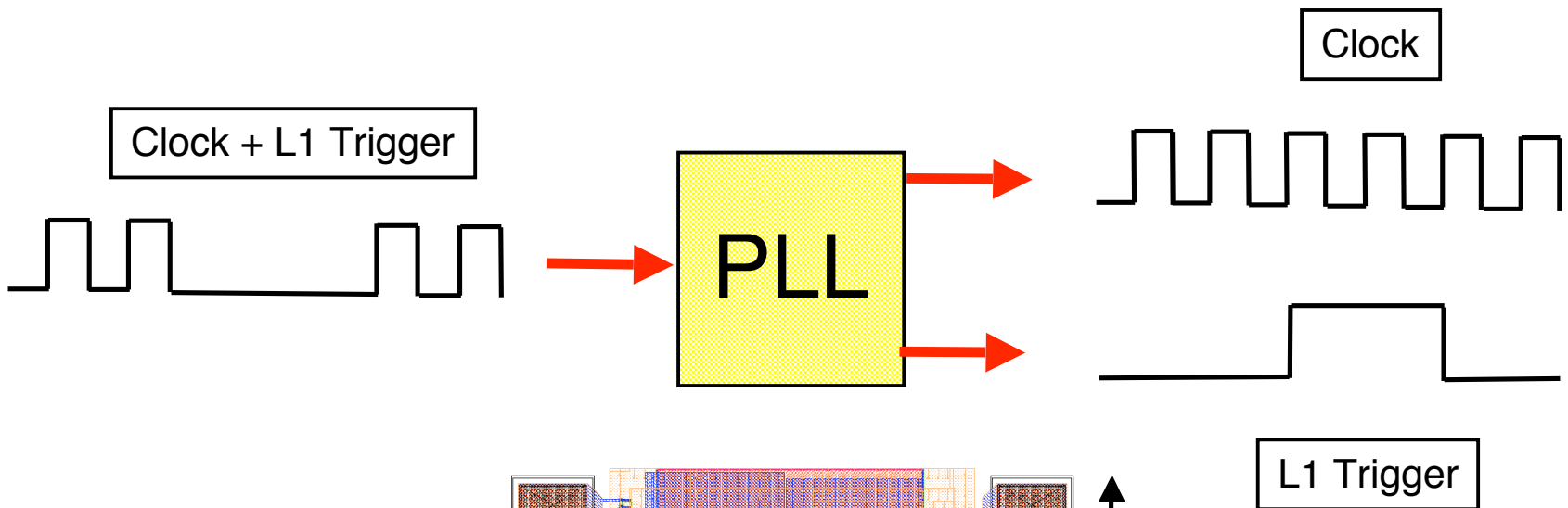


FPGA TBM

Single Pixel Calibration Pulse

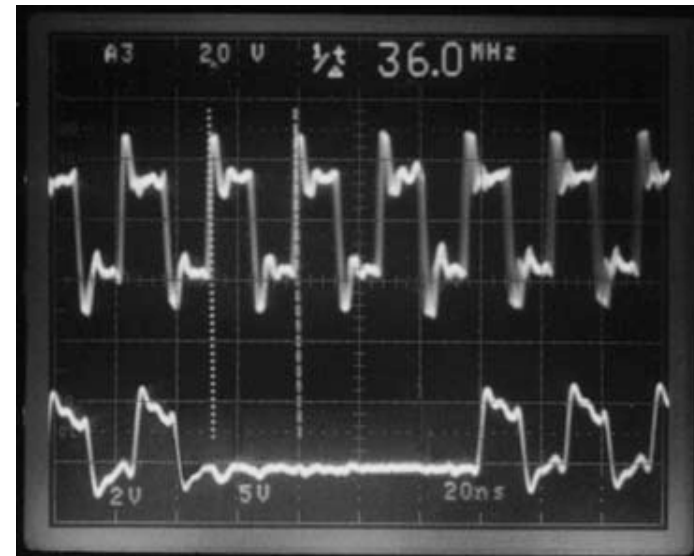


Phase Locked Loop



PLL Test Results

- Clock recovery.
 - locking range low.
 - 27 MHz to 33 MHz @ 20 deg C
 - 30 MHz to 36 MHz @ -3 deg. C.
 - likely due to weak current sink.
- Trigger recovery.
 - works for all trigger types.
- Jitter.
 - ± 1.8 ns @ 26 MHz.
 - ± 1.0 ns @ 30 MHz.
 - ± 0.7 ns @ 33 MHz.



Output

Input

• 3 1/2 weeks from start of conceptual design to submission
• Some problems but basically works

Conclusion

- Dual TBM and PLL work on first DMILL submission
- Future Plans
 - Translate designs to 0.25 μ m (Matching ROC Translation)
 - Redesign Slow I²C Port For CMS Optical Transceivers.
 - Improve Phase Lock Loop Design
 - Minor system level revisions.
 - Reduce Power Consumption
 - Include Analog Output Line Driver