The Token Bit Manager Chip for the CMS Pixel Readout

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1 Introduction

The Token Bit Manager (TBM) is an critical element of the front-end readout for the CMS pixel detector. It is a custom, mixed-mode, radiation-hard IC that controls and orchestrates the readout of a group of ReadOut Chip (ROC's). The TBM is designed to be located on the detector near to the pixel ROC's. In the case of the barrel, they will be mounted on the detector modules and will control the readout of 8 or 16 ROC's depending upon the layer radius. In the case of the forward disks, they will be mounted on the disk blades and will control the readout of 21 or 24 ROC's depending on blade side. [1] A TBM and the group of ROC's that it controls will be connected to a single analog optical link over which the data will be sent to the Front End Driver, a flash ADC module located in the electronics house.

The relationship of the TBM to the group of ROC's it controls is shown in Figure 1. The principle functions of the TBM include the following.

- It will control the readout of the ROC's by initiating a token pass for each incoming Level 1 trigger.
- On each token pass, it will write a header and a trailer word to the data stream. The header will contain an 8-bit event number and the trailer will contain a 8-bits of error status. These will be transferred as 2-bit analog encoded digital.
- It will distribute the Level 1 triggers, clock and resets to the ROC's.
- Each arriving Level 1 trigger will will be placed on a 32-deep stack awaiting its associated token pass. Normally the stack will be empty but is needed to accommodate high burst rates due to either noise, high track density events or trigger bursts.

Since there will be two analog data links per module for the inner two layers of the barrel, the TBM's will be configured as pairs in a Dual TBM Chip. A block diagram of the Dual TBM chip is shown in Figure 2. In addition to two TBM's, this chip also contains a Control Network Hub and a Phase Lock Loop (PLL).

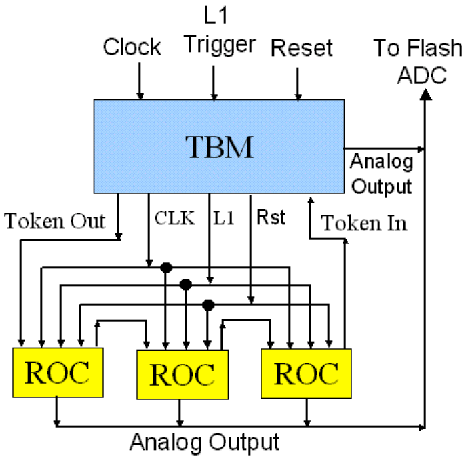


Figure 1: Schematic of a readout chain consisting of a TBM and and a group of ROC's.

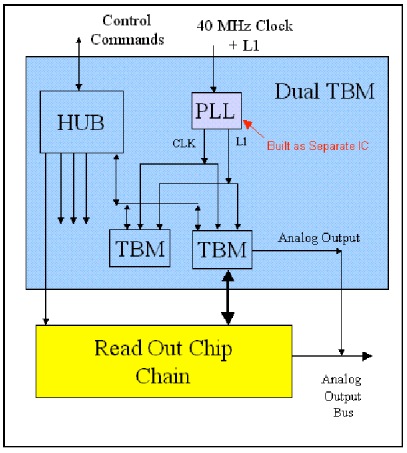


Figure 2: Block diagram of the Dual TBM chip.

The Hub serves as a port addressing switch for control commands that are sent from the DAQ to the front-end TBM's and ROC's. These control commands will be sent over a digital optical link from a Front End Controller (FEC) in the electronics house to the front-end hubs. The commands will be sent using a modified I^2C protocol [2] with a clock speed of 40 MHz. This high speed is mandated by the need to rapidly cycle through a refreshing of the pixel threshold trim bits that can become corrupted due to single event upsets. There are four external ports on each Hub for communicating with the ROC's and there is one internal port for communicating with the TBM's within the chip. The first byte of each command will contain a 5-bit hub address and a 3-bit port address. When a Hub is addressed, it selects the addressed port, strips off the byte containing the hub/port address and passes the remainder of the command stream unmodified onto the addressed port. The outputs of the external ports are on two low voltage differential lines for sending clock and data.

In CMS the Level 1 triggers will be encoded in the clock signal as dropped clock pulses ensuring that the correct phase relation between clock and trigger is maintained. Three clock cycles (75 ns) are available for each trigger allowing for up to four types of triggers to be encoded. A phase lock loop circuit is will be incorporated into the Dual TBM chip for separating out the Level 1 triggers from the clock and and for restoring the missing clock pulses.

2 The Dual TBM Prototype

Although the production Dual TBM chip that will be used in CMS will be built in a 0.25 deep submicron process, for the first prototype of the TBM has been produced in the 0.8 micron, SOI, radiation-hard, DMILL process [3]. This follow in parallel with the development of the PSI43 ROC chip [4] which was a joint part of this submission. Figure 3 shows the layout of the Dual TBM chip. In this submission the PLL was produced as a separate chip.

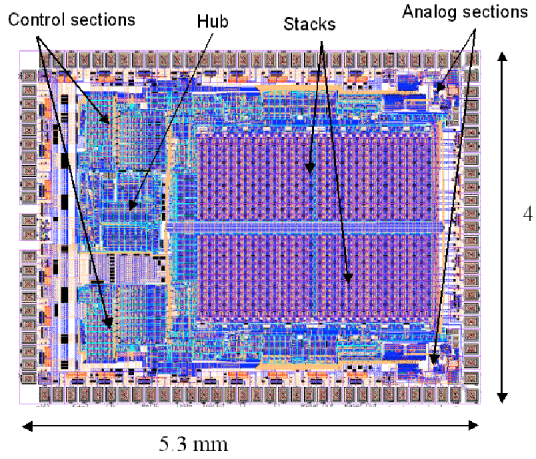
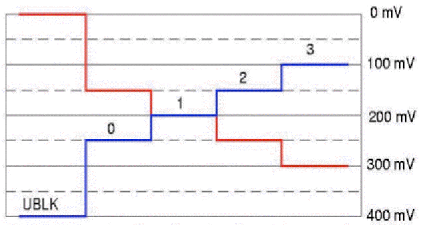


Figure 3: Layout of the Dual TBM chip.



Signal	Differential Voltage
UBLK	-400 mV
0	-100 mV
1	0 mV
2	+100 mV
3	+200 mV

Figure 4: Output levels of the Dual TBM chip.

Although the Dual TBM is predominantly a digital chip, an analog section is needed for writing the header and trailer information to the analog output. The analog output uses four levels of information and an additional "ultrablack" level that marks the start of the header and trailer. The output levels produced are shown in Figure 4. They are chosen to match the corresponding levels produced by the ROC's. (Note, the ROC's will produce six levels of analog information plus an ultrablack. The TBM uses only the lower four levels.)

It is essential to have full adjustability of the analog output levels, since there may be large chip-to-chip variations in the production TBM chips. Also, the TBM output levels should be aligned to the corresponding levels of the readout chips that are connected to the same analog line. The Dual TBM analog output stage in shown in Figure 5. It is driven by a multiplying DAC whose gain can be adjusted by a current source. This is followed by a buffering amp and then by a differential driver. The differential driver has both an adjustable offset and a driver current adjustment. In combination, these three adjustments allow for setting of : the offset, gain and the differential zero crossing of the differential output.

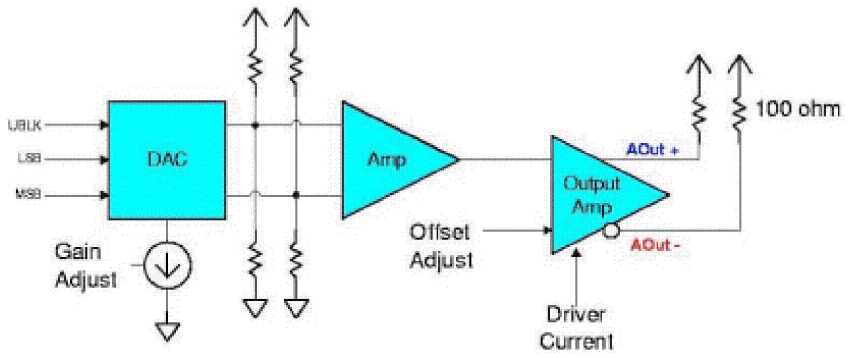


Figure 5: Analog output section of the Dual TBM chip.

An extensive set of control commands have been built into the TBM. These allow various functions and operating modes of the TBM to be controlled by issuing commands to the TBM over the control network described above. The more important of these commands are:

- Analog adjustment
  - adjustment of the analog levels described above
  - enabling and disabling the analog output
- Trigger Control
  - injection of any trigger type
  - ignoring of incoming triggers
  - enabling and disabling of the trigger output
- Token Passing
  - enabling and disabling of the token passing
- Stack Control
  - read back of the number of events on the stack
  - readback (non-destructively)of stack contents
- General Control
  - switching of the readout speed between 40 MHz and 20 MHz
  - enabling and disabling of the TBM clock
  - rest TBM

3 Results

The DMILL Dual TBM prototype was delivered in May 2002. The functionality of several of the delivered chips have been fully tested. Figure 6 shows the measured response of the DMILL TBM operating at the full readout clock speed of 40 MHz upon receipt of a trigger. When the trigger is received, the TBM outputs a header ID

consisting of three "ultrablack" levels followed by a "1". The next four clocks contain an 8-bit analog-encoded event number. In the case of the event shown in the figure, the particular event number is 11. Following the header, the TBM issues a token to the first ROC on the readout chain. The ROC's would then place their ID and any hit information onto the data stream and pass the token along. Since in the present test there were no ROC's connected to the TBM, the token is immediately returned to the TBM. Upon receipt of the returned token, the TBM outputs a trailer ID which consists of two "ultrablack" levels followed by two "1"'s. The next four clocks contain an 8-bit analog-encoded error status word. In these tests, we have determined that the event number is correctly incremented and reported in the header. In addition, all of the status bits in the trailer are correctly set and cleared. Six Dual TBM chips have been tested. Of these, five are fully functional while one has a dead short somewhere in the power lines of the chip.

Figure 6: Header and Trailer output for a typical event.

In the case of the barrel modules, the Dual TBM chip will be located on a hybrid that sits on top of the pixel sensors. The heat generated by the TBM will have to pass through the sensors before reaching the cooling structure. The power consumption of the Dual TBM chip is, therefore, of concern for the barrel application. The present chip consumes 600 mW of power. Of this, 460 mW is consumed by the differential drivers that are used for distributing the clock, Level 1 triggers, resets and token. The remaining 140 mW is consumed by the "core" of the TBM. When the TBM is translated to a 0.25 micron process, there will be an automatic reduction of the driver power by a factor of two due to the halving of the supply voltage. In addition, the voltage swing of the drivers will be reduced. In the current, prototype they are ± 400 mv into 100 ohms. The size of this reduction and the total number of drivers required will be determined by tests performed on multiple ROC's attached to a hybrid prototype. Also, in the 0.25 micron prototype, more attention will be paid to power consumption in the TBM "core" as well.

The adjustment of the TBM analog outputs works very well. The need for this adjustability along with the capability is demonstrated in Figure 7. The top two plots show the outputs of two TBM's before any adjustment is made. The chip-to-chip variation is clearly very pronounced. The lower two plots show the outputs after adjustment. They are very well matched.

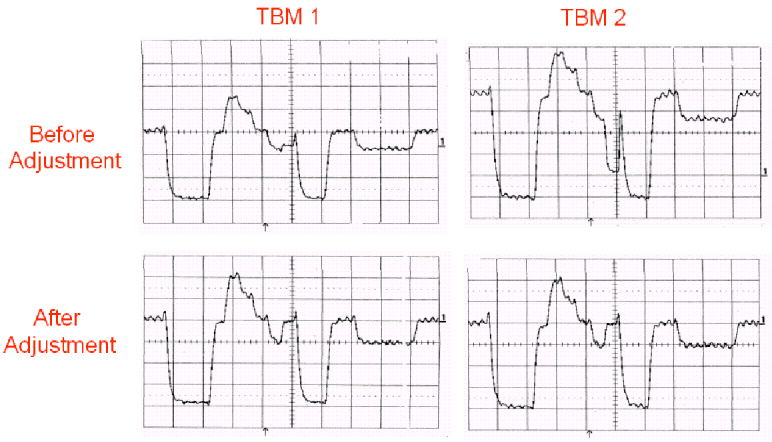


Figure 7: Adjustability of the analog output levels.

In order to see how far beyond design specifications the chip could be run, it was tested with an input trigger rate of 1 MHZ. This far exceeds design requirements since, in normal running, the CMS Level 1 trigger rate will be 30 KHz with possible brief bursts to 100 KHz. Figure 8 shows the output of a TBM chip for a 1 MHz input trigger rate. In this figure, multiple traces for several outputs have been overlaid. The TBM clearly is able to function at this trigger rate. The whole range of 256 event numbers is seen in the header output while the other features: header ID, trailer ID and error status word are indistinguishable from event to event.

The internal fast port that communicates with the TBM's and the four external fast ports that communicate with the ROC's have also been fully tested and found to be fully functional.

In all respects, the Dual TBM prototype chip fully functions as designed at at the full clocking speed of 40 MHz. The one exception is a minor glitch in the the token control circuit. If there are multiple events on the stack, then the token passing is enabled prematurely. The fix is an addition of two transistors that change a 2-input OR into a 3-input OR. This will be incorporated in future prototypes.

The PLL is a small but sophisticated circuit. Initially, we had decided to include the PLL in the succeeding prototype submission. However, because we had an extra month before the submission, we decided to design the PLL and include it as a separate chip. In less than one month, the chip was carried from conceptual design

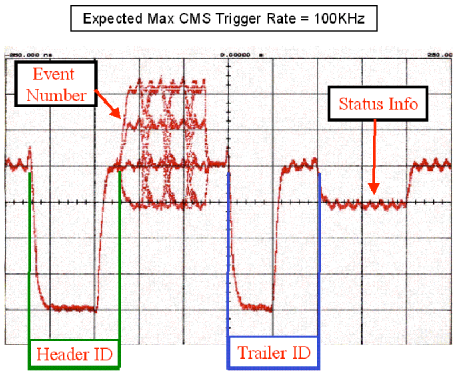


Figure 8: Performance of Dual TBM chip at an input trigger rate of 1 MHz. Outputs of several events are over lain.

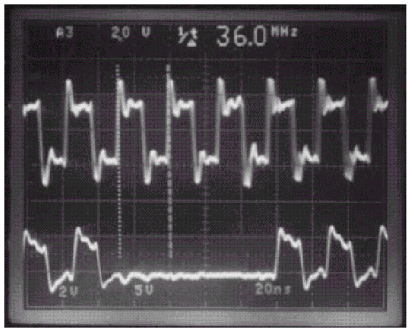


Figure 9: Scope trace of the input and output of the PLL chip demonstrating clock recovery.

to submission. The basic functions of produced chip work although they are slightly below design specifications. The trigger recovery works for all trigger types. The case of a trigger type involving three dropped clocks is shown in Figure 9. The trigger is extracted and the clock recovered for this and for all other trigger types. The one problem with the chip is that the clock recovery only locks over a frequency range lower than the 40 MHz design. The locking range is 27 MHz to 33 MHz at 20^o C and 30 MHz to 36 MHz at -3^o C. This is likely due to a weak current sink that will be fixed in the next submission. The jitter of the recovered clock is good but should be improved. The measured jitter is ± 1.8 ns at 26 MHz, ± 1.0 ns at 30 MHz and ± 0.7 ns at 33 MHz.

4 Future Plans

The Dual TBM chip works as designed on the first DMILL submission. In the coming year we will build on this work to produce the next prototype version. In parallel with the pixel readout chip, the Dual TBM chip will be translated into a 0.25 micron process. Relative to DMILL, this process should result in a chip that is more radiation-hard, consumes less power and have higher yield. We estimate that this translation will require about one year and two prototype iterations. The final chip in the 0.25 micron process should be available by the end of 2003.

In addition to the 0.25 micron translation, several other modifications will be made. The PLL design will be improved and the circuit incorporated into the TBM chip. Several minor system level revisions will be made. The power consumption

will be reduced through a reduction] in the number and in the voltage swing of the differential drivers.

In addition, there will be a need for an analog line driver for driving the analog signal over the approximately 50 cm distance from the detector to the optical components located on the service cylinder. A logical place for this line driver would be in the Dual TBM chip. In that case the analog outputs from the ROC would be sent to the TBM chip where they would be buffered and then sent out on the analog line. In this way only the TBM chip itself would be directly connected to the analog line.

References

[1] "The CMS Tracker Technical Design Report," CMS/LHCC 98-6.

[2] "I^2C Bus Specification," Application Note, Philips-Signetics, January (1992).

[3] M. Dentan *et al.*, "Dmill (Durci Mixte Sur Isolant Logico-Lineaire): A Mixed Analog-Digital Radiation Hard Technology For High Energy Physics Electronics," Nucl. Phys. Proc. Suppl. **32**, 530 (1998).

[4] W. Erdmann, "The DMILL Readout Chip for the CMS Pixel Detector," These Proceedings.