# Active Pixel Sensor Architectures in Standard CMOS Technology for Charged-Particle Detection

D. Passeri[1,2], P. Placidi[1,2], L. Verducci[1,2], G.U. Pignatel[1,2]
P. Ciampolini[3], G. Matrella[3], A. Marras[3], G.M. Bilei[1]

(1) Istituto Nazionale di Fisica Nucleare
Sezione di Perugia - Italy

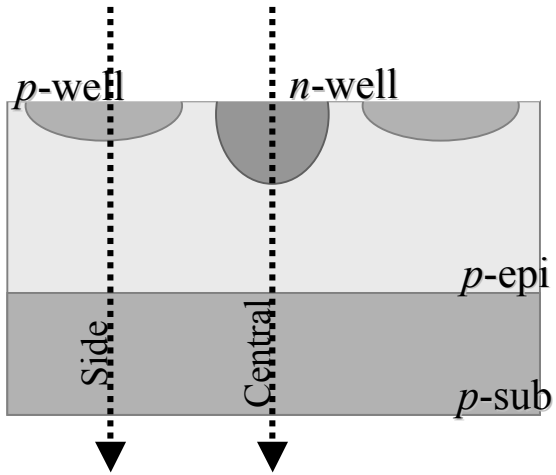
(2) Dipartimento di Ingegneria Elettronica e dell'Informazione
Università degli Studi di Perugia - Italy

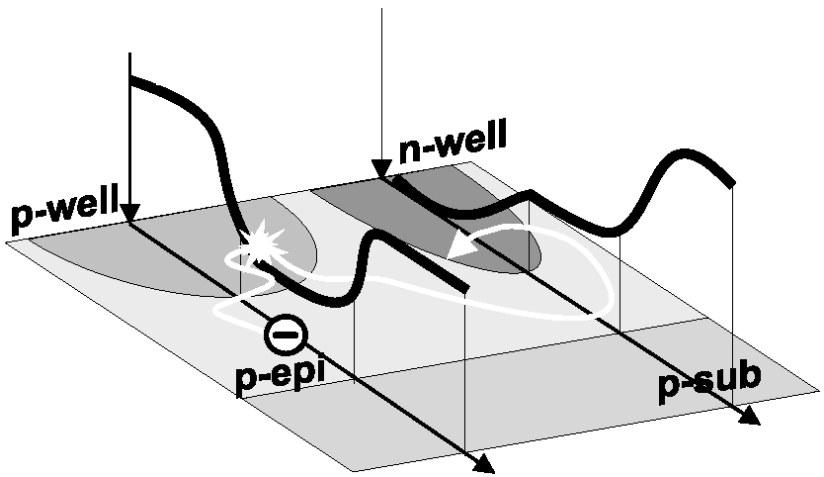
(3) Dipartimento di Ingegneria dell'Informazione
Università di Parma - Italy

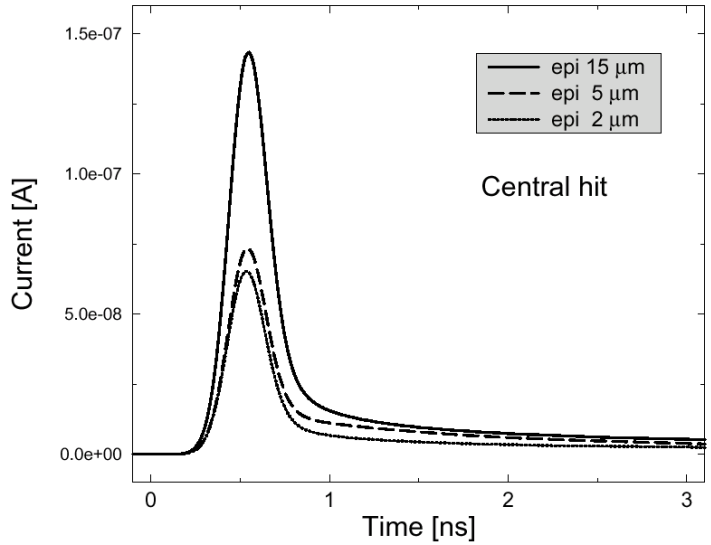
# Outline

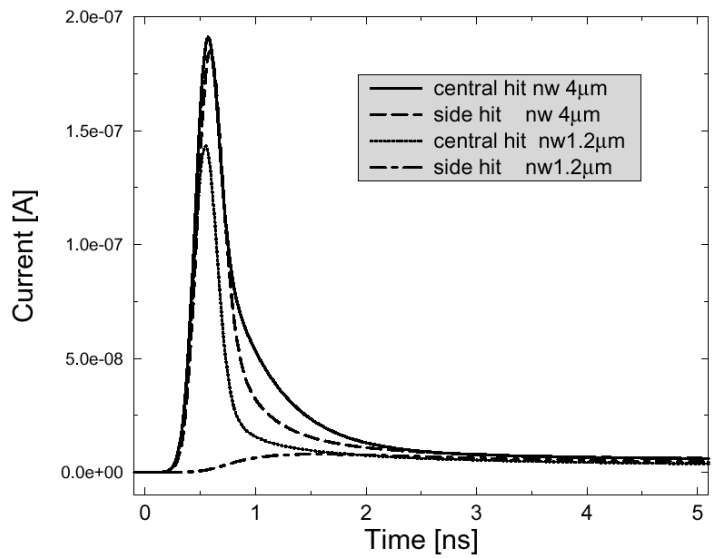
- Introduction.
- Active Pixel Sensor in standard CMOS technology.
- Technology Optimization.
- Design flow.
- Architectures of charged-particle CMOS sensors.
- Results analysis.
- Conclusions.

# Technology Analysis



# Technology Hints for CMOS APS

- EPI layer importance …
- Substrate generation contribution is important !
- n-well depth impact on charge collection…

⇩

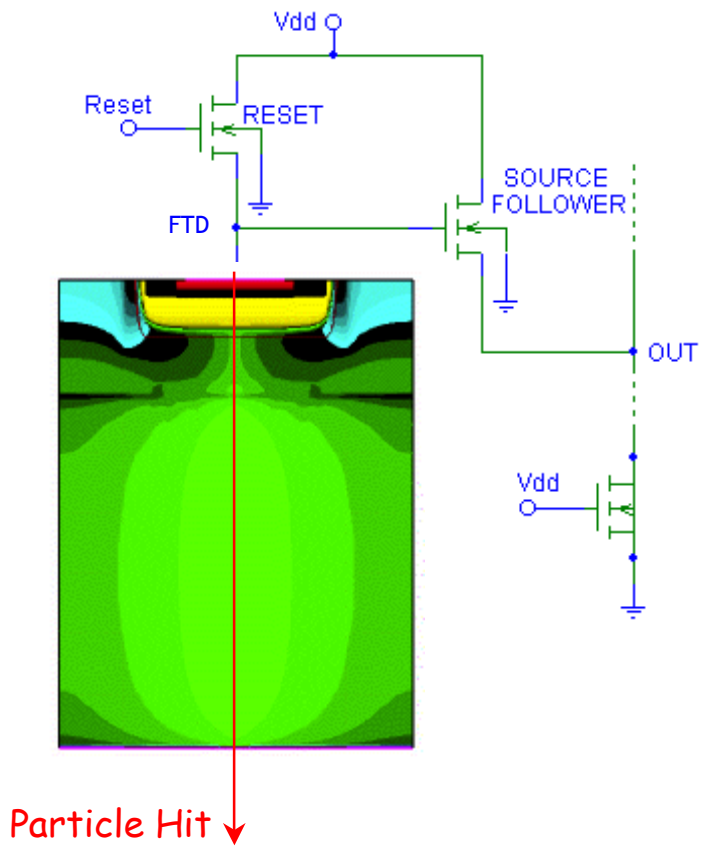
Standard CMOS (deep-submicron) technologies:

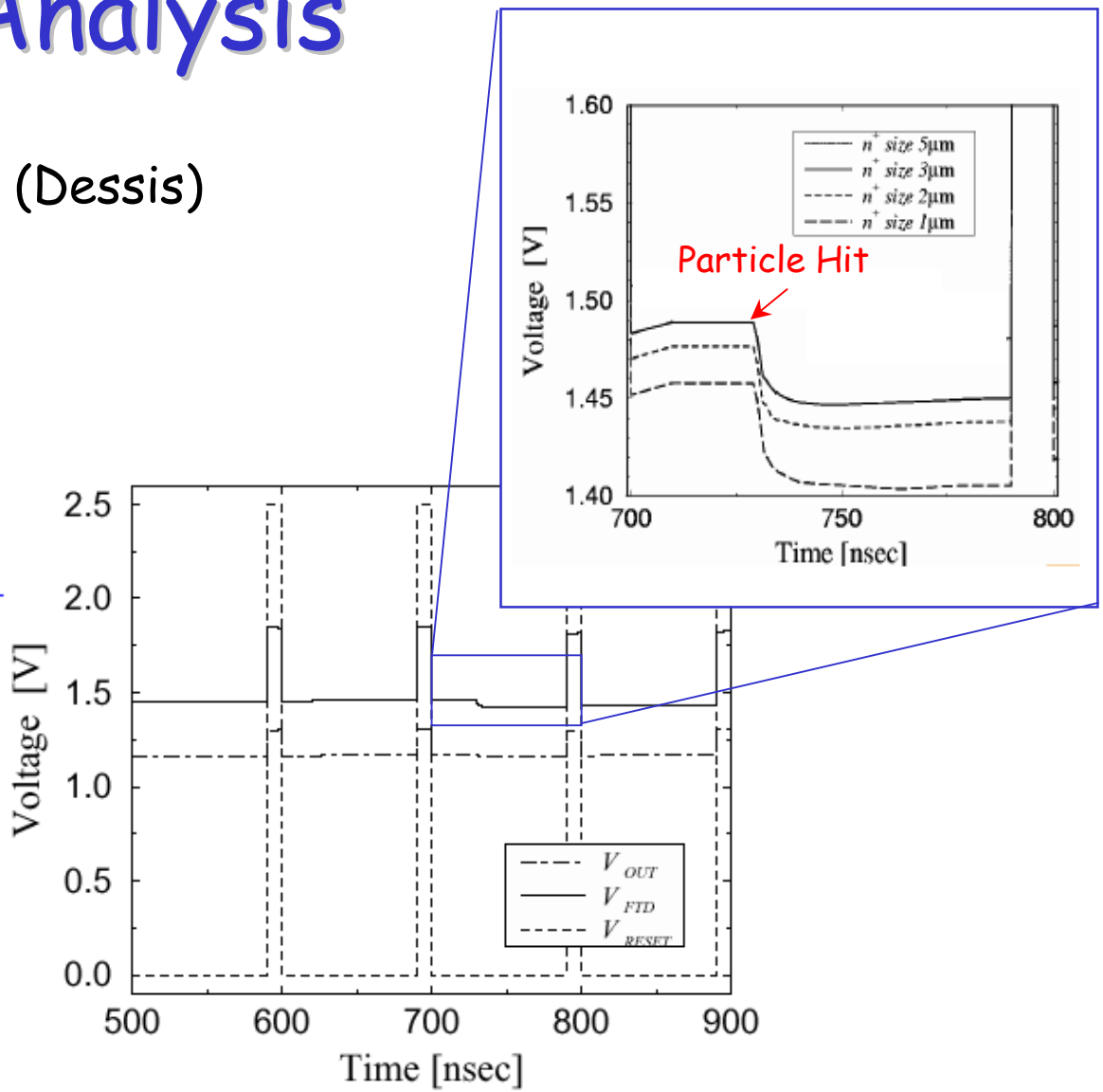
- Smart read-out electronics integration is easier.
- $C_{photodiode}$ is lower, S/N is still acceptable.
- Better control of life-time of the technology node.

↳ Comprehensive technology-node analysis…

# Mixed-Mode Analysis

- Device/Circuit Simulations (Dessis)



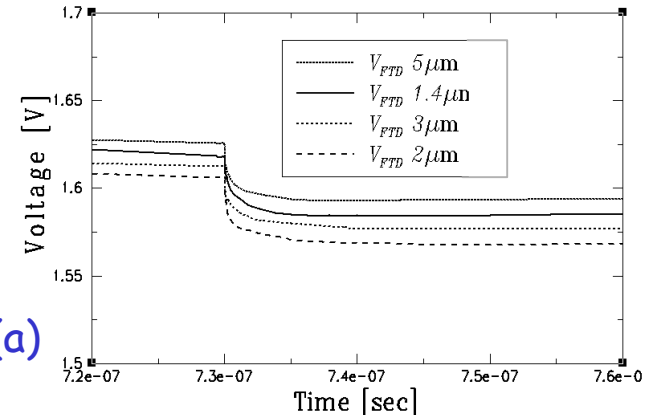



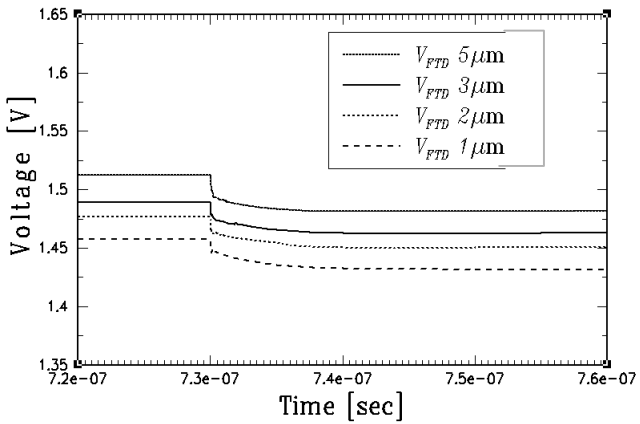
# Technology Options

## A - No EPI-layer

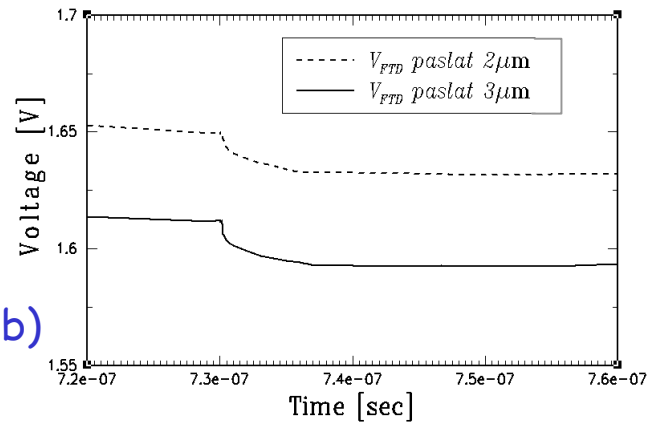
## B - EPI-layer

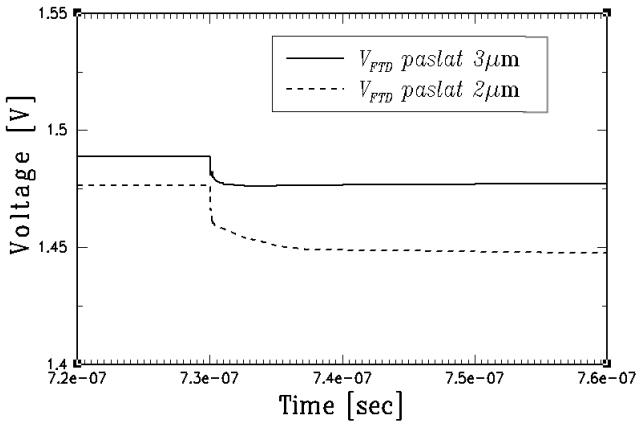
(a)




(b)



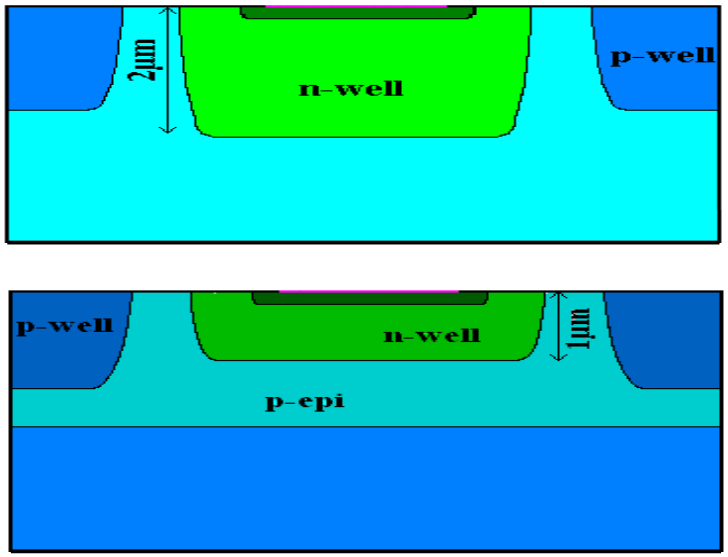



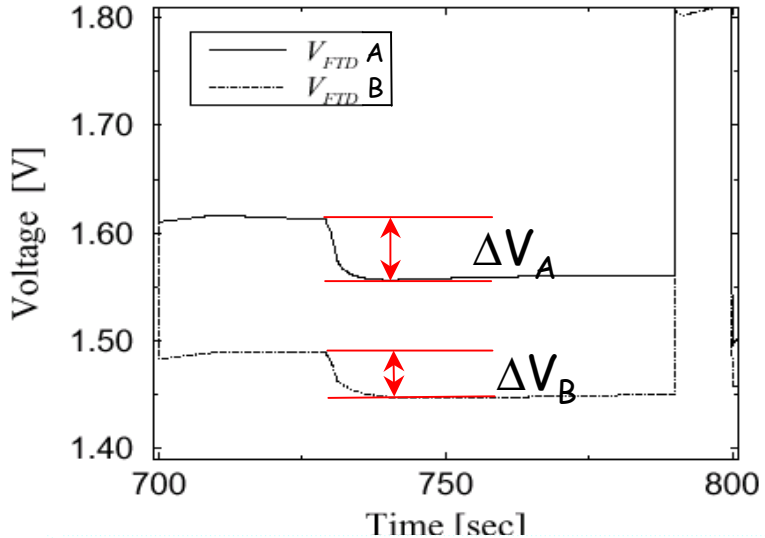

| A | | B | |
|---|---|---|---|
| Diode Area | $\Delta V_{FTD}$ | Diode Area | $\Delta V_{FTD}$ |
| 1.4x1.4 | 34 mV | 1.0x1.0 | 32 mV |
| 2.0x2.0 | 40 mV | 2.0x2.0 | 25 mV |
| 3.0x3.0 | 36 mV | 3.0x3.0 | 26 mV |
| 5.0x5.0 | 32 mV | 5.0x5.0 | 30 mV |

| A | | B | |
|---|---|---|---|
| Diode Area | $\Delta V_{FTD}$ | Diode Area | $\Delta V_{FTD}$ |
| 2.0x2.0 | 28 mV | 2.0x2.0 | 30 mV |
| 3.0x3.0 | 20 mV | 3.0x3.0 | 18 mV |

Voltage responses as a function of the sensitive element area for different particle trajectories: (a) central, (b) lateral.

# Technology Options (2)

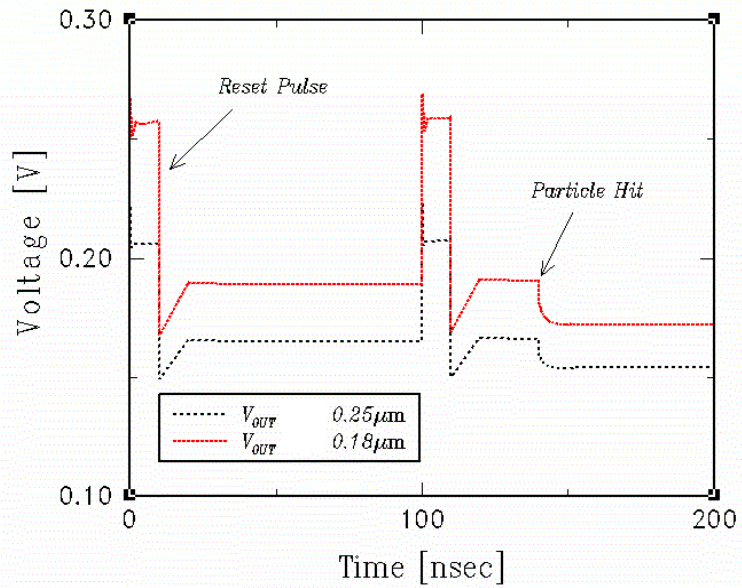



$\Delta V_A$ swing greater than $\Delta V_B$ !

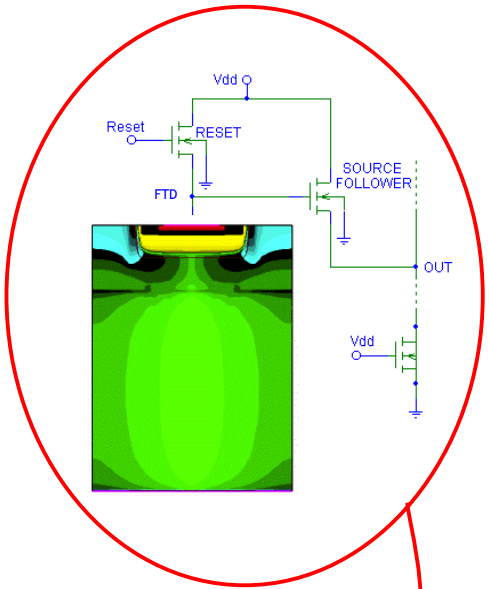
$\Delta V_{A\ 0.18}$ swing greater than $\Delta V_{A\ 0.25}$ !

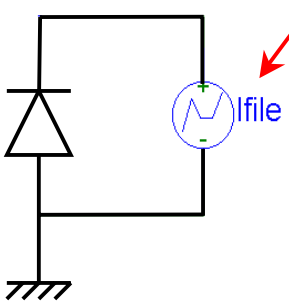
The 0.18 μm technology has been selected !

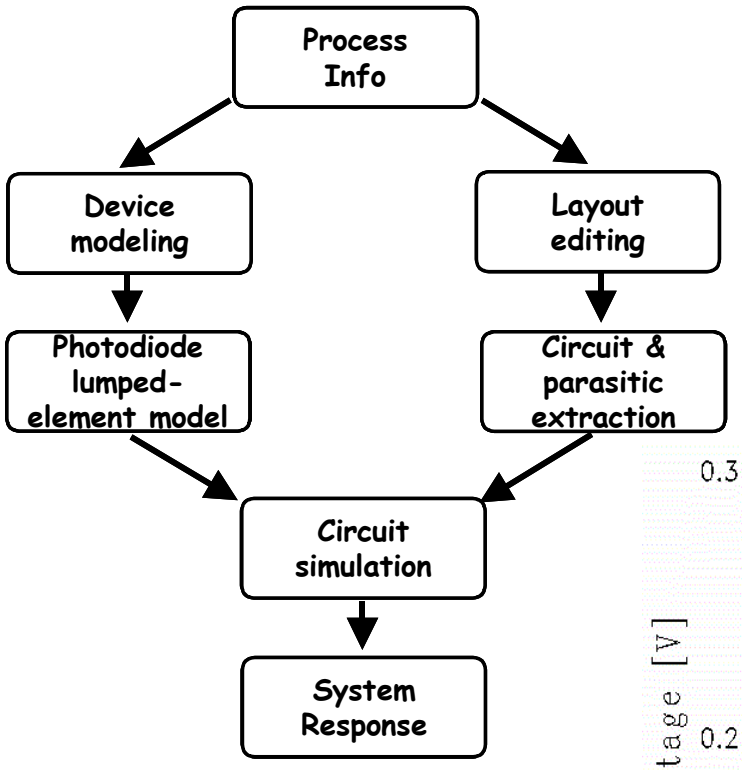


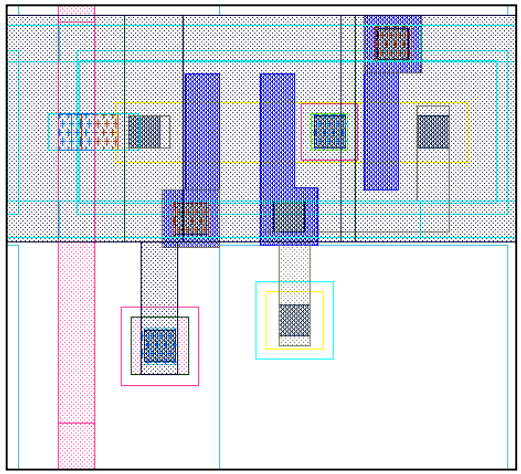
# Design flow

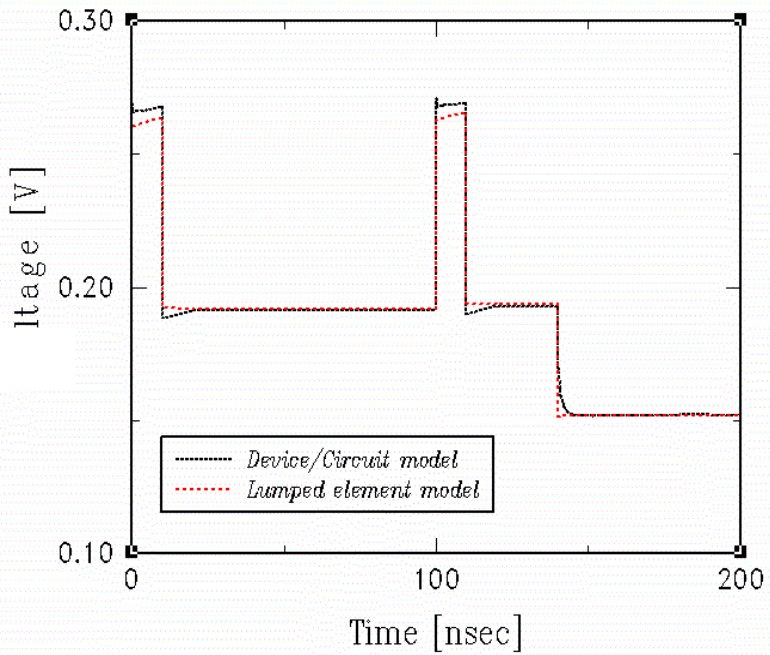
CADENCE IC Design System



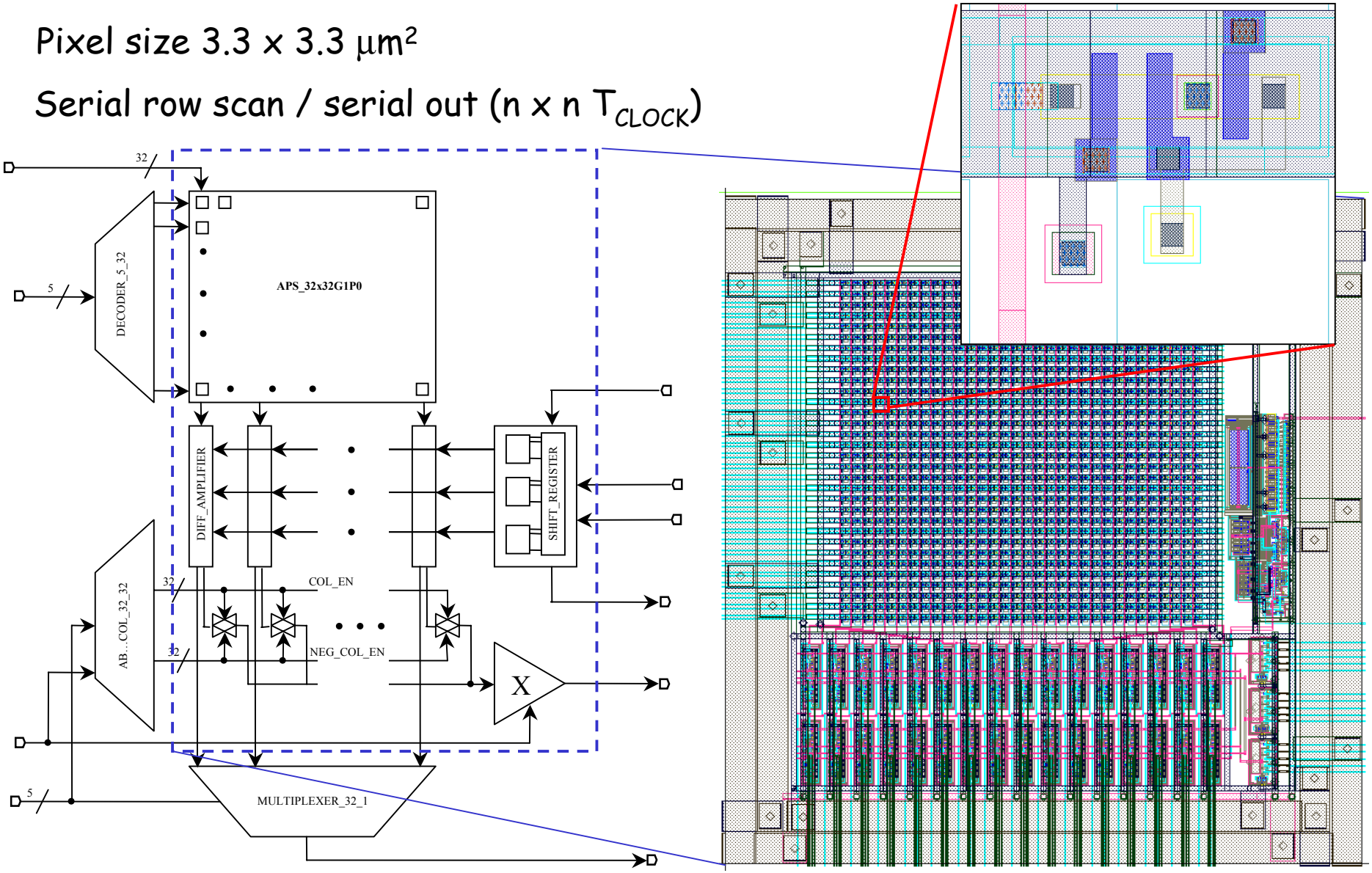





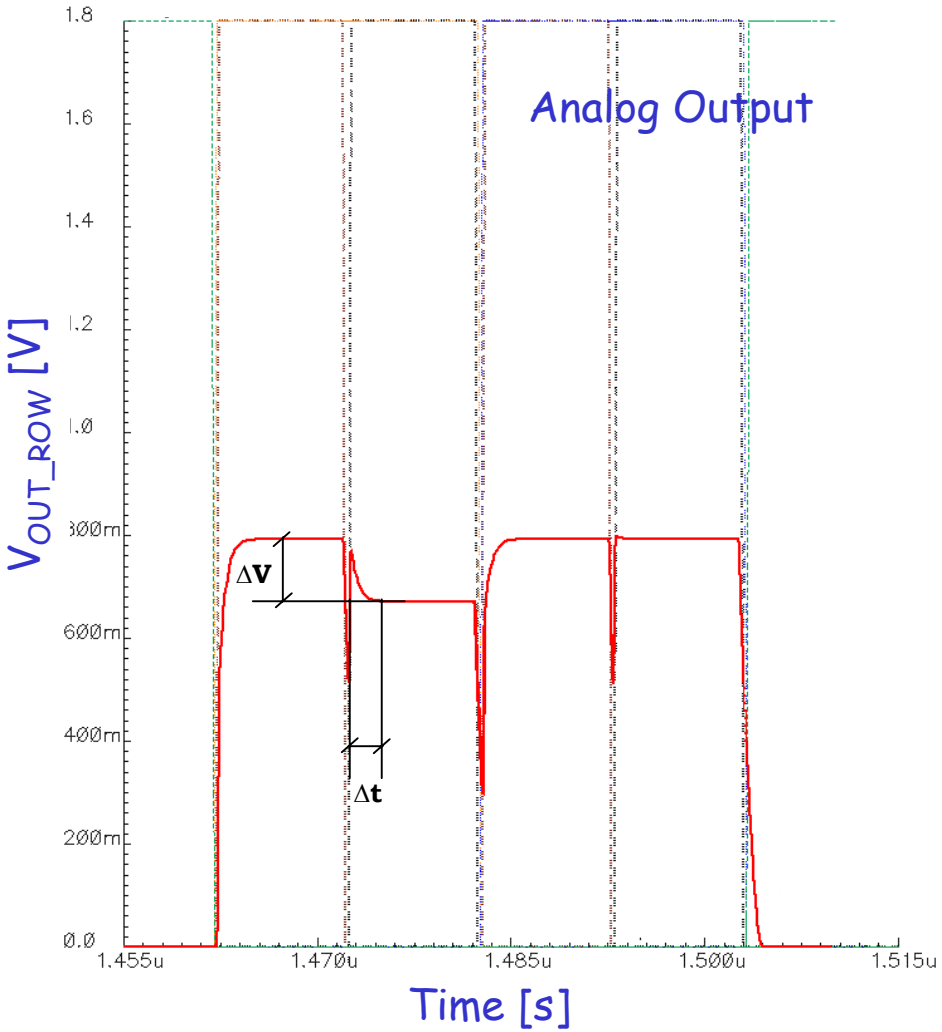
# APS matrix architecture

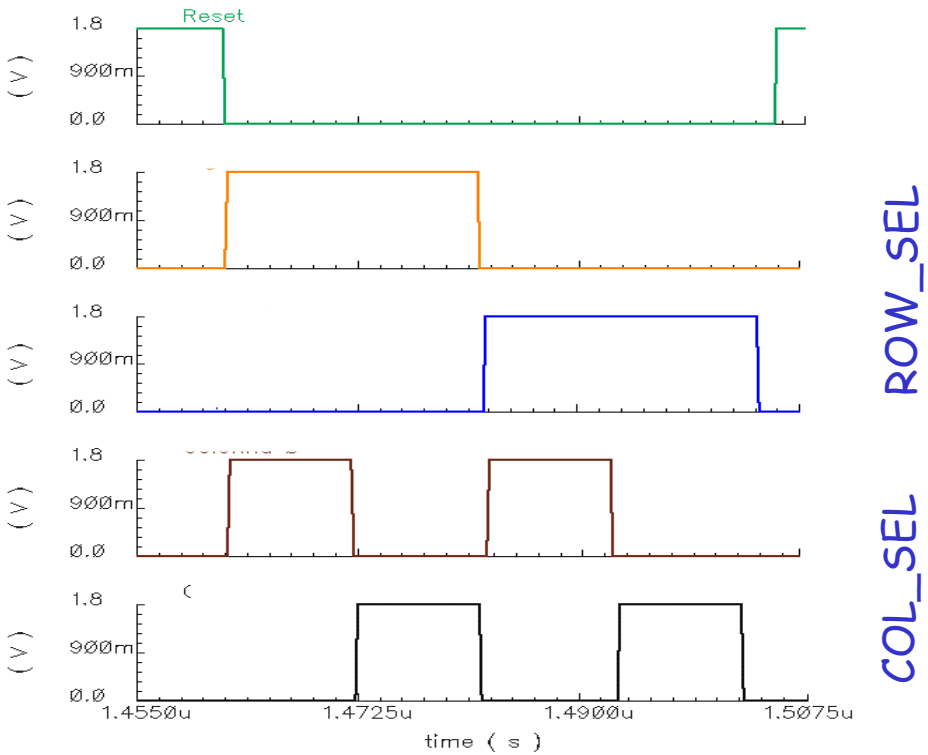
Pixel size 3.3 x 3.3 μm²

Serial row scan / serial out (n x n $T_{CLOCK}$)



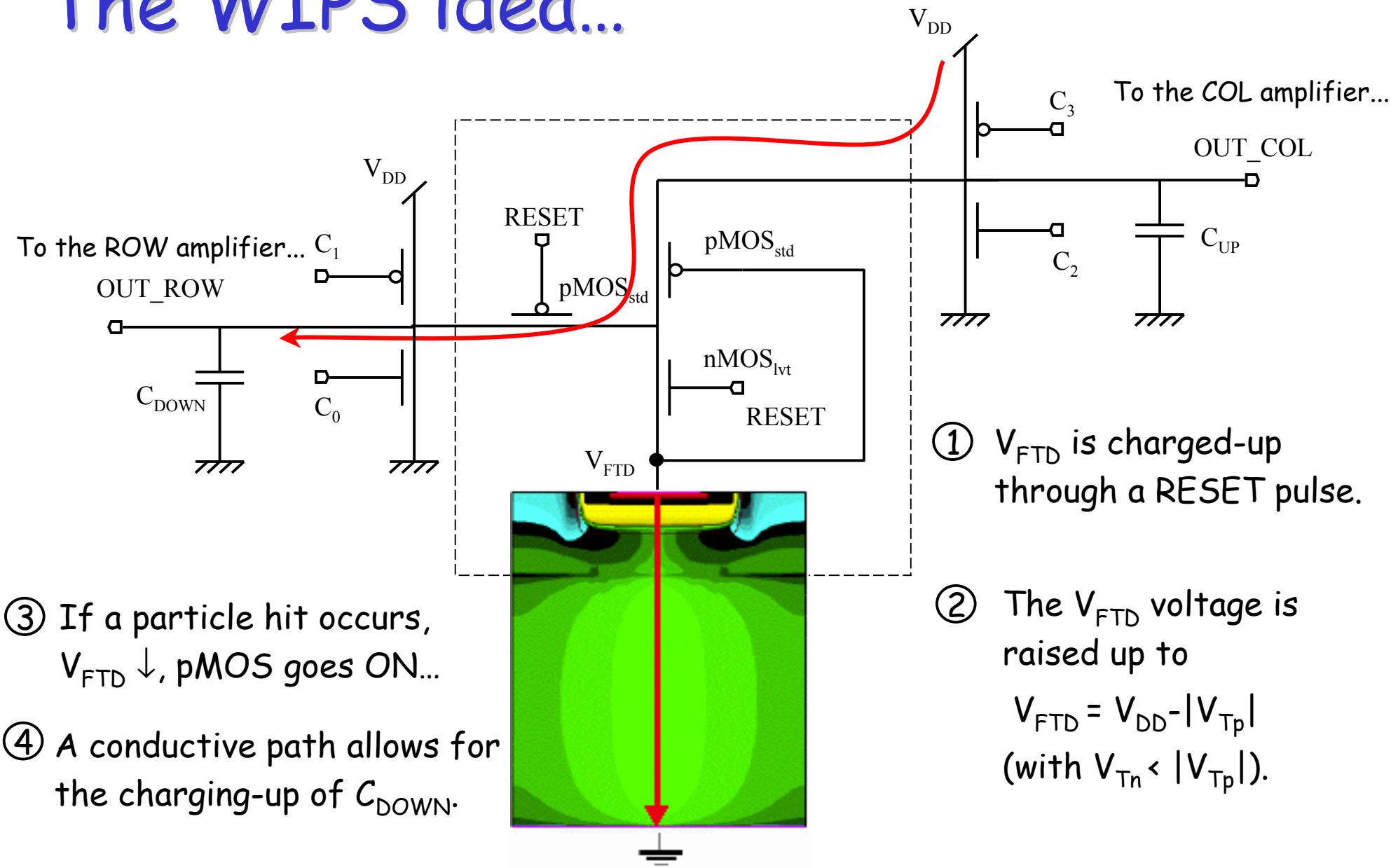
# APS simulation results




| Parasitic Extraction | $V_{dark}$ [mV] | $V_{light}$ [mV] | ΔV [mV] | $\Delta t_{max}$ [ns] |
|---|---|---|---|---|
| **WORST** | 993 | 883 | 110 | 7 |
| **TYPICAL** | 906 | 795 | 111 | 5 |
| **BEST** | 720 | 600 | 120 | 4 |

# The WIPS idea…




① $V_{FTD}$ is charged-up through a RESET pulse.

② The $V_{FTD}$ voltage is raised up to

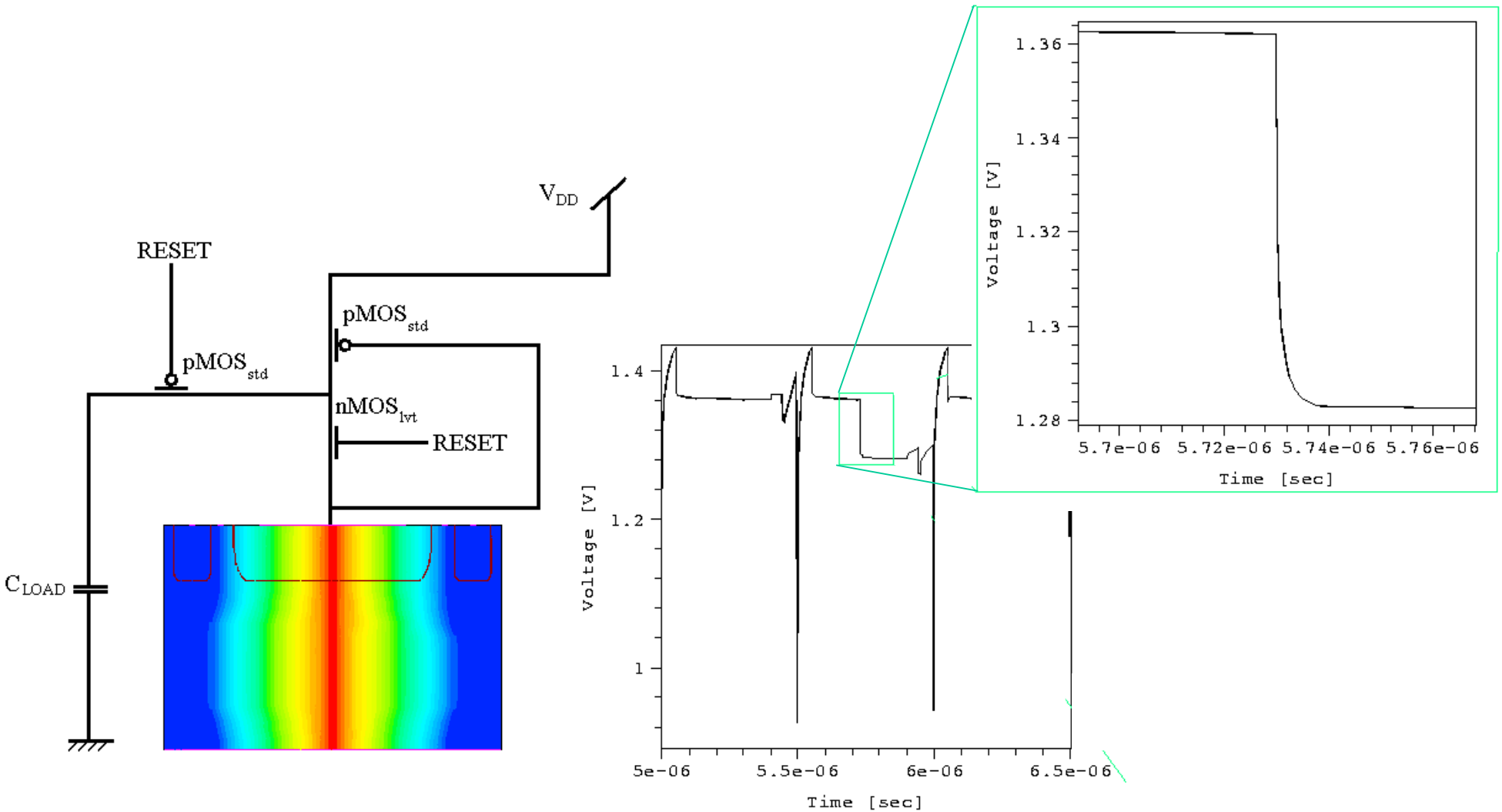
$V_{FTD} = V_{DD} - |V_{Tp}|$

(with $V_{Tn} < |V_{Tp}|$).

③ If a particle hit occurs, $V_{FTD}$ ↓, pMOS goes ON…

④ A conductive path allows for the charging-up of $C_{DOWN}$.

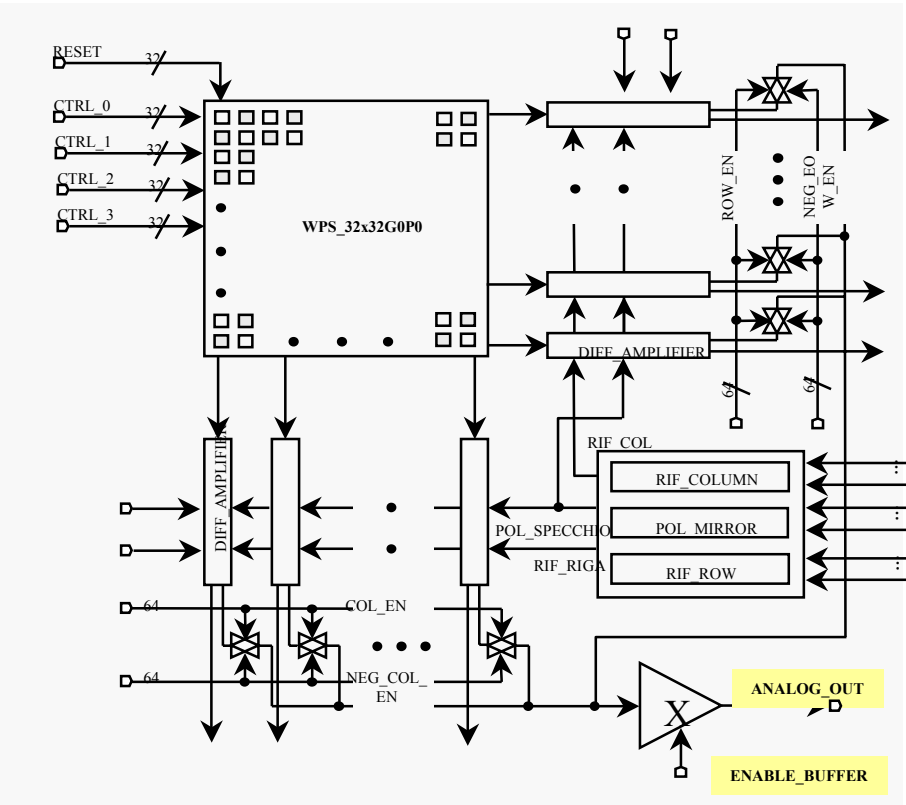
# WIPS Mixed-Mode Analysis

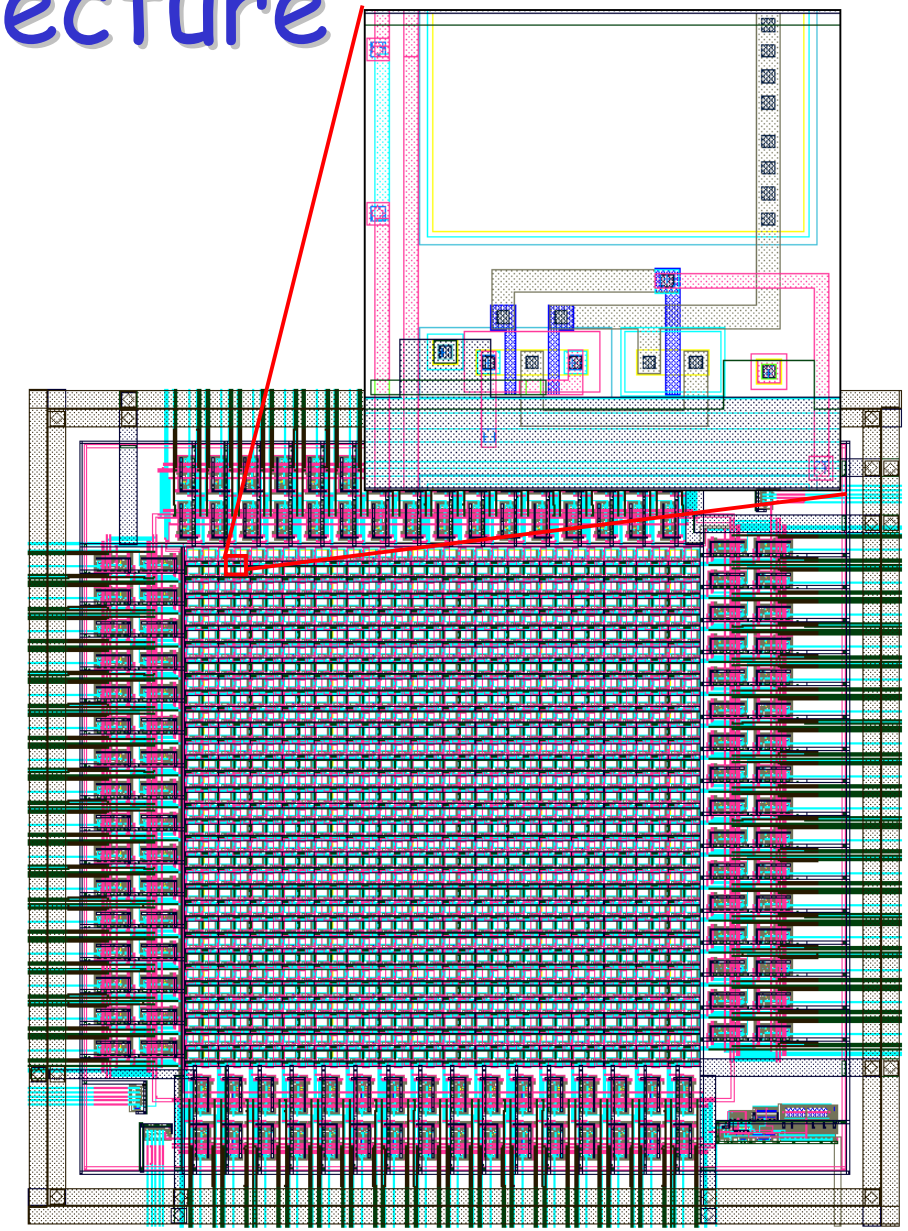


# WIPS matrix architecture

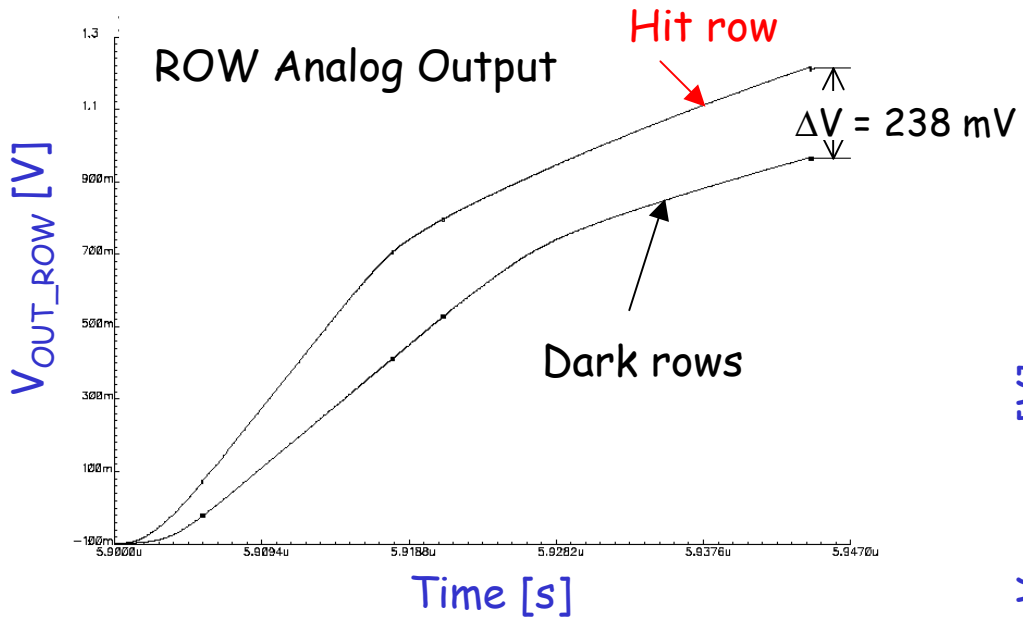
Pixel size 10 x 10 $\mu m^2$

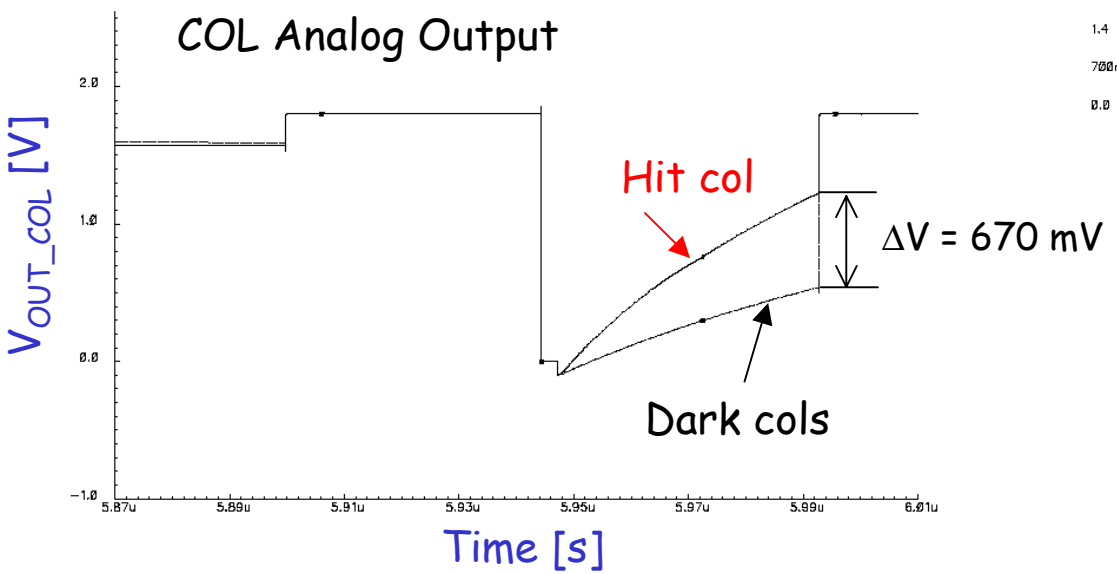
Single row scan / serial out ($n + n\ T_{CLOCK}$)

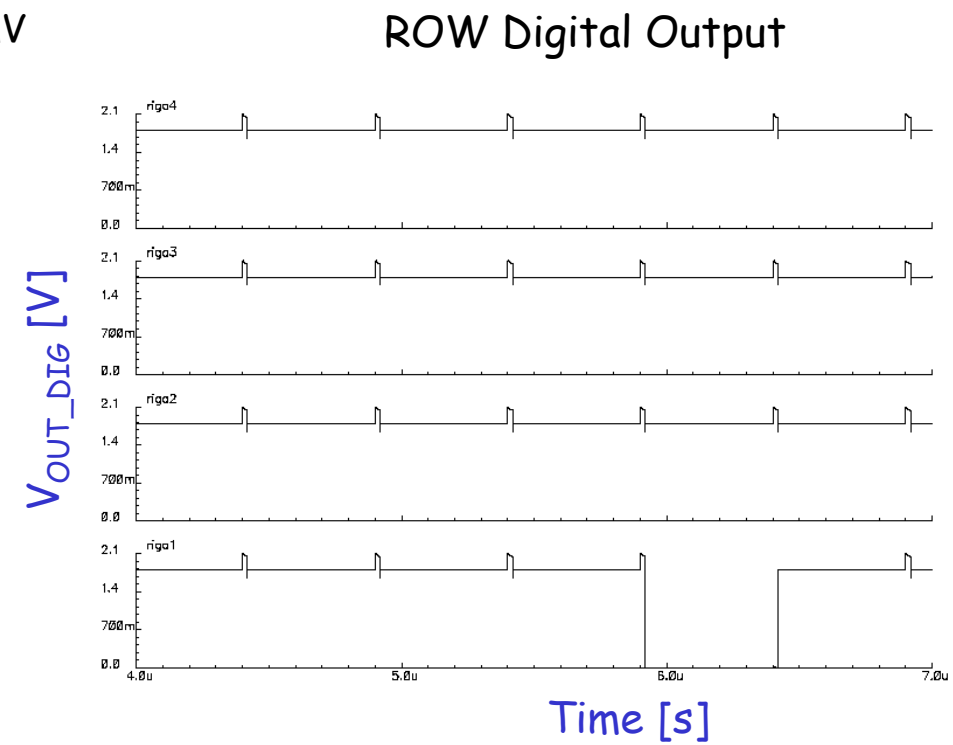


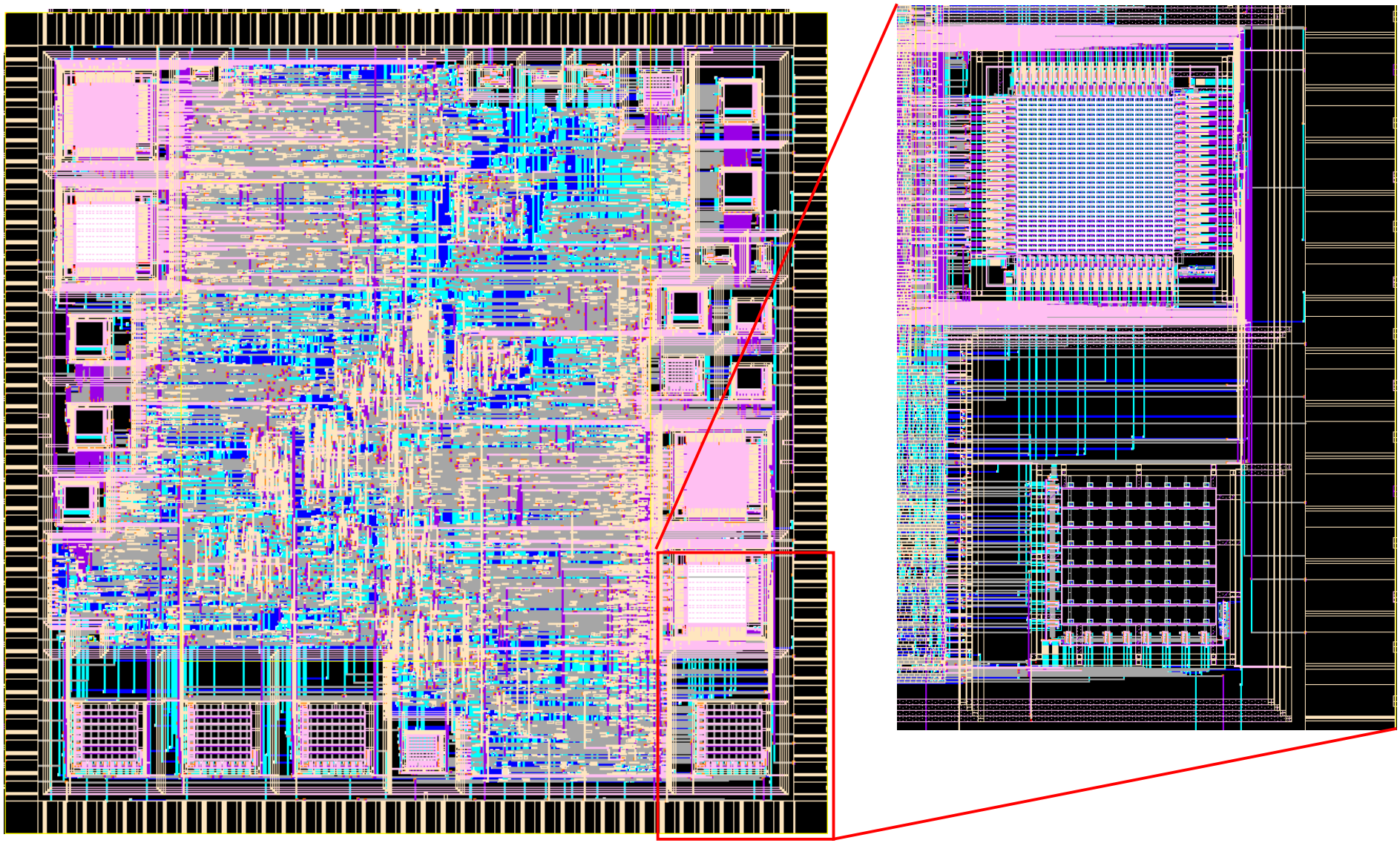
# WIPS simulation results



# RAPS01 chip layout



# Conclusions

Standard VLSI CMOS technologies have been evaluated for the implementation of charged-particle detectors.

Deep submicron technologies appear suitable for such a purpose, allowing for increased spatial resolution and for the integration of smart read-out electronics.

Different pixel architectures have been proposed, especially tailored for the detection of single hits, thus allowing for a simplification and a potential speed-up of the read-out system.

The design of a set of prototypes has been completed, and their fabrication in 0.18 μm technology is under way.

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