Active Pixel Sensor Architectures in Standard CMOS Technology for Charged-Particle Detection

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1 Introduction

The adoption of active pixel sensors (APS), based on an "active" read-out scheme implemented at the pixel level, has been recently proposed for charged-particle detection purposes [1, 2]. Very good performances have been obtained, in particular by exploiting some peculiar features of the actual fabrication technology (i.e., the presence of a relatively deep and low-doped epitaxial layer). In this work, we extend such an approach toward advanced VLSI CMOS technologies with the aim of increasing spatial resolution and optimizing the pixel-level response by exploiting state-of-the-art microelectronic devices. To this purpose, accurate analyses have been performed, investigating performance dependency on actual technology features in order to assess guidelines for the integration of physical sensors and effective signal-processing circuitry on the same chip. In particular, different technological nodes (coming from different silicon foundries) have been evaluated. An extensive CAD-based analysis has been carried out: device, circuit and mixed-mode simulations have been performed, accounting for the effects of several technology and design options. Steady-state characteristics and transient response to a particle hit have been predicted and correlated to major design parameters and to environmental conditions. Based on these results,

the suitability of CMOS technology for the integration of particle detectors has been evaluated and the complete design of a set of prototypal pixel arrays has been carried out.

2 Technology analysis

The first step of our analysis aimed at checking wheter typical CMOS-processes substrates (i.e., substrates featuring resistivity in the order of a few $\Omega \cdot$cm) could be exploited as a sensitive volume for Minimum Ionizing Particles (MIPs). Investigations were made by means of device simulation; a radiation-sensitive diode, implemented by exploiting the n-well/p-sub junction, has been simulated with the ISE TCAD package [3]. Particle hit has been considered by generating a proper amount of electron-hole pairs along the supposed particle trajectory: the simulation of the relaxation transient then allows for estimating the collection properties of the device and to correlate them to main fabrication parameters, such as the layer structure and the doping profile. In this framework, a wide set of issues has been considered, in order to select the optimal fabrication technology, among those commercially available. A detailed review of simulation results goes beyond the scope of this paper; nevertheless, some are worth to be mentioned here, since they have straightforward influence on detector design considerations.

For instance, the presence of a relatively low-doped epitaxial layer (often available in standard CMOS fabrication processes) can be exploited to increase the charge collection efficiency of photodiodes, as illustrated in [1, 2]. Our simulations confirms such a result: in Fig. 1, the amplitude of the current-pulse at the photodiode is shown, depending on the epi-layer thickness. Also the n-well depth has a strong influence on the sensor response: in particular, deeper wells exhibit better responses, as shown in Fig. 2. In the case of a particle hitting the diode in a central position, this can be straightforwardly explained with the increase of the sensitive volume; nevertheless, a significant improvement is found for lateral particle crossing as well (i.e., for particles hitting the gap between two adjacent photodiodes). In this case, carrier diffusion conveys part of the charge toward the n-well sidewalls anyway: for a deeper well, a larger lateral surface collects a larger amount of charge. Simulation, furthermore, shows that the charge collection is not strictly limited to the epi-layer: actually charge generated deeper into the substrate still contribute to a non-negligible extent to the detector response. Such a contribution, in particular, comes from a more conductive layer, located far away from the pixel electrode and may therefore have some influence on the resolution among adjacent pixels. In synthesis, simulations suggests that the integration of a radiation-sensitive device within a state-of-the-art, standard VLSI CMOS technology should be feasible; with respect to customary detector technologies (i.e., high-voltage, low-doped devices) the inherently lower efficiency of the photodiode
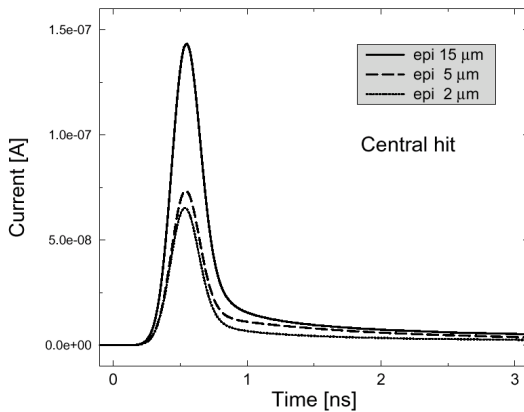
Figure 1: Response of the sensitive element to a crossing particle, as a function of the epitaxial layer depth (for a typical 0.35 μm technology).
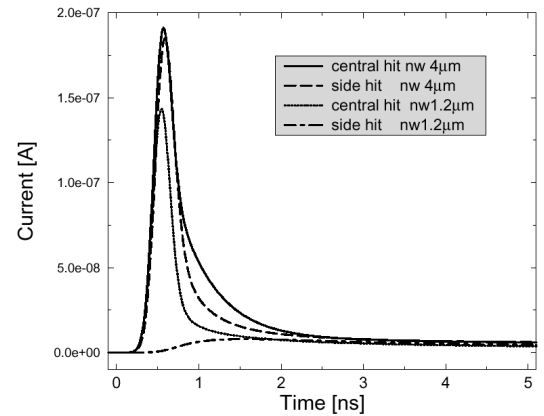

Figure 2: Response of the sensitive element to a crossing particle, as a function of the n-well (nw) depth (for a typical 0.35 μm technology).

can actually by compensated by the possibility of integrating much more efficient and versatile signal-conditioning circuitry, within the pixel itself and in the read-out subsystem. Moreover, deep-submicron technologies are intrinsicly more resistant to radiation damage and allow for reduced parasitic capacitances of the sensitive element (due to the reduced feature size pertaining to scaled technologies). Finally, the adoption of "mainstream" technologies should guarantee a better control over the life-time of the technology nodes and thus over the design and production costs of "smart" detectors.

3 Mixed Mode analysis

Device simulations discussed in the previous section, however, are not sufficient to estimate actual performance of a sensor chip, where an array of photodiodes is embedded within a larger, distributed electronic network. Modeling the whole circuit at the physical level would have been practically prohibitive, so that less demanding approaches have been followed. Depending on the degree of accuracy we sought for, either circuit simulation or mixed-mode simulation have been used. In the former case, as detailed later on, an equivalent-circuit model for the photodiode was needed; the latter approach, instead, consist of a self-consistently coupled device- and circuit-simulation: critical devices (the photodiode and its neighbouring junctions) are still described at the physical level, whereas peripheral circuits are taken into account by compact modeling.

The basic read-out scheme for an APS sensor is sketched in Fig. 3, and includes a

reset and a buffering transistor at each pixel; addressing decoders and bus amplifiers (not shown in figure) have to be considered as well: the line load has been considered by means of a current sink, assuming a worst case condition [4]. By means of
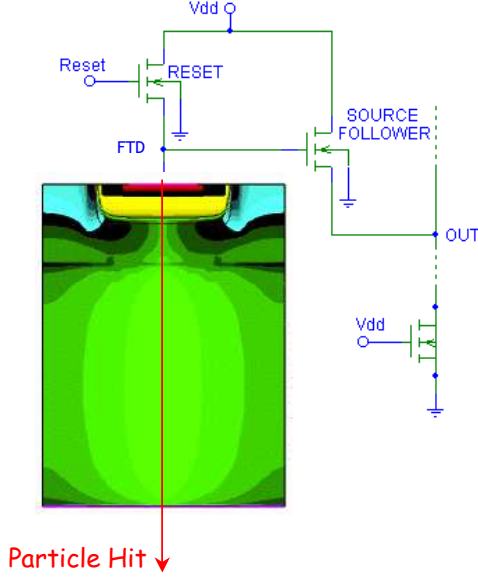

Figure 3: Mixed-mode analysis, combining device-level description of the sensitive element and circuit-level description of the read-out circuitry.
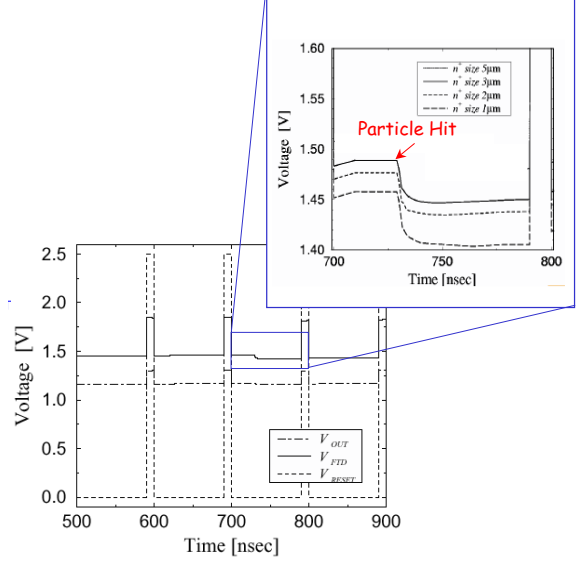

Figure 4: RESET, photodiode (FTD) and output (OUT) node voltage response to a particle hit, depending on the sensitive area dimensions.

such a more complete picture of the array architecture, we can extend indications coming from the analysis of the photodiode alone: in fact, charge collected by the photodiode junction is shared with parasitic capacitances coming from neighbouring devices (reset and source-follower transistors), so that the actual voltage drop at the photodiode cathode strictly depends on the overall pixel architecture. On the other hand, increasing the area of the sensitive window (which would reduce charge sharing and improve the fill-factor as well) does not necessarily imply a better response: the amount of charge generated into the sensitive layer is almost independent of the window footprint (depending only on the layer thickness), whereas the junction capacitance increases with it. Thus, given a fixed amount of charge, a larger capacitance yields a smaller voltage drop.

Comparison between different responses for different technologies, depending on the sensitive area, are summarized in Figs. 5. Here, plots in column (A) refer to a technology featuring no epi-layer, whereas column (B) refers to a $4\mu m$ epi-layer

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technology; response to different hit position (either central or lateral) are reported in both cases. A slightly better responses (i.e., larger voltage swings) are predicted for the (A) technology, differences being less evident for lateral hits: in any case, voltage drops of tens of millivolts are achievable, in the same order of the response of more traditional pixel read-out systems [5]. We then compared similar technologies of the (A) type (i.e., with no epi-layer), characterized by different channel feature-size: namely, 0.25 and 0.18 μm technologies (supplied by the same foundry) were examined. The project specs, in terms of spatial resolution, could be fulfilled in both cases, so we still compared the two options in terms of performances: different pixels were designed, accounting for specific layer structures and design rules; as shown in Figure 6, the simulations predicts a wider voltage swing for the 0.18 μm node, mostly due to the parasitic-capacitance lowering associated with the scaled technology. Once technology features had been assessed, we could proceed with the optimization of the dimensions of the sensitive element, balancing sensitive volume and parasitic capacitance in order to maximize the output voltage swing. Eventually, a 2×2 μm^2 pixel size has been selected: due to the absence of the low-doped epi-layer, charge sharing among adjacent pixels is limited, and small pixel pitches are more easily achieved. Based on such results, the very compact size of the pixel (3.3 × 3.3 μm^2) shown in the layout view in Figure 9 has been achieved. It is worth observing that, as mentioned above, the actual resolution target did not require the adoption of such an aggressive scaling-down; the choice of an advanced technology was instead driven by performance evaluation. With respect to more mature technological nodes, moreover, such a choice better guarantees long-term stability and maintenance.

4   System design

Design and verification of the system chip require a more computationally efficient approach: to this purpose, data coming from device and mixed-mode simulations illustrated so far were exploited to devise and carefully tune a compact model of the sensing element. Basically, a junction diode (properly characterized with respect to the actual technology) was supplemented by a current generator, describing radiation-induced current pulses, as predicted by device simulation. Layout-extracted parasitics have been taken into account as well, thus resulting in a quite realistic, yet computationally reasonable, photodiode model. A comparison between pixel responses predicted at physical (i.e., device-simulation) level and at circuit level is shown in Figure 7 and exhibits a satisfactory agreement. Once validated the photodiode model, simulation of the complete circuit became feasible: several array of pixels, organized in the customary matrix topology (32×32 elements, sufficient for testing purposes) were designed, and arranged on a test chip. Digital circuitry needed for row and column addressing was added, as well as buffers driving analog output pads. A view
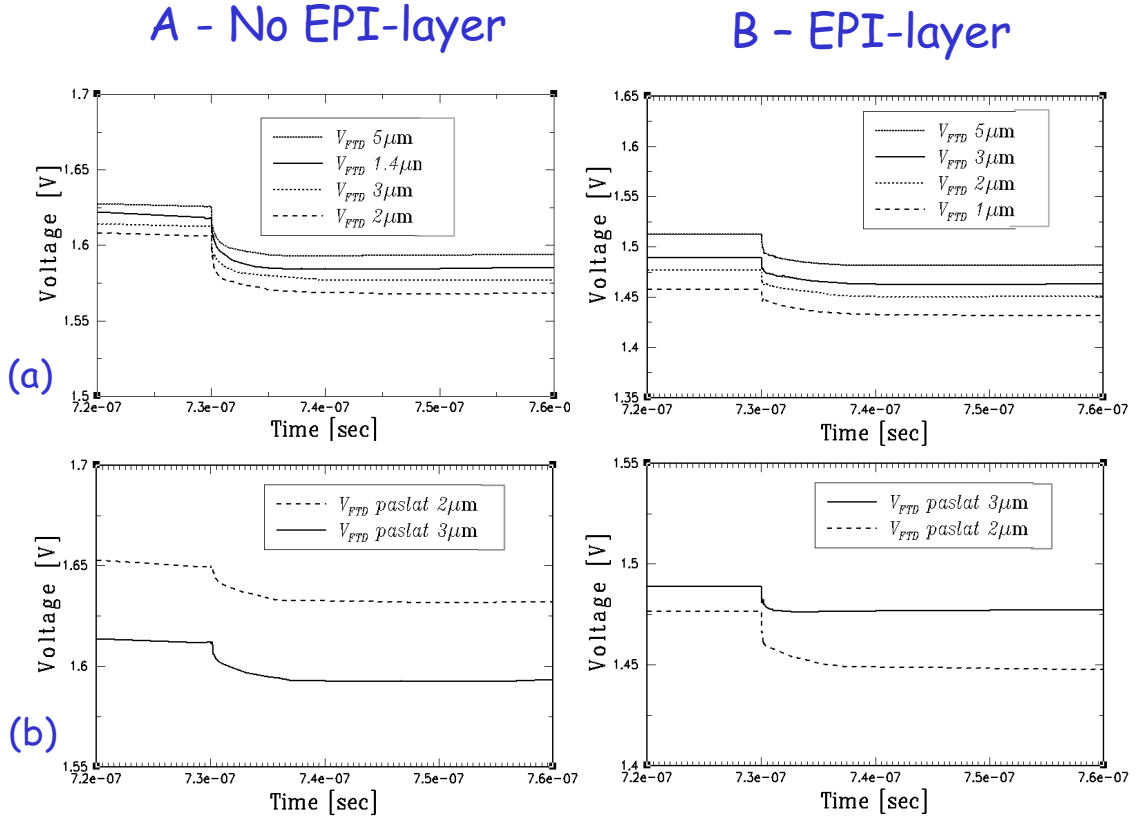
Figure 5: Voltage responses of different technologies (A - No EPI-layer, B - EPI-layer) as a function of the sensitive element dimensions (assuming a square sensitive element whose side featuere is reported) for different particle trajectories: (a) central, (b) lateral (paslat = lateral crossing).

of the complete block diagram is reported in Figure 8, whereas the corresponding physical layout is shown in Figure 9. It is worth pointing out that the hierarchical modeling strategy described above made it possible to exploit customary tools for the verification of a system including active sensors: a fully standard VLSI design flow has thus been followed to design the chip as a whole, allowing, in particular, for the use of digital synthesis tools where needed. By this approach, the design of a set of prototypes has been completed, and their fabrication, in the framework of the RAPS research project, supported by the I.N.F.N., is currently under way.
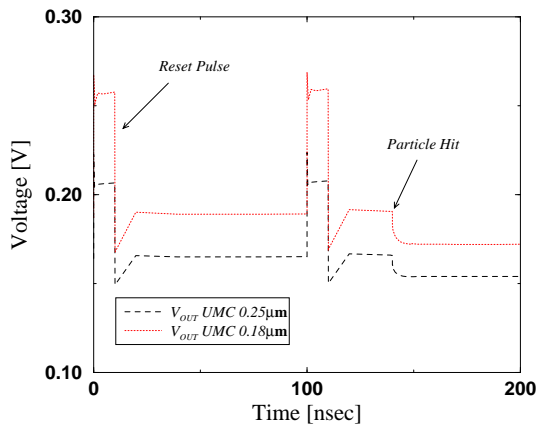
Figure 6: Pixel response, as predicted for 0.25 and 0.18 μm technologies, the latter exhibiting a wider swing of the output signal.
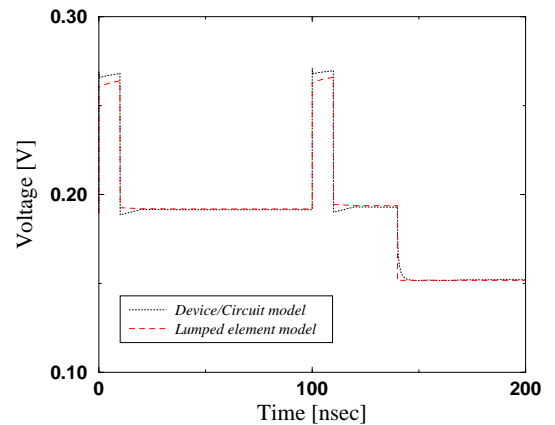

Figure 7: Pixel response, as predicted by mixed-mode (i.e., physical modeling of the sensitive element) and circuit (i.e., compact modeling of the sensitive element) simulations.

5   Conclusions

In this paper, standard VLSI CMOS technologies have been evaluated for the implementation of charged-particle detectors. A comprehensive set of CAD and TCAD tools has been exploited to support technology choice and to drive active pixel sensor design. According to our analysis, deep submicron technologies appear well suited for such an application, allowing for a potential increase of the spatial resolution and for easy integration of read-out electronics. Design and verification of a set of test circuits, in 0.18μm technology, has been carried out and their fabrication is currently being completed.

It is eventually worth remaking that, by exploiting a hierarchical modeling approach, the design of the active-sensor chip has been accomplished by a standard design flow: this will result of the utmost importance in next-generation chips, where, exploiting the advanced VLSI technology, smarter electronics will be implemented, thus achieving better on-chip signal-processing capabilities.
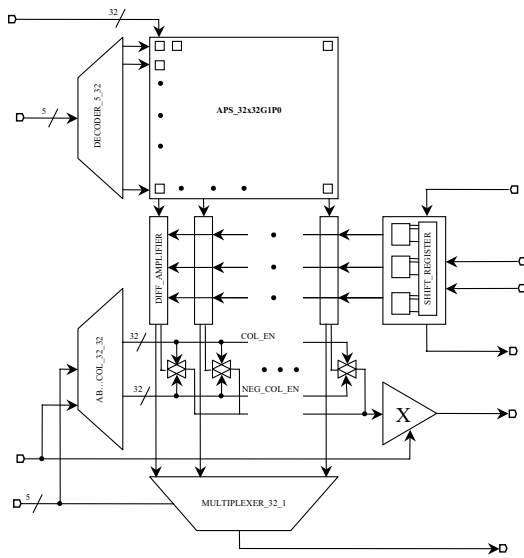
6   Acknowledgements

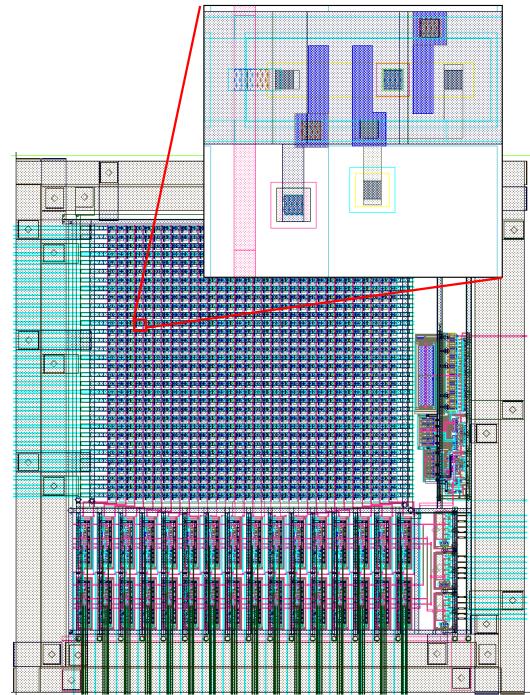Figure 8: Block diagram of a typical APS matrix.

Figure 9: Layout of a APS matrix with the detail of a single pixel.

References

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