The Architecture of the BTeV Pixel Readout Chip

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1   Introduction

The most striking feature of BTeV, a dedicated b physics experiment which is expected to begin running in 2008 in the new CZero interaction region of the Fermilab Tevatron, is that the experiment will use data from a pixel vertex detector to reconstruct tracks and vertices *for every beam crossing.* The lowest level trigger will be an impact parameter trigger designed to identify events containing reconstructable decays of charm and bottom particles[1]. An R&D program to develop a pixel readout chip optimized for the Tevatron was started at Fermilab in 1997, and is now nearing completion. The architecture of the BTeV pixel readout chip is described in this paper.

2   FPIX2 Overview

The BTeV pixel vertex detector will consist of a number of arrays of sensors mounted perpendicular to the beam direction. The inner edge of the sensors will be only 6 mm from the colliding beams and, at the design luminosity of $2 \times 10^{32} cm^{-2} sec^{-1}$, will receive a dose equivalent to $\sim 10^{14} cm^{-2}$ 1-MeV neutrons per year. The BTeV pixel readout chip, designated "FPIX2," has been designed using radiation tolerant layout techniques[2] for implementation in either of two commercial processes - Taiwan Semiconductor Manufacturing Company 0.25 μm CMOS, or the 0.25 μm CMOS process available through CERN.

The BTeV pixel size will be 50 μm $\times$ 400 μm. Each FPIX2 will read out an array of 22 columns $\times$ 128 rows of pixels. The only supply voltages required are 2.5 V and ground; all other bias voltages, bias currents, and threshold voltages are generated by on-chip programmable digital to analog converters (DAC's). Since the pixel hit information is used by the lowest level trigger, all hits are read out. Each readout chip sends hit data directly to an FPGA on a "Pixel Data Combiner Board" located $\sim$10 m away, outside the high radiation field. This means that the FPIX2's and the pixel sensors themselves are the only active devices exposed to significant levels of

radiation. The FPIX2 uses standard Low Voltage Differential Signaling (LVDS) for all I/O.

Data is output from the FPIX2 using point-to-point serial links which operate at 140 Mbps. The average number of hits per crossing is much larger for sections of the BTeV pixel detector located closest to the beam than for sections located farther away from the beam. Consequently, the required output bandwidth also varies greatly across the detector. To reflect this fact, the FPIX2 can be programmed to use 1, 2, 4, or 6 serial output links.
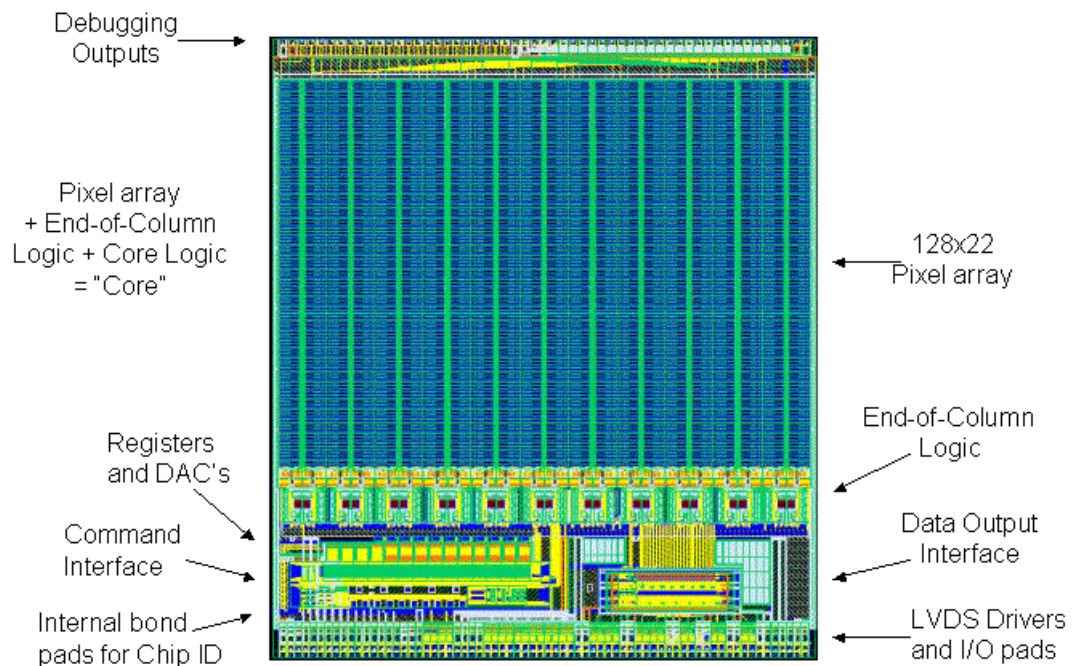
3 FPIX2 Layout

Figure 1: FPIX2 layout.

Fig. 1 shows the FPIX2 layout. The pads located on the top edge of the chip in the figure are for debugging purposes only. All normal connections to the chip

are made using a single row of 70 wire-bond pads located at the bottom edge of the chip. There are five major functional blocks in the FPIX2 design. These are the pixel array itself, the end-of-column logic, the data output interface, the command interface, and the registers and DAC's. The pixel array, the end-of-column logic, plus a block referred to as "core logic" are together referred to as "the core." The balance of the chip is referred to as "the periphery."

4   Pixel Unit Cell

The FPIX2 pixel unit cell consists of a continuous-time-filter amplifier[3], eight comparators which together form a 3-bit flash ADC, and digital logic which encodes the ADC information, stores the hit information until it is read out, and responds to commands from logic located at the end of the column of pixels.

5   Chip Operation

The FPIX2 readout architecture can best be understood by focusing on the operation of the end-of-column (EOC) logic. Each EOC contains four "command sets" and each column can latch data associated with four separate beam crossings before any data is read out. Each command set contains a state machine that changes state on Beam Cross Over (BCO) clock edges. A fifth state machine, that changes state on Readout clock edges, controls the readout of data from the column. The BCO clock frequency is expected to be 7.6 MHz ($\frac{1}{132ns}$). The FPIX2 is expected to operate correctly with readout clock frequencies up to 35 MHz ($\frac{1}{29ns}$). The EOC logic is designed so that the BCO clock and Readout clock need not be related to one another, either in frequency or in phase.

Fig. 2 illustrates how pixel hits are latched and read out. The narrow rectangles represent pixels. The larger rectangles on the left hand side of the bottom of each part of the figure represent the four command sets. The possible command set states are Empty, Listen, Full, and Output, and the state of each command set is indicated by a letter. A number indicates the contents of the BCO register associated with each command set. Priority logic ensures that only one command set at a time can be in the Listen or Output states. The large rectangle on the right represents the readout state of the column. The possible readout states are Nothing To Say, Something To Say, Talking, and Silent.

The normal empty condition of an FPIX2 column is illustrated in the upper left of Fig. 2. One EOC command set is in the Listen state. On each BCO clock *falling* edge, this command set latches the state of the core logic BCO counter (this counter is incremented on BCO clock rising edges). When a pixel or group of pixels is hit, a "Hit Fast OR" signal is sent to the EOC. At the next BCO clock rising edge, the
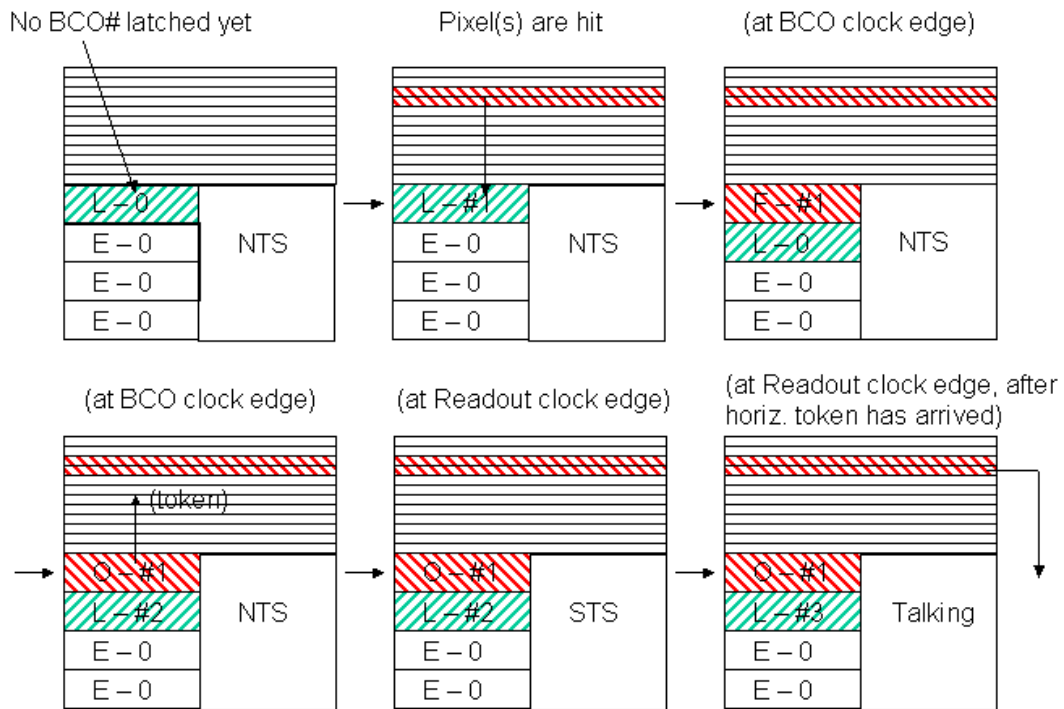
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Figure 2: This figure illustrates how pixel hit data is latched, associated with a BCO number held in the EOC, kept in the unit cell awaiting readout, and finally read out.

command set in the Listen state makes a transition to the Full state, and the Hit Fast Or is reset to zero. Simultaneously, another EOC set enters the Listen state. On the following BCO clock rising edge, the EOC set associated with the hit pixel(s) moves to the Output state and launches a "vertical token." On the first readout clock rising edge after an EOC set enters the Output state, the column readout state machine enters the Something To Say state, and notifies the core logic that the column has data ready to be read out. If the chip is not already reading out data, the core logic responds (on the following readout clock rising edge) by launching the "horizontal token." Data is driven off the hit pixels onto the "core bus" starting on the first readout clock rising edge after the horizontal token reaches the column. On this edge, the readout state machine enters the Talking state. A new pixel hit is read out on each subsequent rising edge of the Readout clock. When the vertical token arrives at the last hit pixel associated with the command set in the Output state, the horizontal token is released and stops at the next column with Something To Say. This ensures that there will not be an empty readout cycle between the last hit in one column and the first hit in the next column. When the horizontal token passes the last column, the core goes silent for one readout clock cycle. Another readout

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cycle is required to relaunch the horizon token, so there are always two empty readout cycles every time the horizontal token sweeps past all 22 columns. These are the only "wasted" readout cycles.
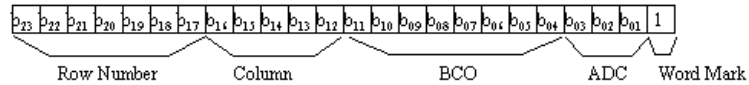
6 Data Output

Figure 3: Output Data Format.

Data is driven off a hit pixel onto the core output bus, which is 23 bits wide. The data word consists of the information generated in the pixel unit cell (7-bit row number and 3-bit ADC value), plus a 5-bit column number and an 8-bit BCO number, which are added by the end-of-column logic. The Data Output Interface (DOI) latches data from the core output bus on the *falling* edge of the readout clock, serializes the data, and drives it off chip. The DOI adds a word mark bit that is used by the receiving FPGA to verify the synchronization of the serial bit stream (see Fig. 3).

In order to establish synchronization with the receiving FPGA in the first place, the DOI sends a "sync/status" word (see Fig. 4). The sync/status word is identifiable because it contains zeros in bits 1-13. The data format ensures that pixel hit data can not contain thirteen consecutive zeros in any string of bits, either in one data word, or across two data words. This is possible because five bits are used to encode 22 column numbers. The FPIX2 column-numbering scheme has no column number ending in 00. This means that every data word has a one in either bit 12 or bit 13, or both. Whenever no data is available for output, FPIX2 transmits the sync/status word. At least two sync/status words are guaranteed to be output every time the column number decreases (indicating that the horizontal token has completed a sweep through the columns). The Pixel Data Combiner Board (PDCB) uses the word mark bit in every data word, and the sync/status words, to ensure that it can deserialize the data correctly.
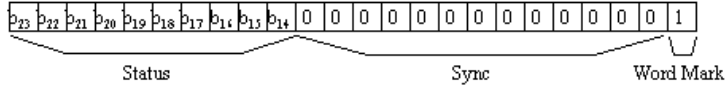
Figure 4: Sync/Status word format. The sync/status word is used to establish synchronization between the FPIX2 Data Output Interface and the receiving FPGA in the Pixel Data Combiner Board.

Configuration	SCLK Frequency	RCLK Frequency	
6 output pairs	140 MHz	35 MHz	140(6/24)
4 output pairs	140 MHz	23.3 MHz	140(4/24)
2 output pairs	140 MHz	11.7 MHz	140(2/24)
1 output pair	140 MHz	5.8 MHz	140(1/24)

Figure 5: This figure shows the relationship between the serial clock (SCLK) which determines speed of each output serial link, and the core readout clock (RCLK).

7 Output Clocks

The core readout clock (RCLK) is derived from the serial clock (SCLK). SCLK is constructed by the FPIX2 from two nominally 70 MHz clocks supplied by the PDCB, and is nominally 140 MHz. The frequency of RCLK is not the same for all FPIX2's in a pixel module, but depends on the number of serial data links being used for output data. The relationship between RCLK and SCLK (see Fig. 5) ensures that the time required to drive a word of data off chip is equal to the Readout clock (RCLK) period. This means that no buffer memory is required in the Data Output Interface.

More information about the data transfer from the FPIX2 to the Pixel Data Combiner Board can be found in Sergio Zimmermann's presentation to this conference[4].

8 Programming Interface

The initialization and control of FPIX2 uses three pairs of bussed lines called shift control, shift in, and shift out. Control I/O is synchronous and is clocked by the BCO clock. Each FPIX2 has a 5-bit chip identification number, which is set by wire bonds on internal bond pads. All control communication takes the form illustrated in Fig. 6. Commands can be addressed to a single chip, or broadcast (using the "wild

card" chip number) to all chips sharing a bus. Similarly, a command can refer to a specific register, or to all registers. Only five instructions have been implemented. They are:

- Write (followed by 2,8, or 2816 bits of data)

- Set (all bits in a register = 1)

- Read

- Reset (all bits in a register = 0)

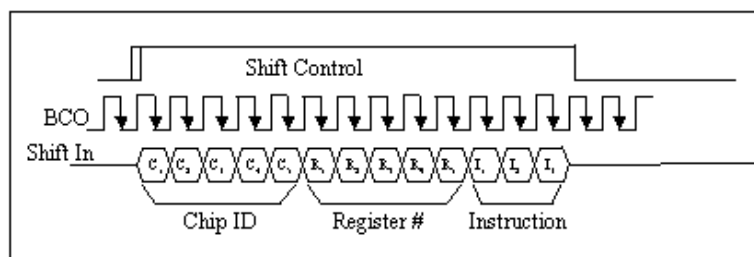- Default (set register to default value)

Figure 6: Command Format.

9 Registers and DAC's

Twenty-three of 32 possible registers are used in FPIX2. Fourteen of these are 8-bit registers that control DAC's. These DAC's are used to set bias currents and voltages and comparator thresholds. Two of the registers are serpentine registers (kill and inject) running up and down the pixel columns, with one bit in each pixel. These two registers control which pixels are disabled, and which pixels can receive a test input. Finally, six registers control facets of chip operation, such as the number of serial output links to be used.

10 Summary

The logical structure of FPIX2 is summarized in Fig. 7. All of the circuit blocks have been tested in a series of small chips. The full sized FPIX2 was submitted to TSMC for fabrication in October, 2002, and is expected to be received at Fermilab before the end of 2002. More information about the development of FPIX2, including the results of radiation damage tests, can be found in references 5-7.
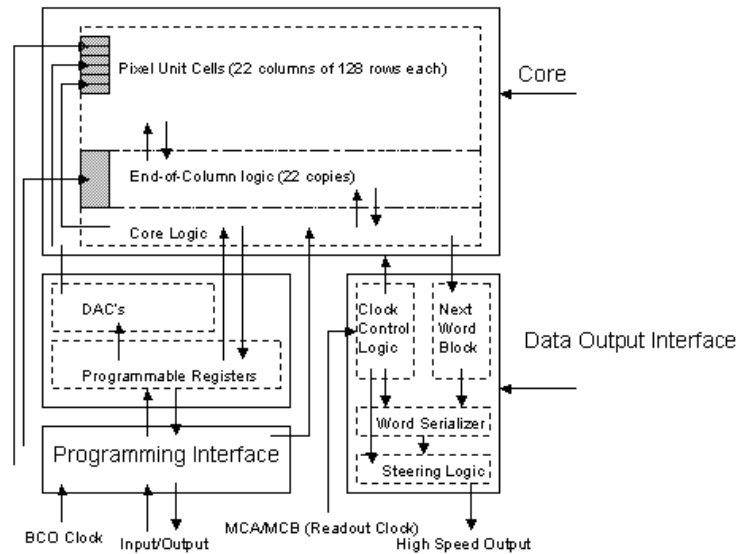
Figure 7: FPIX2 Block Diagram.

References

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