The Read-Out system of the ALICE pixel detector

Kluge, A.
for the ALICE SPD collaboration

CERN, CH-1211 Geneva 23, Switzerland

Abstract

The on-detector electronics of the ALICE silicon pixel detector (nearly 10 million pixels) consists of 1,200 readout chips, bump-bonded to silicon sensors and mounted on the front-end bus, and of 120 control (PILOT) chips, mounted on multi chip modules (MCM) together with opto-electronic transceivers. The environment of the pixel detector is such that radiation tolerant components are required. The front-end chips are all ASICs designed in a commercial 0.25-micron CMOS technology using radiation hardening layout techniques. An 800 Mbit/s Glink-compatible serializer and laser diode driver, also designed in the same 0.25 micron process, is used to transmit data over an optical fibre to the control room where the actual data processing and event building are performed. The read-out system and the tests performed are described.

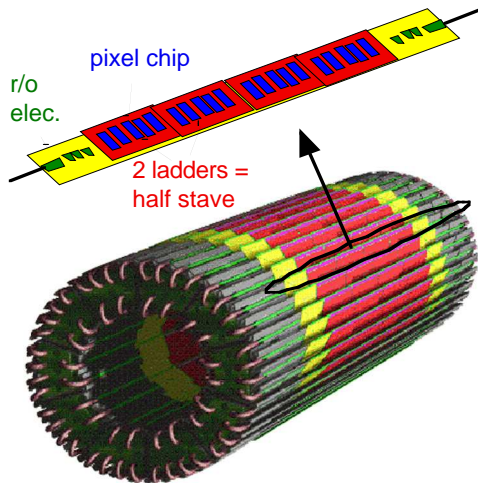## I. INTRODUCTION

A. Detector

Figure 1: ALICE Silicon Pixel Detector

Two ladders (5 pixel chips each), mounted on a front-end bus, constitute a half-stave. The complete detector consists of 120 half-staves on two layers, 40 half staves in the inner layer, 80 in the outer layer. The detector is divided into 10 sectors (in ϕ-direction). Each sector comprises two staves in the inner layer and four staves outer layer. Thus one detector sector contains six staves. Fig. 1 illustrates the ALICE silicon pixel detector. [1, 2]

B. Design considerations

Table 1 summarizes the main design parameters of the readout system.

Table 1: System parameters

L1 latency	6 µs
L2 latency	100 µs
Max. L1 rate	1 kHz
Max. L2 rate	800 Hz
Radiation dose in 10 years	< 500 krad
Neutron flux in 10 years	$2 \times 10^{12} cm^{-2}$
Total number of pixels	9.8184×10^6
Occupancy	< 2%

Although the L1 trigger rate and the L2 trigger rate are low compared to other LHC experiments, the raw data flow yields almost 1 GB/s.

The expected radiation dose and the neutron flux are at least one magnitude of order lower compared to the ATLAS or CMS experiments. However, commercial off-the-shelf components can still not be used. Therefore, the ASICs have been developed in a commercial 0.25-micron CMOS technology using radiation hardening layout techniques [3]. Precautions have been undertaken to reduce malfunction due to single event upset. A minimum of data processing is performed on the detector, which subsequently simplifies ASIC developments.

II. SYSTEM ARCHITECTURE

A. System overview

Fig. 2 shows a block diagram of the system electronics. The 10 pixel chips of one half stave are controlled and read out by one PILOT multi chip module (MCM). The PILOT MCM transfers the data to the control room. In the control room 20 9U-VME-based router cards, two for each detector sector, receive the data. One router card contains six link receiver daughter boards, one for two half staves. The link receivers process the data and store the information in an event memory. The router merges the hit data from 6 half staves into one data block and stores them into a memory where the data wait to be transferred to the ALICE data acquisition (DAQ) over the detector data link DDL [4].
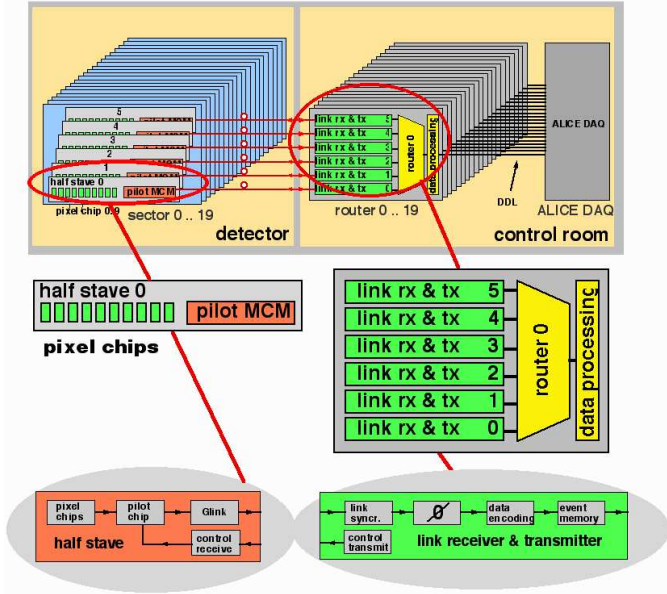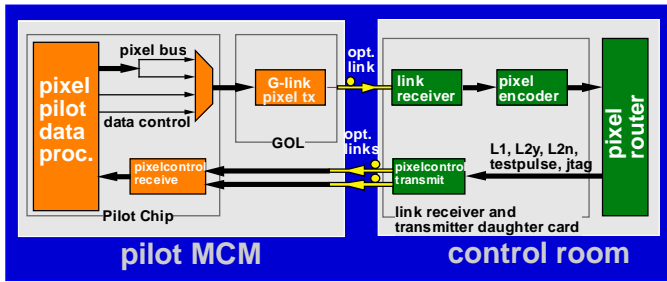
Figure 2: System block diagram

Figure 3: Read-out chain

B. On detector pilot system - OPS

Fig. 3 illustrates a block diagram of the read-out chain. When the ALICE DAQ issues a L1 trigger signal, the pixel router forwards the signal via the pixel control transmitter on the link receiver and transmitter card and the pixel control receiver in the PILOT chip. The PILOT chip asserts a strobe signal to all pixel chips [5], which stores the delayed hit information into one out of four multi event buffers in the pixel chips. Once a L2 accept signal (L2y) is asserted and transmitted to the detector, the PILOT chip initiates the readout procedure of the 10 pixel chips one after the other. The 256 rows of 32 pixels of a pixel chip are presented sequentially on a 32-bit bus. The read-out clock frequency is 10 MHz. As a result, the read-out of 10 chips takes about 256 μs.
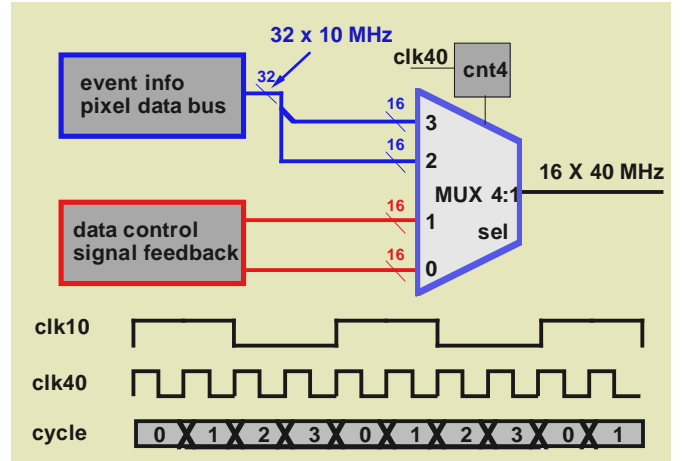

Figure 4: Transmission principle

The PILOT logic performs no data processing but directly transmits data to the control room. This approach has several advantages. The first is, that the on detector PILOT-ASIC architecture is simple. Secondly, the system becomes more reliable as the complex data processing units are accessible during operation in the control room. Finally, if the detector hit occupancy increases in the future, more eleaborate data compression schemes can be adapted in the FPGA based control room located electronics.

For the optical transmission of the data to the control room the encoder-serializer gigabit optical link chip GOL [6] is used. The GOL allows the transmission of 16 bit data words every 25 ns resulting in an 800 Mbit/s data stream. The data are encoded using the Glink [7] protocol.

The pixel data stream arrives from the pixel chips at the PILOT chip on a 32-bit bus in 100 ns cycles. That means that the transfer bandwidth of the GOL is twice as high as required. The 100 ns pixel data cycle is split up into four 25 ns GOL transmission cycles. Fig. 4 shows the transmission principle. In two consecutive GOL cycles, 16 bits of pixel data are transmitted. The remaining two transmission cycles are used to transmit data control and signal feedback signal blocks. The control block contains information directly related to the pixel hit data transmission, such as start and end of transmission, error codes, but also event numbers. In the signal feedback block, all trigger and configuration data sent from the control room to the detector are sent back to the router for error detection.

Upon receipt of a L2 reject (L2n) signal the corresponding location in the multi event buffer in the pixel chips are cleared and the PILOT initiates a short transmission sequence to acknowledge the reception of the L2n signal.

C. Link receiver

The serial-parallel converter receives the Glink data stream and recovers the 40 MHz transmission clock using a commercial component [8]. The implementation of the link receiver is based on a commercial FPGA and dual port memories. Fig. 5 shows a block diagram of the link receiver. The received data is checked for format errors and the data are

loaded into a FIFO. The expected occupancy of the detector will not exceed 2%. As a result, it is economic to encode the raw data format after zero suppression. In the raw data format the position of a hit within a pixel row is given by the position of logic '1' within a 32-bit word. The encoder transforms the hit position into a 5-bit word giving the position as a binary number for each single hit and attaches chip and row number to the data entry [9]. The output data from the FIFO are encoded and stored in an event memory in a data format complying with the ALICE DAQ format [10]. There it waits until merged with the data from the remaining five staves by the router electronics.

Figure 5: Link receiver block diagram

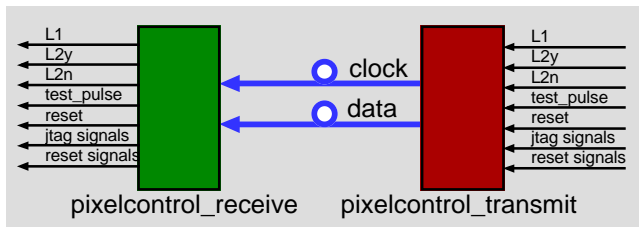## D. Pixel control transmitter and receiver
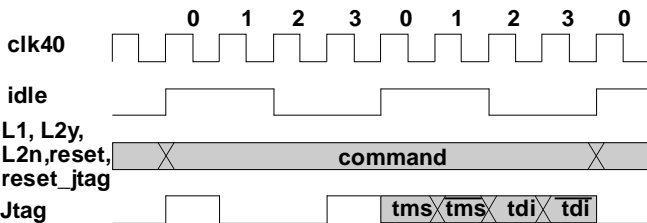

Figure 6: Pixel control block diagram

Figure 7: Pixel control data format

The pixel control transmitter and receivers are responsible for the transmission of the trigger and configuration signals from the control room to the detector. This includes the following signals: L1, L2y, L2n trigger signals, reset signals, a test pulse signal and JTAG signals.

The data must arrive at the detector in a 10 MHz binning, since the on detector PILOT system clock frequency is 10 MHz. The link is unidirectional since the return path for the JTAG system (TDO) uses the Glink data link. The data protocol must be simple in order to avoid complex recovery circuitry on the detector in the PILOT chip and all commands must be DC balanced. (The number of '1's and '0's in the command code must be equal.)

The data transmission is performed using two optical fibres, one carrying the 40 MHz clock and the other the actual data.

The pixel control transmitter (see fig. 6) translates the commands into a serial bit stream. A priority encoder selects the transmitted signal in case two commands are asserted at the same time. L1 is the only signal where the transmission

latency must be kept constant. Therefore, a L1 trigger transmission must immediately be accepted by the pixel control transmitter and, thus, has highest priority. A conflict would arise if the transmitter were in the process of sending a command at the same time as a L1 transmission request arrives. In order to avoid this situation the L1 trigger signal will always be delayed by the time duration, it takes to serialize a command (200 ns). During this delay time, all command transmissions are postponed to after the L1 signal transmission. Thus, when the delayed L1 trigger signal arrives at the transmitter, no other command can be in the transmission pipeline.

Fig. 7 illustrates the data protocol. Four 40 MHz clock cycles form a command cycle. At start-up 64 idle patterns are sent to the receiver. The receiver synchronizes to this idle pattern. Commands are always two transmit cycles (or eight 40 MHz cycles) long. The number of different commands requires a two transmit cycle command length. After each transmission of an idle word, a transmission command can follow. Since the idle word is only 100 ns long, the transmission of a command can be started in a 100 ns binning. However, the duration of a command transmission is 200 ns long [11].

III. ASIC Development

Fig. 8 shows an illustration of the PILOT MCM. Due to mechanical constraints, the MCM must not exceed 50 mm in length and 12 mm in width. A special optical package is being developed, which is less than 1.2 mm in height and houses two pin diodes and a laser diode [14].

Due to the height constraints, all components on the MCM must not exceed 1.2 mm in height. Fig. 8 shows the GOL, which must be in close vicinity to the optical package in order to keep the 800 Mbit/s transmission line short. The distance from the connector to the GOL is less critical, as only 40 Mbit/s signals are connected to the optical package. On the very left, the analog PILOT chip is shown. It is an auxiliary chip for the pixel chips and provides bias voltages and allows the measurement of supply and bias voltages.

All chips have been produced in a 0.25 micron CMOS technology using special layout techniques to enhance radiation tolerance [3].
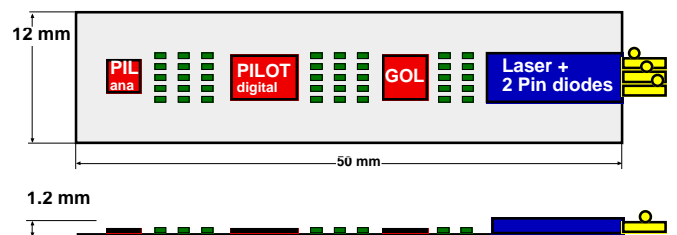

Figure 8: PILOT MCM

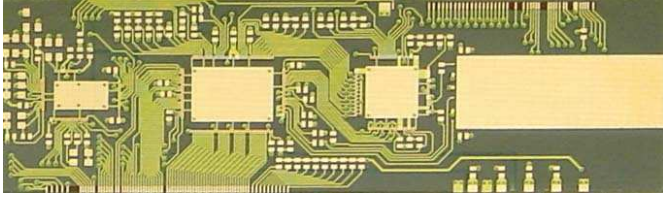Fig. 9 shows a picture of a first prototype of the pilot MCM.

Figure 9: Prototype PILOT MCM

A. PILOT chip

The prototype PILOT chip layout can be seen in fig. 10. The chip size of 4 x 6 mm is determined by the number of I/O pins. A comprehensive description of the PILOT chip can be found in [11, 15]. As described later, the chip has successfully been tested.
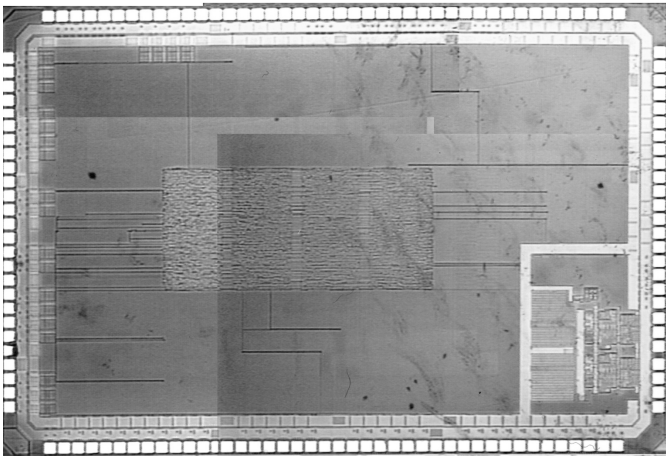

Figure 10: PILOT layout

B. GOL chip

The GOL is a serializer chip which complies to either 8b/10b encoding or to the Glink standard. It can serialize into a 800 Mbit/s or 1.6 Gbit/s data stream. We use the Glink mode with the 800 Mbit/s transmission rate. The final version of the GOL chip has already been tested and its performance is described in [6]. The layout of the chip is shown in fig. 11.
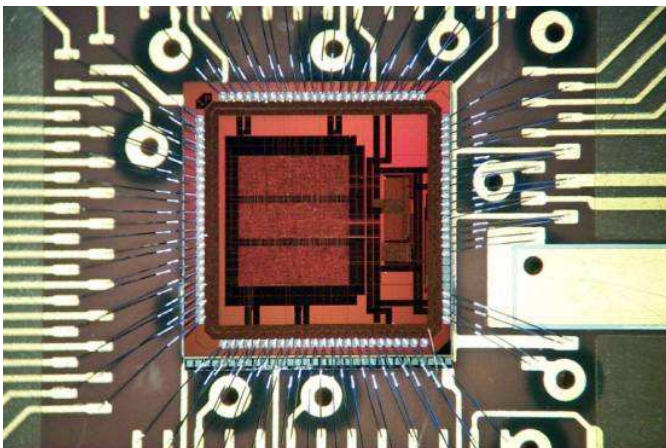

Figure 11: GOL chip

C. Analog PILOT chip

The analog pilot chip provides bias voltages to the 10 pixel chips on a half stave and allows the measurement of supply and bias voltages. Communication is established via the JTAG interface which is connected to the pilot chip. The chip has successfully been tested. The chip can be seen in fig. 11. It has the size of 2 x 4 mm.
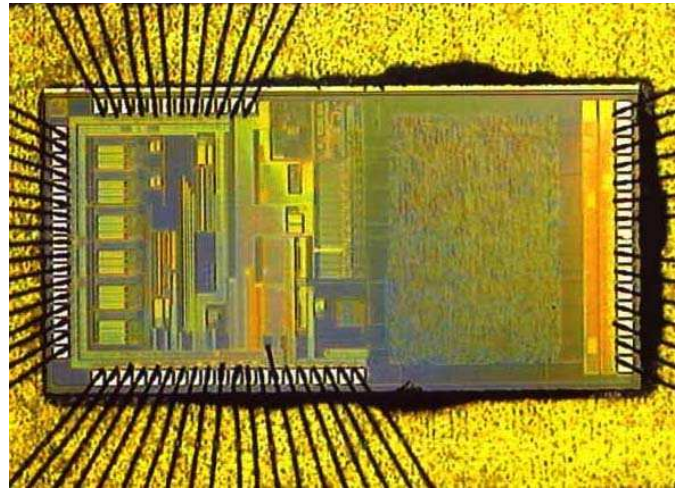

Figure 12: Analog PILOT chip

D. Optical package

A special optical package containing two PIN diodes for the clock and the serial trigger and configuration data and a laser for the G-Link data stream has been developed. The component is only 1.2 mm high. An illustration can be found in fig. 13.
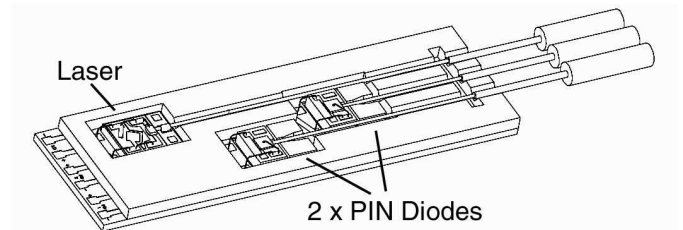

Figure 13: Optical package (16 mm x 6 mm x 1.2 mm)

E. Single event upset

Although the expected neutron fluence is comparatively low, design precautions have been undertaken to prevent single event upsets from causing malfunctions. In both the PILOT chip and the GOL chip, all digital logic has been triplicated and all outputs are the result of majority voting. Internal state machines are made in a self-recovering manner. Fig. 14 shows the principle. In case a flip-flop in a state machine changes its state due to a single event upset, the correct state will be recovered using the state of the remaining two state machines.
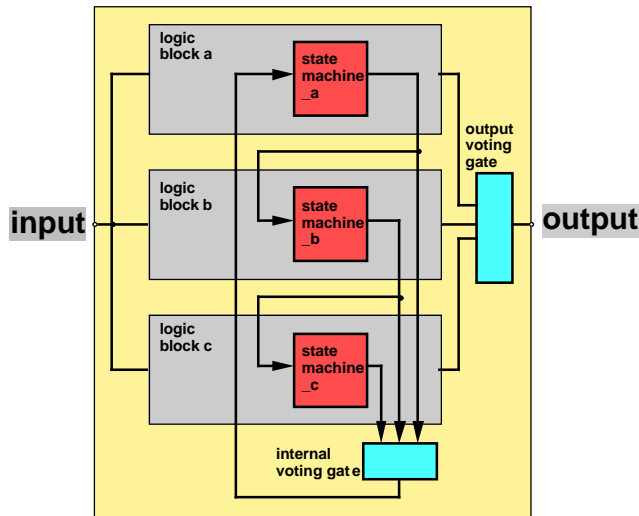
Figure 14:   SEU recovery architecture

IV.   SYSTEM TESTS

A. On detector PILOT system test board

An on detector PILOT system (OPS) test board has been developed. The board is used to test the functionality of the PILOT chip and the entire read-out chain including the pixel chip, the pilot chip, the GOL, the optical link, the deserializer chip. In addition it allows the test of the FPGA based link receiver logic. Although the control room located electronics does not exist yet physically it was emulated in the FPGA. The proper functionality of the read-out system was successfully tested using this test system.

The PILOT chip is directly glued and bonded onto the board. An FPGA [16] provides the test patterns to the PILOT. In the initial test phase the pilot chip only was tested. The FPGA contains functional models of the pixel control transmitter, the ten pixel chips and the link receiver. The outputs of the PILOT chip are stored in a 128k x 48 static memory bank and can also be read back by the FPGA for comparison with the model. Access to the board, the FPGA and the RAM bank is established via a JTAG port. Fig. 15 shows the block diagram of the board. In a second phase, the test included the PILOT chip, the GOL transmitter chip and the commercial Glink receiver chip [8]. Again, the output of the data chain was read into the FPGA and the memory bank. In a third phase a pixel chip was connected to the board. This feature allowed qualification of the entire data read-out chain. All components visible in the block diagram in fig. 3 and the communication between them could successfully been tested.
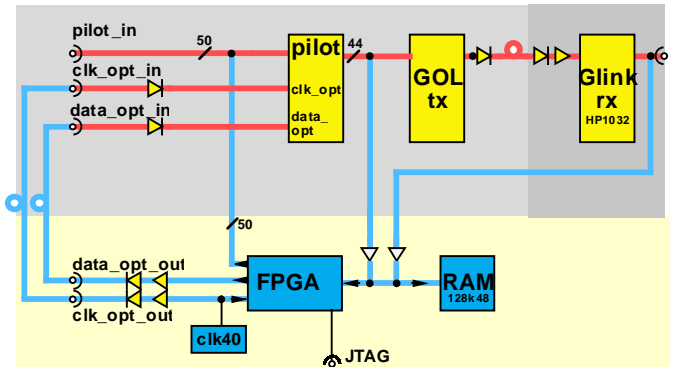

Figure 15:   PILOT system test board

Fig. 16 shows a picture of the test board. The optical components shown used are not the final components.
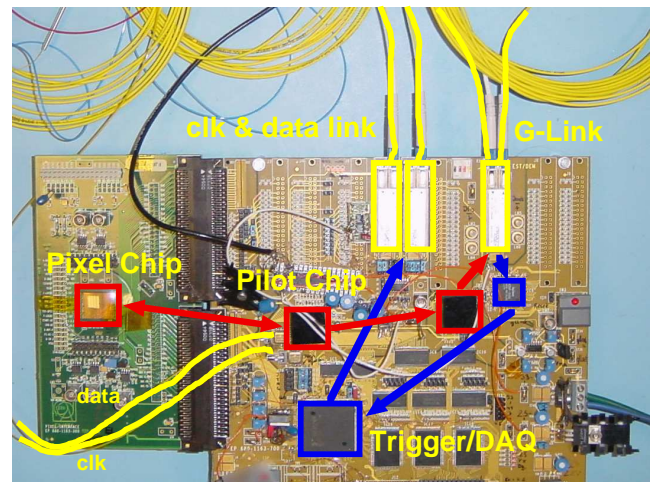

Figure 16:   PILOT system test board

B. System test card RUDOLF

A VME based test system (Rudolf) which allows to test the MCM and the control room located FPGA based link receiver and transmitter daughter card in their final versions has been developed. This setup allows the test of the prototype components but also the test of the final components for production tests. Fig. 17vmoechte shows a block diagram of the card. Again FPGAs allow to send test patterns via the optical links to the MCM. Returning data is either stored in the memory bank or directly compared on-line in the FPGA.
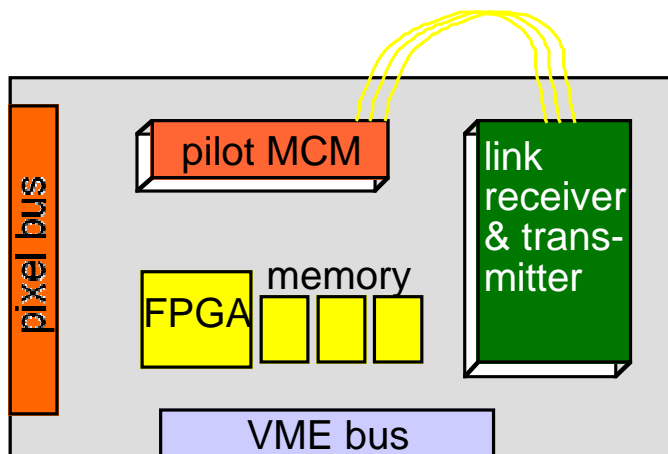
Figure 17:   PILOT system test board

V. CONCLUSION

All chip developments have been conducted using a 0.25-micron CMOS technology and layout techniques in order to cope with the radiation dose. The on detector PILOT system performs no data processing nor requires on-chip memory. The entire data stream can be moved off the detector using the encoder and serializer chip GOL. This has the advantage that the on-detector electronics is independent from the detector occupancy and future upgrades can be performed on the FPGA based electronics located in the control room. The transmission of data is performed using optical links. The number of electrical read-out components is minimized, as the available space for physical implementation is very limited.

The read-out architecture has been proven to be working efficiently in the test systems. Prototype versions of all electronic components exist and have successfully been tested individually but also embedded in the full system. The physical implementation of these components in their final form remains as a final demanding challenge.

VI. REFERENCES

[1] M. Burns et al., The ALICE Silicon Pixel Detector Readout System, 6th Workshop on Electronics for LHC Experiments, CERN/LHCC/2000-041, 25 October 2000, 105.

[2] ALICE collaboration, Inner Tracking System Technical Design Report, CERN/LHCC 99 –12, June 18, 1999.

[3] F. Faccio et al., Total dose and single event effects (SEE) in a 0.25 µm CMOS technology, LEB98, INFN Rome, 21-25 September 1998, CERN/LHCC/98-36, October 30, 1998, 105-113.

[4] György Rubin, Pierre Vande Vyvre, The ALICE Detector Data Link Project, LEB98, INFN Rome, 21-25 September 1998, CERN/LHCC/98-36.

[5] K. Wyllie et al., A pixel readout chip for tracking at ALICE and particle identification at LHCb, Fifth workshop on electronics for LHC

Experiments, CERN/LHCC/99-33, 29 October 1999, 93

[6] P. Moreira et al., G-Link and Gigabit Ethernet Compliant Serializer for LHC Data Transmission, N S S 2 0 0 0 P. Moreira et al., A 1.25 Gbit/s Serializer for LHC Data and Trigger Optical links, Fifth workshop on electronics for LHC Experiments, CERN/LHCC/99-33, 29 October 1999, 194.

[7] R, Walker et al., A Two-Chip 1.5 GBd Serial Link Interface, IEEE Journal of solid state circuits, Vol. 27, No. 12, December 1992, Agilent Technologies, Low Cost Gigabit Rate Transmit/ Receive Chip Set with TTL I/Os, H D M P - 1 0 2 2 , H D M P - 1 0 2 4 , http://www.semiconductor.agilent.com, 5966-1183E(11/99).

[8] Agilent Technologies, Agilent HDMP-1032, HDMP-1034, Transmitter/Receiver Chip Set, http://www.semiconductor.agilent.com, 5968-5909E(2/00).

[9] T. Grassi, Development of the digital read-out system for the CERN Alice pixel detector, UNIVERSITY OF PADOVA – Department of Electronics and Computer Engineering (DEI), Doctoral Thesis, December 31, 1999.

[10] A. Kluge, Raw data format of one SPD sector, to be submitted as ALICE note, http://home.cern.ch/akluge/work/alice/spd/spd.html.

[11] A. Kluge, Specifications of the on detector pixel PILOT system OPS, Design Review Document, to be submitted as ALICE note, http://home.cern.ch/akluge/work/alice/spd/spd.html.

[12] F. Meddi, Hardware implementation of the multiplicity and primary vertex triggers from the pixel detector, CERN, August 27, 2001, Draft, to be submitted as ALICE note.

[13] V. Arbet-Engels et al., "Analogue optical links of the CMS tracker readout system, Nucl. Instrum. Methods Phys. Res., A 409, pp 634-638, 1998.

[14] Private communication with G. Stefanini.

[15] A. Kluge, The ALICE pixel PILOT chip, Design Review document, March 15, 2001, to be submitted as ALICE note, http://home.cern.ch/akluge/work/alice/spd/spd.html.

[16] Xilinx, XC2S200-PQ208.

[17] Morel M., The ALICE pixel detector bus, http://home.cern.ch/Morel/documents/pixel_carrier.pdf http://home.cern.ch/Morel/alice.htm