Eutectic Sn/Pb Fine-Pitch Solder Bumping and Assembly for Rad-Hard Pixel Detectors

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Abstract

A number of new particle physics experiments due to come online in the next few years will be relying on pixel detectors as the means of tracking the elementary particles generated by a collision event. The pixels on these detectors are very small in size (50_m pitch) to provide adequate spatial resolution for particle tracking, and the detectors must be reliably produced in large numbers in order to cover the necessary 3-D space in which interactions take place. The size of these pixels present challenges for the interconnect method, and necessitates a fine-pitch solder bumping and assembly process. The methods for fabricating bumps and assembling the detectors must have a high yield and be compatible with a high radiation, high vacuum, and low temperature operating environment to provide the necessary performance and operating lifetime.

MCNC (Research Triangle Park, NC) has developed a fine-pitch Sn/Pb solder bumping process that is capable of reliably fabricating 25_m bumps on 50_m pitch, as well as flip-chip assembly methods that allow the construction of multi-chip modules of sensor – readout circuit pairs. This paper presents an overview of MCNC's bumping and assembly processes and the results of our ongoing collaboration with Fermilab (BTeV) and Northwestern University (US-CMS) for bumping and assembling pixel detector modules on 50_m pitch (Fermilab) and 100_m pitch (NU) and the performance of these modules as tested by Fermilab and NU.

Introduction

The use of flip chip packaging has increased greatly in the past 5 years, finding wide use in consumer electronics (i.e. hand-held devices), military systems, and other specialized and mainstream packaging applications. While flip chip technology has been around since the mid-1970's, it has been only recently that commercial-volume wafer bumping suppliers have become available and that manufacturers have taken advantage of the smaller size, higher I/O counts, and improved electrical performance that flip chip offers. Currently, commercially available wafer bumping typically deals with devices with I/O pitches of 150_m to 250_m for true flip chip applications. However, there are growing niche markets for fine-pitch wafer bumping for devices with I/O pitches of 100_m and less. One of the first mature applications to require fine-pitch bumping is in the high-

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energy physics (HEP) community, where several new experiments are relying on large numbers of pixilated sensor devices to be mounted to readout integrated circuits (ROIC), which make up the detectors that track collision events. The size of the pixels is typically 50_m to 100_m in one length direction, and the associated wafer bumping, handling, and assembly of these devices becomes considerably more difficult compared with most commercial applications. Not only are there issues with the I/O pitch, but also the sensor wafers, which typically have contacts on both sides and are thinned, require a process that is compatible with them. Additionally, the process must also be able to withstand a thinning process applied to the ROIC wafers before assembly to the sensor devices.

MCNC (Research Triangle Park, NC), for the past ten years, has been a leader in the development of wafer bumping and assembly technologies. MCNC was recently a participant in the DARPA-funded Seamless High Off-Chip Connectivity (SHOCC) program, with the objective of developing and evaluating flip chip bumping and assembly processing down to 50_m pitch devices (25_m bump size), a 5X decrease in what was the current market state-of-the-art when the program began. MCNC's success in developing this technology has made available an I/O density of 40,000 interconnections/cm^2 for leading edge applications.

MCNC is currently working with two groups to provide wafer bumping and assembly of fine-pitch devices. The BTeV experiment, which will be installed at Fermi National Accelerator Lab, is using pixilated sensors with 50_m pitch, and will require nearly 1800 multi-chip ROIC-sensor modules for the full detector. The US-CMS project, which will be installed at the LHC at CERN, is using sensors with 100_m pitch, and will also need hundreds of modules for the detector. This paper presents details of the MCNC bumping and assembly processes, and will attempt to serve as a guide for other groups looking to take advantage of this technology. Also, the results of our ongoing collaborations with the BTeV and US-CMS groups will be presented, substantiating the application of these processes in ROIC-sensor module production.

Wafer Bumping Process

MCNC's wafer bumping process relies on a unique combination of process conditions and materials that have been engineered to provide uniform and robust solder bumps. The process relies on an electroplating method to form the solder bumps, which gives tremendous flexibility in processing conditions and excellent wafer-level uniformity. Figure 1 shows a cross-sectional view of a wafer section as the process progresses.

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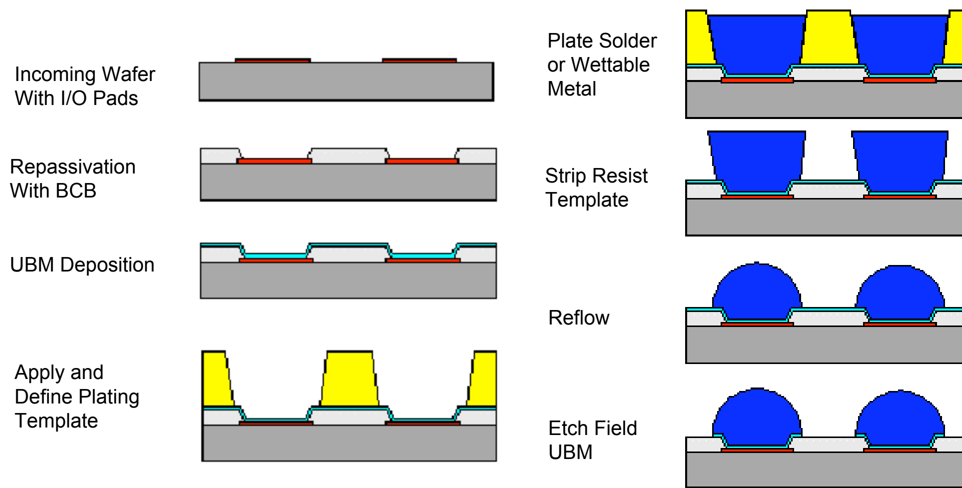

Figure 1: Wafer Cross-Sections Through the Bumping Process

Incoming wafers are given a thorough inspection to identify any damage or problems that may impact the wafer bumping process. Special attention is given to common defects such as deep scratches, large particles, and I/O pad damage due to wafer probing. Also during this incoming inspection, a solvent clean is done using acetone and isopropyl alcohol to remove any particles or marks on the wafers before beginning the bumping process. During this solvent clean, any ink dots on die will be removed, if possible, due to their possible impact on later processing.

After incoming inspect and clean, the wafers are repassivated with an organic spin-on polymer called BCB (benzocyclobutene), which is manufactured by Dow Chemical under the trade name Cyclotene™. Cyclotene (www.cyclotene.com) has very good electrical properties (dielectric constant = 2.7) and high frequency performance, has extremely low moisture uptake, and has low cure temperatures when compared with other organic passivations. Once applied, the BCB is then imaged and developed to create via holes over the I/O pads to be bumped. The application of the BCB provides a number of benefits. First, the BCB becomes the device final passivation, and is pinhole-free, alleviating concerns with the device final passivation. Second, the BCB serves to planarize the wafer surface and provide a uniform base over which the bumps will be formed. Third, the BCB provides a stress buffer between the bumps and the wafer surface, resulting in increased thermo-mechanical reliability.

In the case of the ROIC devices used by BTeV and US-CMS, there are also wirebond pads that must remain accessible after the bumping process is complete. We have developed a dry etch process that reopens these pads after the bumping process is complete. Once the BCB polymer is removed no other preparation before wirebonding is necessary.

After repassivation, a blanket Under Bump Metallurgy (UBM) is deposited on the wafer. The UBM is a carefully engineered metal stack that serves several purposes. First, the

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UBM provides the mechanical interface between the solder bump and the I/O pad. Second, the UBM provides a seed layer that is both solder-wettable (to mechanically join the solder to the UBM) and low resistance (for good wafer-scale electroplating uniformity). Third, the UBM provides a diffusion barrier between the I/O pad and the other metals in the UBM and solder system.

Abrupt changes or sharp features in the topography of the I/O pad metal have a detrimental impact on the UBM's ability to provide a robust connection between the I/O pad and solder bump. Previously mentioned, I/O pad damage due to wafer probing is the most common cause of these discontinuities. Typically, wafer probing is done after the IC fabrication to check functionality and yield. If the scraping action of the probe tip on the I/O pad pushes up excessive amounts of the metal, discontinuities can exist in the UBM, which can lead to failure of the pad or bump. It is therefore important that wafer probing done over proposed bump locations be done with a minimum of disturbance to the I/O pad. Judicious choice of probing locations and parameters, as well as the application of BCB to the wafer, help to eliminate this possible problem.

Once the UBM is deposited, a thick photoresist is applied to the wafer and patterned to create openings down to the UBM. This is a very uniform process, as significant deviations in the size of these openings leads to non-uniform solder bump sizes in the final product. Solder is then electroplated in these openings to a height calculated to provide the necessary final reflowed bump height. MCNC has developed special techniques for the plating of fine-pitch patterns that result in uniform plating over wafers up to 8" in diameter.

Once the solder has been plated, the photoresist plating template is removed in a solvent cleaning step, and the wafer is reflowed to form a strong intermetallic bond between the solder and the UBM. After reflow, the UBM field metal is etched away using a carefully controlled process that minimizes the amount of undercut to the bumps. Controlling undercut of the solder bumps is of paramount importance in fine pitch designs. Whereas commercial-pitch applications can withstand bump undercuts on the order of a few microns, due to the large base diameter of the bump, that amount of undercut on 25_m bumps results in an unacceptable decrease in bump strength. MCNC's UBM etch process keeps the undercut to less than 2_m, leaving an ample bump base intact to provide the necessary mechanical strength.

If the I/O pads are not properly located, they can be "redistributed" prior to the standard bumping process. Redistribution involves the deposition of metal traces that connect the original I/O pad with a new pad where the bump will be located. This process is particularly advantageous for sensor applications where elongated pixels are utilized where two ROIC chips are mounted next to each other. With redistribution the pixel size can remain constant and the connections to those pixels can be moved to other locations on the sensor and ROIC devices. Redistribution can also be used to convert perimeter-array I/O designs into area-array designs, to take advantage of relaxed pitch afforded by area-array I/O's, or the reverse can be done, in order to leave areas free of solder bumps.

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For sensor-ROIC applications there are two separate wafers to be processed, the sensor wafer, which is usually thinned and has contacts on both sides, and the ROIC, which is a standard unthinned CMOS wafer. MCNC processes these wafers in similar ways, but they differ in the handling and metalizations applied. The ROIC wafers are processed as outlined above with electroplated solder and the BCB is removed from the wirebond pads after the bumping is complete. The sensor wafers follow the same process as the ROIC's until they reach the electroplating step. Rather than apply solder to the sensor wafers, a Ni/Au bond pad metallization is electroplated, which provides a wettable metal for the solder on the ROIC devices to join to. The Au on the bond pad provides protection against oxidation for the Ni, and the bond pads require no pretreatment before the flip chip assembly process. The amount of Au on the bond pads is kept to a minimum to inhibit Au-induced embrittlement from occurring in the solder.

Post-Bumping Processing

Before assembly of the sensor-ROIC modules, there are several issues that must be addressed. Generally, the ROIC wafers need to be thinned to approximately 200_m before assembly. Both types of wafers must be diced, and each has its own particular set of challenges.

For ROIC wafer thinning, preserving the integrity of the bumps during the thinning process is of primary concern. Wafer thinning processes all require some method of fixing the front side (bumped side) of the wafer to a holder while material is removed from the back side. Despite vendors' assurances that their processes were compatible with bumped wafers, we found that all had difficulty avoiding bump damage on unprotected wafers during our initial qualifications. This was not completely unexpected, and served to further illustrate the difficulties in handling and working with fine-pitch bumped wafers. In order to prevent bump damage during the thinning process, MCNC developed a front side protective coating process that provides adequate defense against bump damage without hampering the vendor's front side fixturing procedure.

We also have seen vendors have trouble with breakage when thinning 8" wafers. In discussions with industry experts, they attribute this breakage to unrelieved stresses induced in the Si matrix from the grinding process. Polishing the wafers after grinding helps remove stress and minimize the chance of breakage. The majority of vendors we have worked with in the past either do not polish after the grind, or did not when they were initially approached during early qualification. We are working with a source that does use a post-grind polish and are continuing to integrate their service with our bumping process.

Dicing for sensor-ROIC applications requires a level of care not normally needed in the dicing operation. Since the ROIC devices are placed in such close proximity to each other when assembling multi-chip detector modules (on the order of 100_m gap between chips on the module), the dicing tolerances are critical. In addition, most sensor wafer layouts are multi-user runs, or consist of dissimilar sizes of pixel arrays that require extensive sub-dicing in order to singulate the parts. MCNC has in-house dicing

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capabilities to provide both tolerance-critical dicing and sub-dicing services required for these unique applications.

Assembly

Fine pitch flip chip assembly requires a precision tool set and well controlled processes in order to achieve a high assembly yield. For the assembly of pixilated detector modules, several ROIC devices must be placed on a single module of multiple sensor arrays. Due to the limited space between sensor arrays on a single module, the placement of the ROIC's must be done with very high precision, so as not to disturb the neighboring chip. In addition, the very nature of fine pitch flip chip assembly makes issues associated with flux residue removal after reflow highly nontrivial. This problem is completely eliminated by the use of MCNC's patented Plasma Assisted Dry Soldering (PADS) process during assembly.

PADS is a plasma treatment process that reacts with the Sn oxides on the surface of Sn-bearing solders. The Sn oxides are converted into a compound that breaks up as the solder melts during reflow, exposing unoxidized solder to the bond pad, allowing full solder wetting to occur. Reflow is done in a conventional nitrogen-inerted belt furnace that prevents the reoxidation of the solder during the bonding process. The PADS process leaves no residues on the chip during treatment or after reflow. The PADS treatment cycle time takes only 5-10 minutes, and parts do not have to be immediately joined after treatment. The storage time of treated parts in air is days long (and even longer in nitrogen), but parts may be treated a number of times with no adverse effects if the dwell time after initial treatment is too long.

PADS is integrated into the assembly process prior to the flip chip bonding. Solder bearing parts are treated, mounted on the flip chip bonder, and then aligned and bonded together. Tacking the bonded parts together, so that one chip cannot shift relative to the other during the process of removing the assembly, is an issue, since flux normally provides this benefit. MCNC has developed proprietary methods of tacking that are compatible with PADS and provide equal or better assembly yield as compared to fluxed assembly.

To perform the flip chip bonding procedure, MCNC has two precision flip chip bonders, a manual tool and a semi-automatic tool. The manual tool has a throughput of approximately 8-12 single chip placements per hour, the semi-automatic tool increases that throughput by 5-10X, depending on the application. These tools also have heated chucks to provide in-situ reflow capability. Both of the tools have placement accuracy of 2_m or less. The placement accuracy of the bonders is critical for sensor-ROIC multi-chip modules where the ROIC chips must be placed extremely close to one another, which, as mentioned previously, is on the order of 100_m. We have successfully demonstrated up to 10 ROIC placements on a single sensor module, which is the highest number of placements so far encountered for either BTeV or US-CMS.

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Once the chips are placed and tacked together, the assembly is transferred to a standard nitrogen-inerted reflow oven to complete the bonding cycle. Peak reflow temperature is between 225°C and 250°C, depending on the materials in the assembly. Depending on the tacking method used, the assembly requires no further processing after reflow other than a methanol rinse.

Application Data

MCNC's fine pitch bumping process has been extensively characterized under numerous conditions. While there are several methods to quantify the quality of wafers that have completed the bumping process, we have found a number of standard tests to be good indicators of the success of the process and the reliability of the bumps.

Individual bump shear and die-to-die tensile pull tests provide failure strength and failure mode information on the strength of the I/O pad-BCB-UBM-solder bump interfacial system. These two tests provide quantifiable means of evaluating the physical integrity of the bump system. Typical bump shear strength on 25µm bumps averages about 3.3 grams with _ = .4 grams. The failure mode is predominately solder shear, with a small amount of lifting at the front of the shear where the tool first contacts the bump.

Bump height measurements show the uniformity of the solder electroplating process. The bump height impacts the yield of the assembly process in that uniform bump heights provide consistent contact to the bond pads on the mating device. MCNC's electroplating process controls wafer-level uniformity to within a 10% standard deviation and controls die-level uniformity even tighter, typically within 5%. To give a specific example, one application has a die size of approximately 1in x 1in, with a targeted bump height of 27µm. The bump height for one wafer from this lot averaged 27.37µm with _ = 2.52, and a die-level uniformity of 4.48%, based on measurements from 10 random die.

Electrical testing of 4-point Kelvin structures or 2-wire resistance measurements of connected bumps provides important information on the metalization process and on various other process steps. Such structures are built into the alignment mark cluster on each design processed and there are at least two of these on each wafer. These Kelvin structures consistently average about 3m_ in a 4-wire test.

Finally, extensive cross-section work has been done on numerous individual chips and joined assemblies to quantify and understand process characteristics that cannot be directly observed or measured. Figure 2 shows a cross-section of two chips with 25µm diameter bumps that have been flip-chip mated. This picture illustrates the excellent bump shape and UBM conformality produced with the process. In addition the via defined by the BCB is clearly visible.

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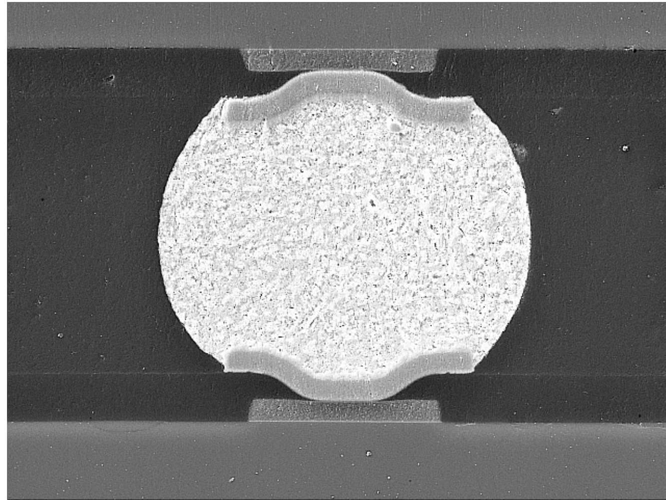

Figure 2: Cross-Section of Joined 25µm Bumps

Results From BTeV Collaboration

MCNC has been working with researchers at Fermilab since 1999 to provide fine-pitch pixel detector bumping and assembly for the BTeV experiment. An internally designed 50µm pitch test vehicle with 25µm bumps, shown in Figure 3, was initially fabricated to provide proof-of-concept data. This test design was populated with daisy chain structures of 14 to 16 bumps, called a channel, which could be electrically probed to provide continuity data, and thus give a direct measurement of the bump assembly yield. Figure 4 shows a cross-section from one of these daisy chain test assemblies showing the excellent alignment and uniform bump shape.

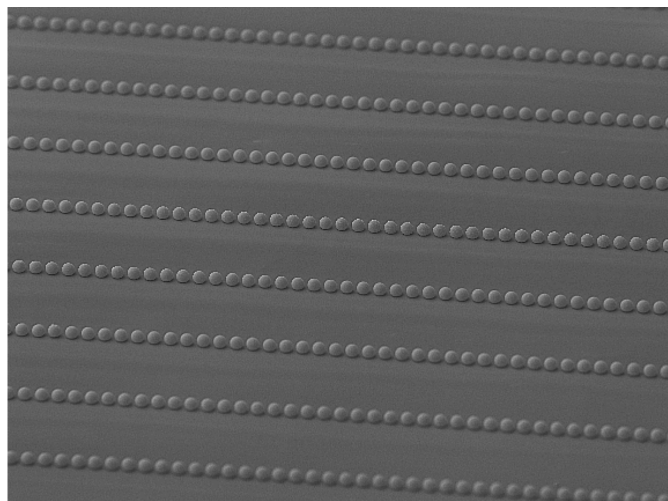

Figure 3: SEM Photo of Fermilab Test Chip

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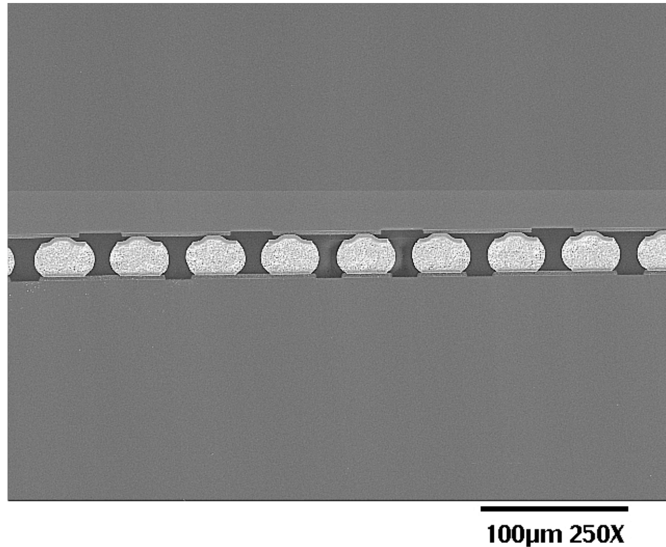

Figure 4: Cross-Section of Fermilab Test Chip Assembly

82 of these single-chip test detectors were delivered to Fermilab where they were electrically tested.[1] The assembly yield measured was 91.5% (75 good out of 82). The seven assemblies failing the assembly yield tests were determined to have failed due to placement errors during the flip-chip bonding process. The remaining 75 good detectors had a channel yield of 99.32% or $6.8x10^{-3}$ failed-channel/channel. Assuming that in the failed channels only one bump joint had failed, the bump yield of the assemblies was 99.95%, or $4.5x10^{-4}$ failure/bump. Investigations of the failed channels after testing showed that the assumption that only one bump joint was bad per failed channel was predominately true. These yields were considered to be adequate for Fermilab's application.

Fermilab has also subjected a subset of these test detectors to thermal cycling and radiation exposure testing.[2] The thermal cycling conditions were 1) cooling to -10°C for 144 hours; 2) heating to 100°C in vacuum for 48 hours. The detectors were measured before starting the cycling and again after the cooling and heating steps. For the radiation exposure, the parts were irradiated by a Cs-137 gamma source to 13 MRad and measured again. The reported failure rates for Known Good Modules (KGM) were $4.6x10^{-5}$ failures/bump after the cooling process and $3.3x10^{-4}$ failures/bump after the heating process. The researchers also cited the possibility that the failure rates may be inflated to some degree because of damage to the probe pads due to repeated probe testing. The failure rate per bump reported after radiation testing on KGM was $1.8x10^{-4}$. Again, this rate may be higher than actual due to damage to the probe pads from repeated probing and also radiation-induced damage to the Al that was observed after exposure to the gamma source. Indeed, it is not clear that the failures attributed to radiation exposure (6 out of 2280 total channels) were not actually due to radiation damage to the Al traces connecting the bumps, rather than damage to the bumps themselves.

We are currently in a prototype production phase with Fermilab, which will continue for approximately the next 18 months while new sensor and ROIC designs are being tested.

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Two successful device runs with 25μm bumps have been completed with functional single and multi-chip detector modules, some with the ROIC chips thinned to 200μm. Figures 5 and 6 show a bumped ROIC and a sensor device with Ni-Au bond pads, both with 25μm base diameter. Fermilab expects to begin a pre-production phase sometime in 2004, which will involve a 10% build of the full detector. This 10% build will require approximately 140 detector modules, with over 800 total sensor-ROIC chip placements on 4-, 5-, 6-, and 8-chip arrays.

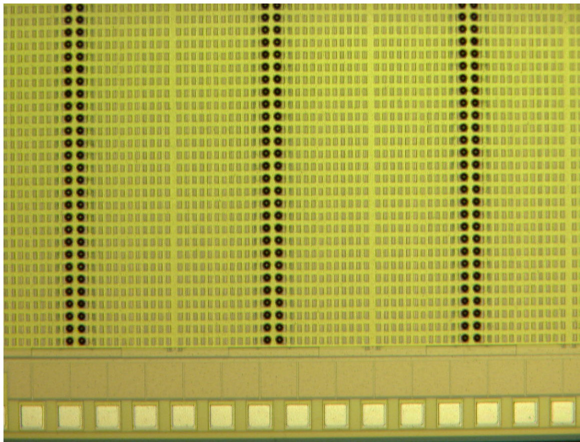

Figure 5: Bumped Fermilab ROIC

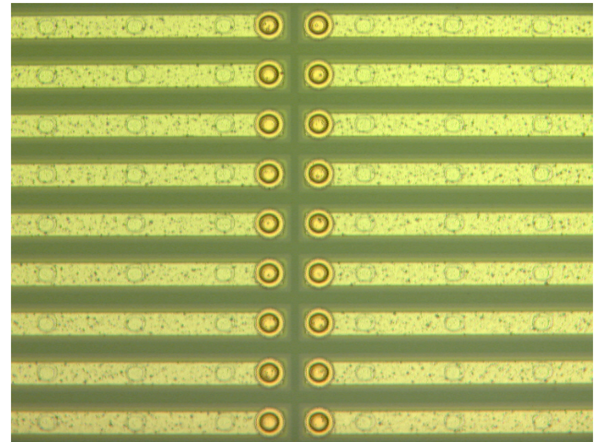

Figure 6: Fermilab sensor with Ni-Au Bond Pads

The pre-production phase will be followed by the full detector build, in which over 1,800 total modules will be built, with over 10,500 total chip placements. This total number of detectors consists of the required modules for the detector plus an additional 30% to be used as spare parts.

Results From US-CMS Collaboration

We have also been working with researchers from the US-CMS project to provide fine-pitch bumping and assembly for their detector modules. Proof-of-concept work was done on another internally generated test design, shown in Figures 7 and 8, which had 50μm bumps on 100μm pitch. Daisy chain channels consisting of 106 electrically connected bumps were built into the test chips so that conductivity tests could be done to determine the assembly and bump yield. Multi-chip modules of 2, 5, 6, 8, and 10 chips were assembled to show the capability of the assembly process. An example of one of these multi-chip modules (MCM) is shown in Figure 9, with two of the test ROIC chips left off to show the bump detail.

A bump yield study was done at The University of California-Davis on several different sizes of modules.[3] A bump yield of .9997 ± .0001 was reported from these measurements, a more than adequate yield for their application. This number is calculated assuming that for any open channel, only one failed bump bond is the cause of

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the open. In investigating samples with open channels, this assumption was shown to be predominately true.

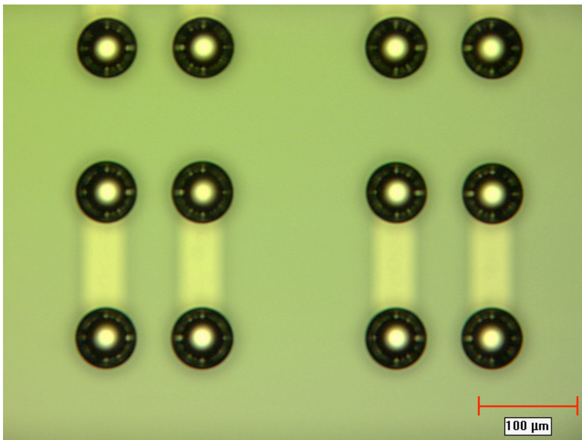

Figure 7: US-CMS Bumped Daisy Chain Test Chip

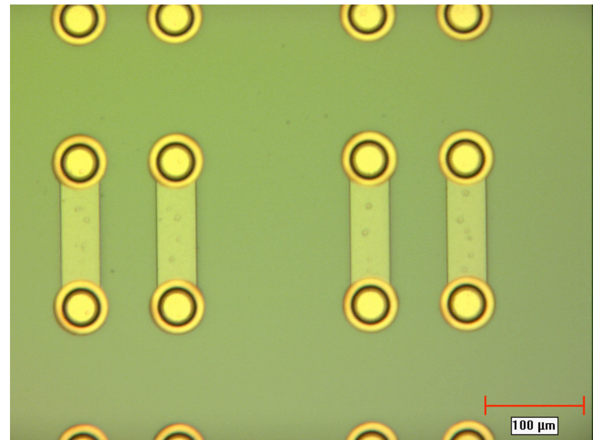

Figure 8: US-CMS Test Chip With Ni-Au Bond Pads

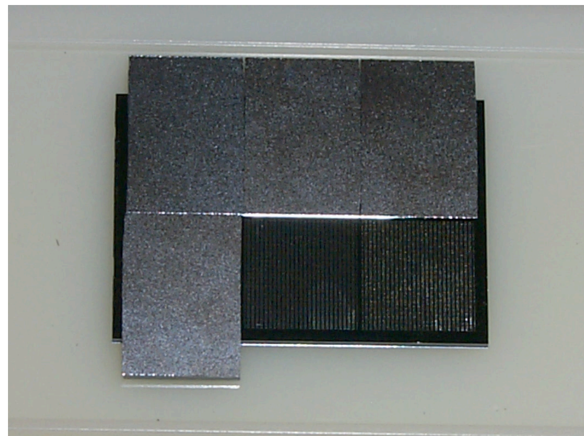

Figure 9: A Partial Build US-CMS Test Design MCM

MCNC expects to continue working with the US-CMS group over the coming months to do wafer bumping and detector module assembly on active sensor and ROIC devices. Although the pixel size will be 100µm, the bump size will be reduced to 25µm to reduce coverage of the sensor area.

Conclusion

MCNC has developed a fine-pitch solder bumping and flip-chip assembly process that has been proven to provide consistent and reliable results. This technology has been shown to meet the pitch and bump size requirements of pixilated particle detectors that are being used in high-energy physics experiments. Our collaborations with the BTeV program and the US-CMS program have shown that the process can be successfully used

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with the sensor and ROIC devices with no impact on functionality. The bump yield, which directly equates to the number of live pixels for a detector assembly, has been measured by both BTeV and US-CMS and shown to be satisfactory. Thermal testing of detector modules indicates that the assemblies will be able to withstand the detector construction and subsequent cool-down/heat-up cycles that will be required. In addition, radiation exposure testing on the bump-bonded detector modules indicates a minimal effect on bump failure rates. Further, the materials used in the bumping and module assembly processes show good compatibility with vacuum environments, where the modules will ultimately be located. Future work with both BTeV and US-CMS is planned, with thousands of multi-chip detector modules to be assembled over the coming years.

References

1. S. Cihangir and S. Kwan; talk presented at 3rd International Conference on Radiation Effects on Semiconductor Materials, Detectors and Devices, Florence, Italy (June. 28-30, 2000).

2. Cihangir, et. al.; talk presented at 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden (Sept. 10-14, 2001).

3. Conversations with Dr. Richard Lander, University of California – Davis.

Acknowledgements

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