IMPROVEMENT OF WAVEFORM EFFICIENCY USING A COMPENSATION CIRCUIT

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Abstract

In order to improve the efficiency(usable RF to total pulse) of a klystron modulator, a system using a solid-state compensation circuit has been developed. This system remarkably improves a flat-top and flatness of the output waveform of the modulator by means of waveform synthesis. This paper presents the design and specifications of the compensation circuit and the results of a preliminary test using a line-type modulator.

1 INTRODUCTION

The power efficiency of the klystron modulator is extremely important. Its improvement is a major challenge in a large scale liner collider such as the Japan Liner collider[1]. The effective output power of the modulator is the power of the flat-top portion of the high-voltage output pulse and hence, the rectangular output pulse is required. In order to realize the rectangular output pulse, we have been developing a system that improves the output waveform of the modulator with a simple method of waveform synthesis[2]. This system, which uses a solid-state compensation circuit, can easily improve an effective flat-top width of the output waveform, resulting in a high power efficiency of the modulator.

2 IMPROVEMENT OF OUTPUT WAVEFORM

Figure 1 shows a basic line-type modulator with a compensation circuit to synthesize the output waveform. The modulator mainly consists of a high-voltage DC power supply, a pulse forming network (PFN), a high-power switch, a pulse transformer and a compensation circuit. The compensation circuit is connected in series to either the primary or the secondary ground side of the pulse transformer. In this figure this circuit is connected to the primary ground side. The output current waveform of the modulator has usually ripples and droop as the solid curve shown in Figure 2(a). They can be improved by adjusting the PFN but it is very difficult to expand usable flat-top part because (1) there is a certain limit determined by PFN circuit parameters and (2) the rise and fall times of the output waveform are also determined by the limitation of time constant of the output circuit including the pulse transformer and klystron. If the compensation circuit produces a waveform to suppress both the ripple and droop, and to expand the flat-top at the rise and fall parts as the broken curve shown in Figure 2(a), and it is synthesized with the output current waveform of the PFN, an effective flat-top width of the output waveform will be significantly improved as shown in Figure 2(b).

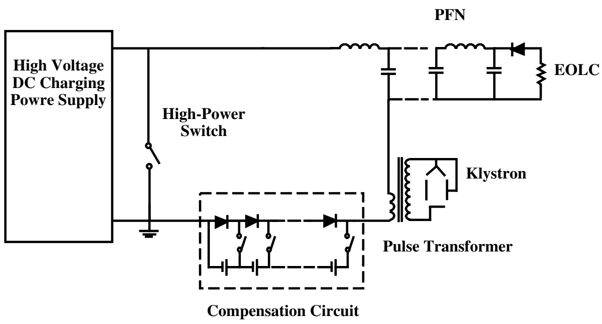

Figure 1: Basic line-type modulator with a compensation circuit.

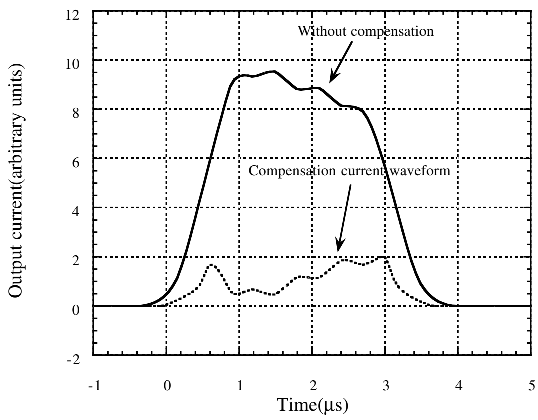

Figure 2(a): Output current and compensation current waveforms.

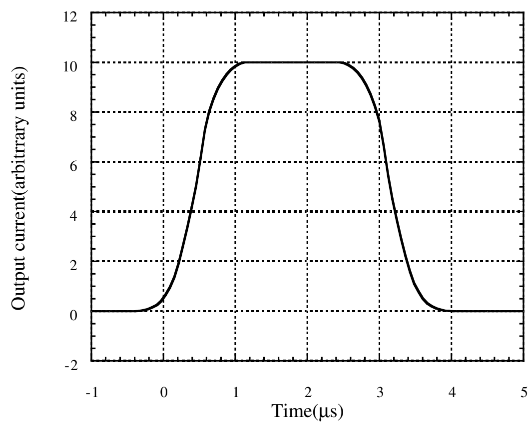

Figure 2(b): Improved output current waveform.

3 TEST CIRCUIT

3.1 Test circuit

The test modulator was designed to generate an output pulse with a peak current of 300 A and a pulse width of 2.5 μs. Figure 3 shows the circuit diagram of the test modulator. The test modulator consists of a PFN, a 15 Ω resistor as a dummy load, a solid-state switch and a compensation circuit. The PFN consists of 5 sections with fixed capacitors and tunable inductors. The capacitance and inductance of each section are 14 nF and 3 μH, respectively. The PFN is charged by an inverter DC power supply. The solid-state switch is used to discharge the PFN. It consists of 8 Insulated Gate Bipolar Transistors(IGBTs), MITSUBISHI CM300DY-28H stacked in series. The CM300DY-28H is rated at 1.4 kV peak voltage and 300 A average current. The output current was measured with a Pearson's current transformer that is installed between the compensation circuit and the IGBT switch.

3.2 Compensation circuit

The compensation circuit is connected in series to the ground side of a dummy resistor as shown in Figure 3. It is made of a DC power supply and 12 diode sections, each which consists of a balance resistor R, a diode D, a solid-state switch S and an energy storage capacitor C. The switch S is made of 8 Metal Oxide Semiconductor Field Effect Transistors(MOSFETs), MITSUBISHI FS14SM-18A connected in parallel. The FS14SM-18A has a maximum voltage rating of 900 V, an average current rating of 14 A and a pulsed current rating of 42 A. The diode D is used as a bypass-diode and consists of 4 diodes NIHON INTER KSF30As connected in parallel. The KSF30A is rated at 600 V and 30A average current. The capacitance of the energy storage capacitor C was determined to be 10 μF in order to keep its voltage drop within 20%. Each gate circuit for the MOSFET switches is connected with a control circuit through optical cables. The control circuit is used to control both the timing and width of each gate trigger pulse and to make a waveform pattern to improve the output pulse.

This circuit works as follows. The energy storage capacitor C of each section is initially charged by the DC power supply. This charging voltage corresponds to the compensation voltage. The compensation circuit is connected in series to the PFN in this system. Hence, the PFN voltage is given by subtracting the compensation voltage from the charging voltage of the inverter power supply. When all the MOSFET switches are opened, the compensation circuit is completely separated from the output circuit, and the output current flows through the diodes D. When the MOSFET switch of one of the sections is closed, the current in the diode of the section is commutated. The energy storage capacitor of the section is now connected in series with output circuit, and the charging voltage of the energy storage capacitor is added in the output circuit. By controlling the MOSFET switch for each section, a compensation waveform is generated.

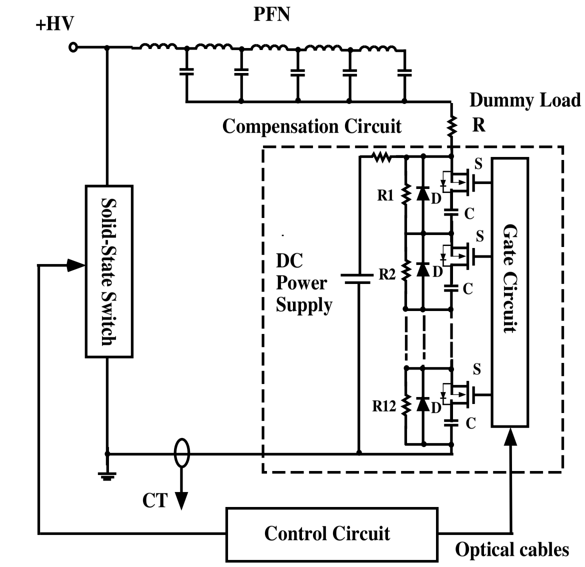

Figure 3: Simplified diagram of the test modulator with a compensation circuit.

4 RESULTS

4.1 Improvement of the output pulse waveform

Figure 4 shows an example of the output current waveforms at the dummy load, with and without compensation, at a PFN voltage of 9 kV. The compensation circuit operated at 1 kV. The trigger controls for the MOSFET switches were carefully performed to obtain both maximum flat-top width and best flatness of the pulse, while checking the output waveform. The output current waveform without compensation was rounded with no flat-top but the compensated waveform became rectangular with a wide flat-top width of 1.2 μs. The compensation current waveform is also shown in Figure 4. It shows a significant improvement with the compensation circuit.

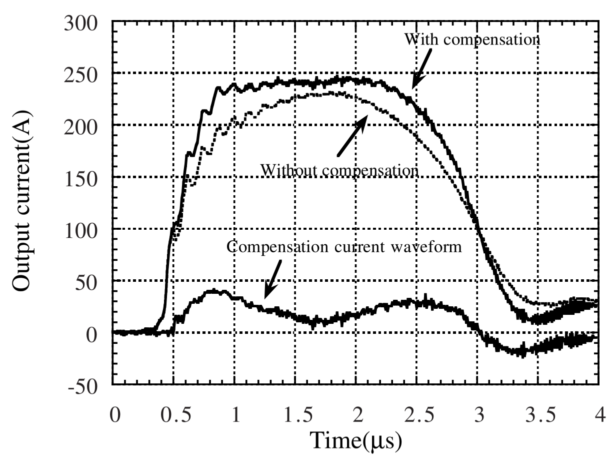

Figure 4: Output current waveforms with and without compensation, and the compensation current waveform.

In order to investigate the performance of the compensation, the flat-top width of the output pulse was measured at a compensation voltage of 0, 1, 2 and 3 kV. The modulator was charged at 9, 10, 11 and 12 kV, respectively to keep a peak value of the output current. The flat-top width is the width required for the output current to be over 98% of its maximum value. Figure 5 shows the flat-top width as a function of compensation voltage. The flat-top width is proportional to compensation voltage. Comparing the flat-top widths at 0 and 3 kV, it is found that the flat-top width is increased by factor 2.

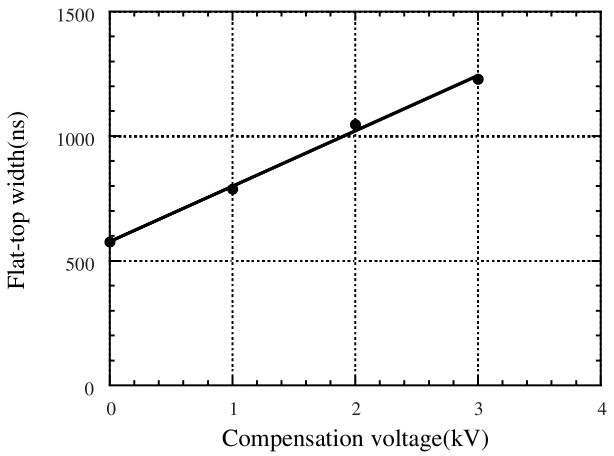

Figure 5: Improved flat-top width as a function of compensation voltage.

4.2 Improvement of the flat-top waveform

Figure 6 shows the expanded pulse top traces of the output current at the dummy load, with and without compensation, at a PFN voltage of 10 kV. The compensation circuit operated at 1 kV. The output current waveform without compensation had a 400 ns flat-top within ±0.25%, while the output waveform with compensation had a 520 ns flat-top within ±0.1%. It is found that both the flat-top width and flatness of the output current pulse can be excellently improved.

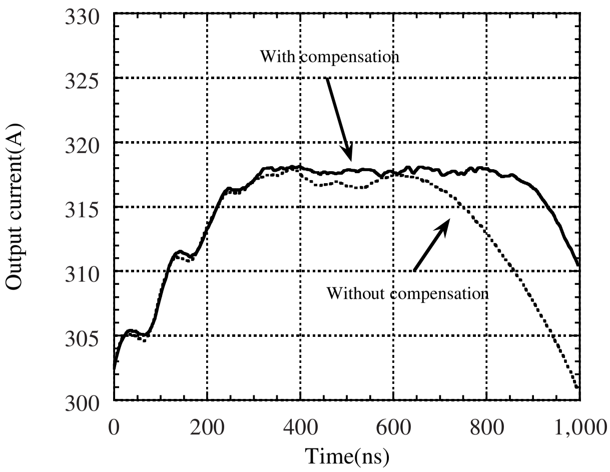

Figure 6: Expanded pulse top traces of the output current with and without compensation.

5 ALLPLICATION

This system is effective in reducing the size of the storage capacitor in a direct switching modulator, which consists of an on-off switch and a storage capacitor. The compensation circuit is connected in series to the ground side of the klystron load. In this type of modulators, the required capacitance of the storage capacitors is inversely proportional to the droop of the output waveform. For example, twice the droop can be compensated by using the compensation circuit, so that the storage capacitor sizes can be reduced by half for achieving the same droop characteristic. Therefore, the use of this system results in compact direct switching modulators.

6 CONCLUSIONS

In order to improve waveform efficiency of a klystron modulator, a system using a compensation circuit has been developed. We have designed and assembled a experimental modulator to investigate the performance of this system. From the experimental results, we found that this system enables us to produce excellent waveform with a wide flat-top and good flatness and it improves the energy efficiency.

REFERENCES

[1] JLC Design Study Group, “JLC Design Study,” KEK Report 97-1, 1997.

[2] S. Murata et al., “Development of a Sag Compensation Circuit for the Klystron Pulse Modulator,” 1996 National Convention Record I.E.E Japan, No. 772, 4-93(1996).