DEVELOPMENT OF HIGH POWER X-BAND SEMICONDUCTOR RF SWITCH FOR PULSE COMPRESSION SYSTEMS OF FUTURE LINEAR COLLIDERS

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Abstract

We describe development of semiconductor X-band high-power RF switches. The target applications are high-power RF pulse compression systems for future linear colliders. We describe the design methodology of the architecture of the whole switch systems. We present the scaling law that governs the relation between power handling capability and number of elements. We designed and built several active waveguide windows for the active element. The waveguide window is a silicon wafer with an array of four hundred PIN/NIP diodes covering the surface of the window. This waveguide window is located in an *over-moded* TE_{01} circular waveguide. The results of high power RF measurements of the active waveguide window are presented. The experiment is performed at power levels of a few megawatts at X-band.

1 INTRODUCTION

High power pulse compression systems are one of the important subsystems in the future linear colliders [1,2] to achieve high gradient acceleration in the main linac. Pulse compression systems have to have high efficiency and have to have reasonably compact size. Several schemes of pulse compression systems [3] have been developed. The active pulse compression systems, which use high power RF switches, are an alternative scheme [3]. Theoretical studies [4] and [5] have explored possibilities of active RF pulse compression systems. These studies showed that active pulse compression systems have higher efficiency and less system size than passive systems.

In this presentation, we describe the theory for designing high power RF switches, and show experimental results of PIN/NIP diode array active window, which is the key element of the active RF switches.

2 SYNTHESIS OF RF SWITCHES

The SPDT (Single Pole Double Throw) switches described here have two designs. Both designs consist of two 3dB hybrids and active modules. In the first design, the active module is array of SPST (Single Pole Single Throw) switches. In the second design, the module is composed of cascaded phase shifters (see Figure 1).

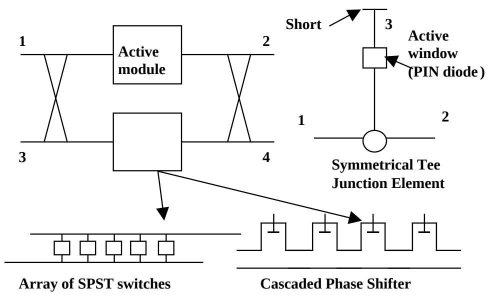

Figure 1: Synthesis of high power RF switches

Each cascaded element of the phase shifter and SPST switch have similar design. The active element consists of a symmetrical three-port tee-junction and an active waveguide window (PIN/NIP diode array window) placed in the third arm of the symmetrical tee-junction. The S-matrix of the elements is given by [6]

$$S = \begin{pmatrix} \cos\frac{\zeta-\phi}{2} e^{j\left(\frac{\zeta+\phi}{2}+\alpha\right)} & j\sin\frac{\zeta-\phi}{2} e^{j\left(\frac{\zeta+\phi}{2}+\alpha\right)} \\ j\sin\frac{\zeta-\phi}{2} e^{j\left(\frac{\zeta+\phi}{2}+\alpha\right)} & \cos\frac{\zeta-\phi}{2} e^{j\left(\frac{\zeta+\phi}{2}+\alpha\right)} \end{pmatrix}$$

where θ, φ, and α are parameters which characterizes the tee junction and ζ is the parameter which changes as a function of the change of status of the active windows.

2.1 SPST arrays

For SPST switches, $\zeta = \phi$ and $\zeta = \phi + \pi$ is the perfect-reflector and match conditions, respectively. With this configuration, input is port 1 and output is port 3 and 4 (in Figure 1) for reverse and forward bias, respectively.

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Normalized voltage at the active window is given by (with similar procedure to that presented in [6])

$$V = \frac{2}{\sqrt{n}} \sqrt{\frac{1 - 2\cos\theta\cos\phi + \cos^2\theta}{2\sin^2\theta}} \left|\sin\frac{\Psi_1 - \Psi_2}{2}\right|,$$

where θ is a parameter which characterizes the tee junction, $\Psi_1 - \Psi_2$ is reflection phase difference in the third arm between forward and reverse bias status, and n is the number of the tee junction elements.

2.2 Cascaded phase shifters

In case of the cascaded phase shifter, the tee junction is designed [6] so that total phase shift of the whole cascade structure is $\pi/2$ when each element is matched by itself ($\zeta = \phi + \pi$). When the PIN/NIP diode is forward biased, each element is not matched by itself but the whole cascaded structure is matched, and the total phase shift is 0 and π for upper and lower structure respectively. ζ is chosen for forward biased status as [3]

$$\zeta_1 = \phi - 2\arctan\left(\frac{\sin\frac{\pi}{n}}{\cos\frac{M\pi}{n} - \cos\frac{\pi}{n}}\right),$$

$M = 4m + 4$, (total phase shift 0)

$M = 4m + 2$, (total phase shift π)

where m is integer and n is number of cascaded elements. With this configuration, input is port 1 and output is port 2 and 4 (in Fig. 1) for reverse and forward bias, respectively. Normalized voltage at the active window is given by [6]

$$V = \sqrt{\frac{1 - 2\cos\theta\cos\phi + \cos^2\theta}{2\sin^2\theta}} \left|\sin\frac{\Psi_1 - \Psi_2}{2}\right|,$$

where θ is parameter which characterizes the tee junction, and $\Psi_1 - \Psi_2$ is the reflection phase difference in the third arm between forward and reverse bias status. With large number of elements, $\Psi_1 - \Psi_2$ become smaller, because the phase shift of each element is small. Then the maximum voltage V is reduced.

3 SCALING LAW

We derive the normalized maximum field at active RF window in the third arm with some approximations**.** It is given by

$$E_{\max} = C\sqrt{\frac{R_s}{nL_0}}\sqrt{\frac{1}{AG}},$$

where C is a constant, π for cascaded phase shifter, and 2 for SPST switch array. This means that the case of the SPST array is better than that of the cascaded phase shifter. In the above Equation, R_s is the surface resistivity, L_0 is the allowable loss, n is the total number of active elements, A is the cross sectional area of the waveguide, and G is a geometrical factor that dependes on the mode and the shape of the waveguide. This scaling law is quite general; it can be used for not only PIN/NIP diode switches but also for laser-driven switches [4] or other kind of active switches.

Examples

We assume the maximum field limit on the silicon window to be 10MV/m. Also, we assume that the acceptable loss $L_0 \cong 2\%$. With forward bias, the surface resistivity obtained by a maximum carrier density of 10^{17} cm^{-3} is R_s = 4.9 ohm. Input power is assumed to be 100MW.

With TE_{10} mode active windows in WR90 rectangular waveguides, 24 and 58 elements are needed for SPST array and cascaded phase shifter, respectively. Also, with TE_{01} mode active windows in 1.3 inch diameter circular waveguides, 21 and 51 elements are needed for SPST array and cascaded phase shifter, respectively.

Figure 2: PIN/NIP diode array window and supporting RF structure

4 DESIGN AND IMPLEMENTASION OF PIN/NIP DIODE ARRAY WINDOW

The picture of the PIN/NIP diode array active window is shown in Figure 2. The base material is high purity silicon. All doping profile and metallic terminals are radial, i.e. perpendicular to electric field of the TE_{01} mode. Hence, the effect of doping and metal lines on the RF signal is very small, when the diode is reverse biased. P and N type impurities (boron and phosphorus) are doped on front side and backside, respectively. Because all surface currents of the TE_{01} mode are in the azimuthal direction, a gap for the DC bias voltage is easily designed in RF structure supporting the window. Thus, we avoid the RF chokes needed when using other types of waveguide modes such as the TE_{10} mode in rectangular waveguides [8, 9].

In this design, the diameter of active region is 1.299 inch, and window thickness is 220μm. Doping and metalization lines are tapered in width from 25μm to 3μm. The number of lines is 400. The coverage factor (the ratio between the are of the diodes to the area of the window) is 10%, and the reflection caused by the diode lines when the diode is reverse or zero biased is small.

For testing the window, the TE_{01} mode is excited using a compact high-power TE_{10} (rectangular) to TE_{01} (circular) mode converter [5].

The process of building the PIN/NIP diode array window is based on common IC processing.

5 LOW POWER MEASUREMENT

In the low power measurement, waveforms of reflected and transmitted signal from the active window are measured by peak power meter. Current through the active window is measured by current transformer.

We summarize low power measurement results here.

- Total reflection is 2.41 dB and 0.6 dB, and total transmission is 4.16 dB and 22 dB, with reverse and forward bias, respectively.
- Loss dissipated into the active window is 3% and 11.5% with reverse and forward bias, respectively. Loss of TE_{01} mode converters and the support structure is 1.3%.
- Resultant carrier density in I region is $7\times10^{14}\,cm^{-3}$ under forward bias, assuming uniform carrier distribution.
- Switching speed of forward to reverse bias is 2μsec. Natural recovery time is more than 10μsec. Switching speed is so far limited by external circuit of reverse bias.

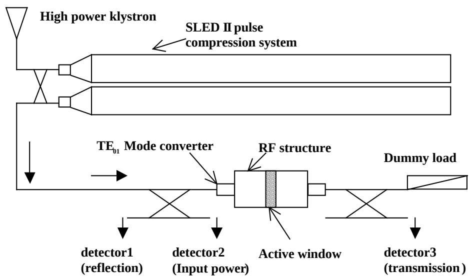

Figure 3: Schematic diagram of high power experiment

6 HIGH POWER EXPERIMENT

The schematic diagram of high power experiment is shown in Figure 3. With this setup, up to 15MW of power with 150 nsec pulsewidth at 11.424GHz is feed to the active window. The purpose of this experiment is following:

first, to investigate failure mode of the active window with increasing peak electric field, second, to demonstrate switching capabilities at the power levels of megawatt order.

Avalanche breakdown in the silicon did not occur at 12MW input power (with 3MW of transmitted power). However, arcing between aluminium lines on the diode structure occurred at about 5MW input power. Once arc occurred, the threshold of arcing went down because the surfaces of the aluminium lines were damaged by arcing. This arcing limited the high power operation.

With forward bias, reflected power is 1.7MW and transmitted power is 61kW at the 1.84MW of input power. Transmission modulation is 10dB.

7 DISCUSSIONS

We emphasize that high-purity silicon window can handle high power at the level of multi-megawatt. So far, arcing between aluminium lines limited high power operation. One possibility to prevent this arcing is to embed the aluminium lines inside a layer of Silicon. We also are investigating biasing circuit to improve switching speed.

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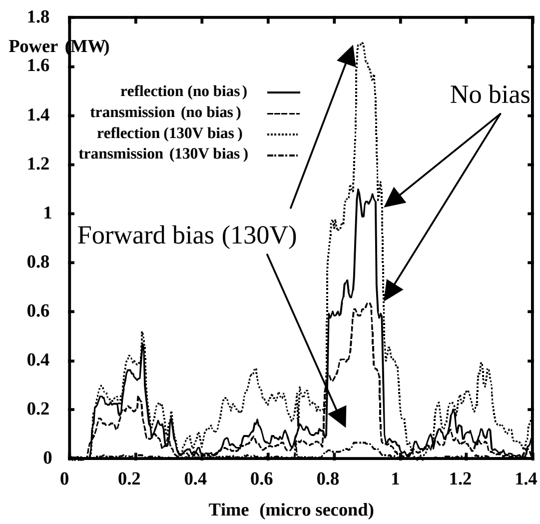

Figure 4: Waveform with zero and forward bias