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BaBar SVT Electronic Readout System Design Requirements

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Abstract

The essential and functional requirements for the electronic readout system for the *BaBar* silicon vertex tracker (SVT) are described.

Contents

I Introduction

This document describes the requirements for the *BaBar* Silicon Vertex Tracker (SVT) electronic readout system. The document begins with a general introduction to the SVT, its primary physics goals, the SVT geometry, the electrical parameters of the silicon detectors and the expected physics and background rates at PEP-II. Next we present a detailed list of requirements. An overview of the components of the electronic readout system and a detailed description of each is given in a companion document, "*BaBar* SVT Electronic Readout System Description." For a more detailed description of the SVT detector and the *BaBar* physics program the reader is referred to the *BaBar* Technical Design Report[1].

The requirements for the SVT readout IC were reviewed in June, 1995 and are described in a separate document[2]. The readout IC requirements are not intended to be included as part of the present requirements review, but are included in the documentation for completeness.

I-A The SVT and its Physics Goals

The major motivation for building *BaBar* is to find and precisely measure *CP* violation in the decays of neutral B mesons. To this end, the time interval between the two B-meson decays must be measured for each event by reconstructing the two primary decay vertices to an accuracy which is better than one-half of their average separation, which is 250 μm along the boost ($+z$) direction at PEP-II ($\beta\gamma = 0.56$). This translates into a resolution of 80 μm in z on an individual B^0 vertex. Measurement of primary and secondary vertices in B decays is the primary task of the vertex detector. The vertex detector also dominates in the determination of track angles. In addition, the vertex detector provides complete stand-alone tracking; this is particularly important for the reconstruction of the many particles with low transverse momenta ($p_t < 100\,\mathrm{MeV}/c$) which cannot be reconstructed in the drift chamber. Due to this capability, the *BaBar* vertex detector is known as the silicon vertex tracker (SVT).

The measurement of CP asymmetries in B^0 decays depends upon the reconstruction of final states with very small branching fractions, and consequently it is very important to maximize acceptance and efficiency. The largest possible solid angle must be instrumented, especially in the forward region where track density is highest due to the forward boost. In addition, the single point efficiency must be very high for tracks at all angles and momenta from B^0 decay. Finally, detector reliability must be very good and redundancy should be built in wherever possible in order to minimize downtime and maximize the total integrated data sample.

The physics requirements of *BaBar* have driven the requirements for the electronic readout system of the SVT, and this is reflected in the conceptual design of the SVT electronic readout. Analog readout was selected in order to get the best point resolution, by exploiting charge sharing between silicon strips. This improves the impact parameter resolution, which is dominated by the precision of the first measurement. The electronics for the SVT will be mounted outside of the active tracking volume in a very narrow region just above the machine stay-clear. This design minimizes multiple scattering for the low momentum particles produced in B decays, and maximizes the acceptance especially in the forward (boost) direction. Access to the SVT for maintenance and repairs will be very limited and will require a major shut-down to remove the support tube which contains the final machine elements as well as the SVT. Consequently, the readout must be very reliable and provide redundancy for common failure modes.

I-B SVT Detector Geometry

The SVT has five layers of double-sided silicon microstrip detectors, with the strips oriented orthogonally to provide 5 measurements each in the z and ϕ. The coverage of the SVT extends to within 350 (500) mrad of the beamline in the forward (backward) direction. Each of the three inner layers has six detector modules, arrayed azimuthally around the beam pipe, while layers 4 and 5 consist of 16 and 18 detector modules, respectively.

The inner 3 layers of detector modules are traditional barrel-style structures, while the outer detector modules employ a novel arch structure in which the detectors are electrically connected across an angle. The bends in the arch modules minimize the area of silicon required to cover the solid angle and also avoid very large track incident angles. Layers 4 and 5 are further divided into “a” and “b” modules, where layers 4a and 5a are situated at slightly smaller radii than layers 4b and 5b, respectively. The azimuthal overlap between the “a” and “b” type modules ensures full efficiency. In the inner three layers a pin-wheel type arrangement is used to provide overlap.

A side view of the detector is shown in Figure 1, and an end view is shown in Figure 2. The parameters of the SVT detector are summarized below in Table 1. The intrinsic resolution is calculated at 90° track incidence assuming $S/N = 20 : 1$. The z-ganging numbers represent the percentage of detector strips connected to one other strip.

The detector modules are mechanically stiffened with a pair of kevlar/carbon-fiber composite ribs which run lengthwise along the module and connect at each end of the module to a high density interconnect, or HDI. The HDI is a ceramic circuit which supports the readout IC’s. Flexible fanout circuits which are wirebonded to the silicon detectors bring the signals from the silicon strips to the inputs of the readout IC’s, which are mounted on both sides of the HDIs. The HDIs are mounted on cooling rings located at the forward and backward ends, outside the active tracking region. The cooling rings in turn are supported from carbon fiber cones which are kinematically mounted on the B1 magnets. All of the electronic readout and support for the SVT must fit into the region below approximately 350 mrad, where the active tracking volume starts, and the machine stay clear which is located at approximately 300 mrad.

In all five layers of the SVT the detector modules are oriented with the z-strips closest to the beampipe, and the support ribs on the top side (away from the IP). Detector modules in layers 1 and 2 are glued together to form “sextants”; this is the only case where the ribs are glued to the z-side fanout, which extends the full length of the detector module. For layers 1-3, the p-side of the detectors is used for the z-strips (positive polarity signals), while in layers 4-5 the n-side is used for the z-strips (negative polarity signals).

In layers 4 and 5, two z-strips may be connected to a single readout channel. This is necessary due to lack of space to mount additional readout IC’s. This results in a ganging ambiguity which must be handled in the event reconstruction, and it also increases the capacitive load seen by the front-end preampflier. The ϕ-strips are daisy-chained between detectors, resulting in total strip lengths of up to 26 cm and a maximum capacitance of 35 pF.

The design has a total of 340 silicon detectors of six different types. The total silicon area in the SVT is about $1\,\mathrm{m}^2$, and the number of readout channels is $\sim$150,000.

I-C Silicon Detectors

The SVT is based on double-sided silicon microstrip detectors which are AC-coupled and biased with polysilicon resistors. The wafers will be n-type, 300 μm thick, with resistivity in the range 4-8

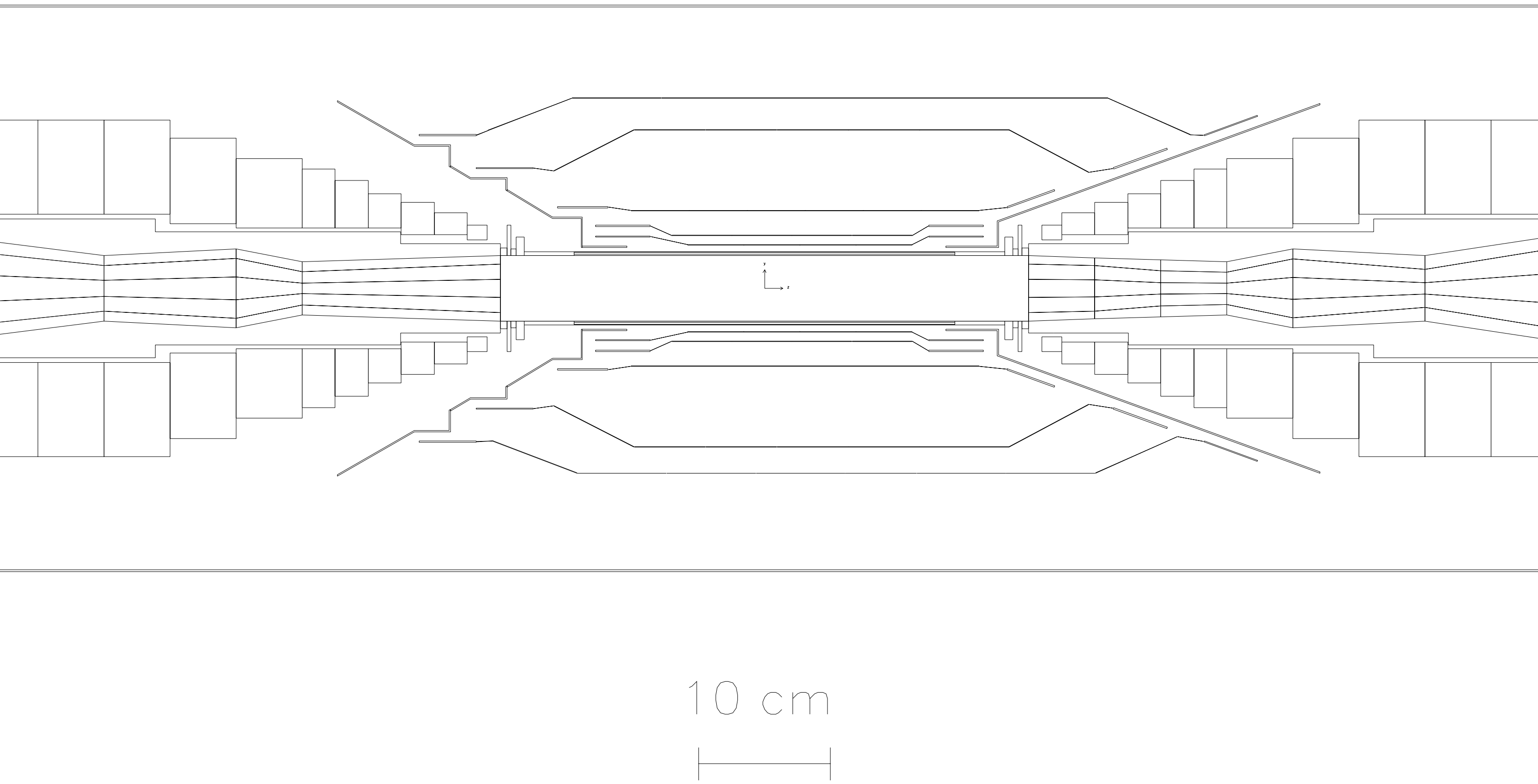

Figure 1: Cross-sectional view of the SVT in a plane containing the beam axis. The beampipe, B1 magnets, and SVT support structure is also shown.

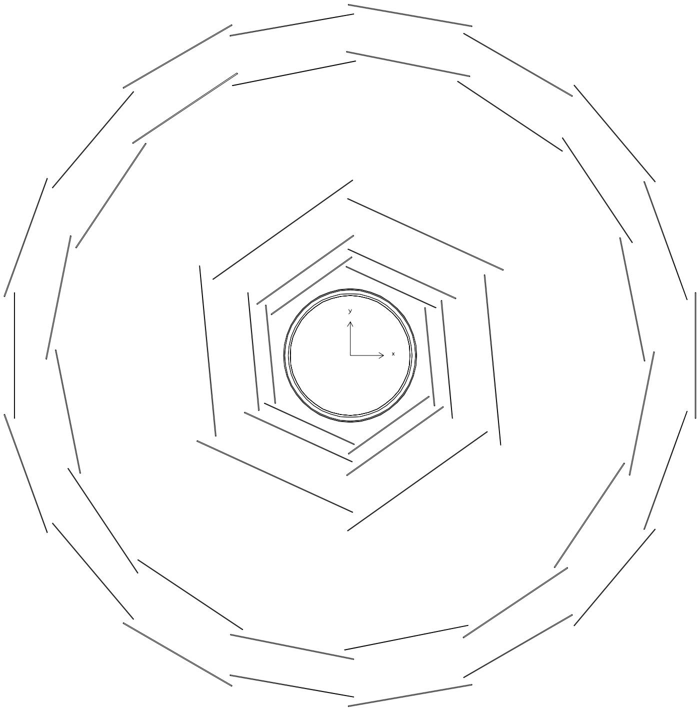

Figure 2: Cross-sectional view of the SVT in a plane perpendicular to the beam axis.

Quantity	Layer 1	Layer 2	Layer 3	Layer 4a	Layer 4b	Layer 5a	Layer 5b
Radius (mm)	32	40	54	124	127	140	144
Wafers/Module	4	4	6	7	7	8	8
Modules/Layer	6	6	6	8	8	9	9
R.O. Section/Module	4	4	4	4		4	
ICs/R.O. Section	7	7	10	5		5	
Strip Length, f/b (mm):							
ϕ	82	88	127	230/189	230/203	270/257	270/270
z	40	48	70	42–51	42–51	42–51	42–51
z Ganging (f/b):				34%/67%	48%/67%	88%/98%	98%/98%
Readout pitch (μm):							
ϕ	50	55	55	80–100		80–100	
z	100	100	100	210		210	
Floating Strips:							
ϕ	—	—	—	1		1	
z	1	1	1	1		1	
Intrinsic Resolution(μm):							
ϕ	10	10	10	10–12		10–12	
z	12	12	12	25		25	

Table 1: Parameters of the SVT detector layout.

Det. Type	I	II	III	IV	V	VI
Dimensions (mm)						
z	42.40	45.40	43.90	67.55	53.9	67.97
ϕ	41.30	49.415	71.47	52.50	52.50	$52.80 \rightarrow 43.30$
Junction on	z	z	z	ϕ	ϕ	ϕ
$z-$side						
C_{int} (pF/cm)	1.3	1.3	1.3	1.5	1.5	1.5
C_{AC} (pF/cm)	40	40	40	80	80	80
R_{series} (Ω/cm)	7	7	7	3.5	3.5	3.5
$\phi-$side						
C_{int} (pF/cm)	2.8	2.8	2.8	1.3	1.3	1.3
C_{AC} (pF/cm)	40	40	40	40	40	37
R_{series} (Ω/cm)	7	7	7	7	7	7.5

Table 2: Electrical parameters for the different detector types.

kΩ cm. On the junction side p^+ strips are employed and on the ohmic side n^+ strips are employed with p^+ blocking strips in between. Floating strips are foreseen in between the readout strips in some layers, in order to increase capactivie charge sharing and improve position resolution.

The AC coupling capacitance will range from 40-80 pF/cm, depending on the implant width, and are specified to withstand up to 60 V. The polysilicon resistors are specified to be 8 MΩ. The detectors will fully deplete at a bias voltage of between 15 and 55 V. The bias voltage will be applied symmetrically to the detectors, so that only half of the total depletion voltage is applied to each side relative to earth ground. The readout electronics will float at the detector bias voltage in order to avoid placing a large voltage across the AC coupling capacitors. The implications of this choice for common-mode noise need to be studied in detail and carefully evaluated with prototype electronics and detectors.

The parameters of the six detector models are given in Table 2, including the interstrip capacitance, AC-coupling capacitance, and series resistance.

I-D PEP-II Data-Taking Environment

The environment of the high-luminosity PEP-II machine poses certain unique challenges. PEP-II beam crossings occur at a rate of 238 MHz, which, in terms of the response time of the electronics, is essentially continuous, unlike at previous e^+e^- colliders. This necessitates an asynchronous data acquisition system and front-end electronics which are continuously sensitive. PEP-II may have severe backgrounds, producing high occupancies. These high occupancies present a significant burden on the storage, transport and recording of data. As described in the *Technical Design Report* (TDR) [1], Chapter 12, the backgrounds expected in PEP-II include particles lost near the IP, beam-gas interactions, and cosmic rays. The dominant source of occupancy in the SVT is predicted to be the lost particle background, which depends on beam intensity and the quality of the vacuum in the machine in the region from 3 to 50 m from the IP. The SVT electronic readout system should perform well at up to ten times the expected nominal backgrounds, and its performance should degrade gracefully at higher levels.

Stave	Layer 1 z	Layer 1 ϕ	Layer 2 z	Layer 2 ϕ
1	3.1%	1.4%	2.1%	1.3%
2	1.1%	0.6%	0.8%	0.5%
3	0.4%	0.3%	0.2%	0.3%
4	1.3%	0.6%	0.8%	0.5%
5	0.6%	0.4%	0.4%	0.3%
6	1.1%	0.6%	0.7%	0.5%

Table 3: Occupancy per μs in layers 1 and 2 at nominal background.

The percent occupancy in a 1 μs window versus stave number for layers 1 and 2 in the SVT at nominal background is shown in Table 3 [5]. The distribution is peaked in the bend plane of the machine, with significantly higher occupancy in staves 1 and 4 which are located at at $\phi = 0$ and π.

The background occupancy is fairly high, and this has some important consequences for the readout architecture. One notable consequence is that a data-push readout is not feasible due to the large data transmission bandwidth that would be required; this in turn implies a fast Level 1 trigger to enable the vertex detector readout [6]. The Level 1 trigger will latency of no more than 12 μs and an uncertainty of no more than 1 μs, and a maximum rate of 10 kHz.

Radiation damage from the lost-particle flux is also a concern for the SVT. Layer 1 sees an average of about 33 krad per year (10^7 s), layer 2 sees 19 krad/yr and layer 3 sees about 6 krad/yr [5]. The dose is not uniformly distributed, but exhibits sharp peaks in the bend planes of the machine. This results in a highly nonuniform dose per stave in the inner layers. The worst case is in layer 1, stave 1, where the average yearly dose is 82 krad/yr, and the peak dose is 240 krad/yr over a region covering approximately 6° in azimuth. The increased leakage current due to radiation damage will contribute to the electronics noise. In addition, the readout IC's, which are located near the detectors themselves, must withstand significant ionizing radiation without degradation in performance.

II Requirements

The requirements are divided into two major categories: (A) essential requirements derived from physics goals and from practical considerations of the PEP-II/*BaBar* environment. (B) functional requirements derived from the essential requirements and from good engineering practice. The second category is further broken down by sub-component.

II-A Essential Requirements for the SVT Electronic Readout System

1. **Asynchronous Operation**

   Due to the close bunch spacing in the storage rings (4.2nsec), the SVT electronics must acquire, process, and transmit data simultaneously.

2. **Triggered Readout**

   Due to the expected high occupancy rates from lost-particle backgrounds, the SVT has adopted a triggered readout system. The SVT readout system must store data for the duration of the L1 trigger latency of 12 μs and be able to retrieve data within the L1 trigger jitter window of 1 μs.

3. **Background Safety Factor**

   The SVT readout must withstand up to 10 times the nominal background rate, and degrade gracefully at higher levels. It must withstand an integrated radiation dose equivalent to 10 years at nominal background rates.

4. **Dead time**

   The data transmission must be able to handle a maximum L1 trigger rate of 10 kHz at 10 times nominal background with less than 10% deadtime.

5. **Error Rate**

   The bit error rate should be good enough that the fraction of transmitted events with a bit error is less than 1 in 10^7.

6. **Acceptance**

   The coverage of the SVT is nominally 350 mrad with respect to the beam line in the forward direction and nominally 520 mrad in the backward direction. The electronic readout system should not extend beyond these boundaries.

7. **Single Hit Efficiency**

   The efficiency for the electronic readout system to record a single hit above a nominal threshold of 1 fC on a good strip should exceed 98%. This includes the effects of bad readout channels, bad connections (other than bad wirebonds) and noise fluctuations.

8. **Signal to noise**

   The ratio of the most probable signal on a single strip, assuming a track that passes mid-way between two strips, to the worst case noise, including the effects of 10 years of radiation at nominal background, should never fall below 4.0 for any of the strip configurations at any incident track angle.

9. **Time stamp**

   A Hit Time Stamp with a binning resolution of 100 nsec or less is required in the inner two detector layers for correlation to calorimeter hits and drift chamber hits. Finer resolution would be helpful for off-line pattern recognition. For layer 3, 200 nsec is acceptable and for layers 4 and 5, 400 nsec binning resolution is acceptable.

10. **Reliability**

    The electronic readout must be very robust and have redundancy built in for critical data and control lines. The SVT must also have a monitoring and interlock system to safeguard against catastrophic failure which cannot be manually overridden.

11. **Power dissipation**

    The maximum power dissipated by the Front-end Electronics must be less then 250 W per detector end. An additional 100 W may be dissipated by passive or active components at the Matching Cards on each end.

12. **RF Shielding**

    The Front-end Electronics must tolerate or be shielded from RF noise generated by the accelerator.

II-B Derived Functional Requirements

These requirements follow from the essential requirements, taking existing constraints into account and following good engineering practices.

II-B-1 Readout IC

The requirements for the readout IC were finalized and reviewed much earlier than the rest of the SVT readout system due to the need to begin engineering immediately on this long lead-time component. See Appendix A for *BaBar* Note # 213, "Requirements Specifications for Silicon Vertex Detector Readout Chip."

II-B-2 Hybrid

Introduction

The SVT hybrid consists of two separately manufactured items along with the readout IC's and discrete components. One is the high density interconnect (HDI) and the other is the tail.

The HDI's function is to provide the physical support, cooling and electrical interconnections for the readut IC's, and the connections to other components. The silicon detectors are mounted via the support ribs to the HDIs, which in turn are mounted to the support/cooling cones. The positioning tolerance of the detectors determines the dimensional tolerances of the HDIs. Also, the size of the HDIs is extremely constrained by the small gap between the B1 magnet stay clear at 300 mrad and the active tracking volume at 350 mrad. The need to run electrical connections for the inner layers out under the HDIs of the outer layers imposes additional mechanical constraints. The electrical requirements are also stringent in order to minimize crosstalk and noise, especially on the analog power and ground planes.

The tail provides the electrical connection between the HDI and the matching card. It must be a flexible multi-layer circuit which carries both power and signals with minimum coupling between the digital and analog sections. The DC resistance and impedance must be minimized while conforming to stringent constraints on its thickness and width.

Mechanical Requirements for the HDI

1. Dimensions: The HDI's are constrained to fit in a very narrow region below the tracking acceptance and above the machine stay-clear; this space is only about 1 cm wide. To accomodate this requirement, there will be three different HDI layouts, as summarized in Table 4.

	Type I	Type II	Type III
Width (mm)	46.80	66.30	33.80
Length (mm)	41.20	38.00	43.51
Thickness(mm)	1.2	1.2	1.2
Quantity	24	12	68

Table 4: Dimensions and quantities of the HDI layouts.

All of the circuits are double-sided in order to read out both the ϕ and the z strips of one half detector module. The quantity listed does not include spares.

Type I, which is used for layers 1 and 2, will have 7 chips per side. Type II, used for layer 3, has 10 chips per side, and Type III which is used for layers 4 and 5, will have 5 chips per side.

2. Accuracy in IC positioning: ± 25 μm.
3. Planarity tolerance in the stay-clear regions for the contact with support feet: 10 μm
4. Accuracy of the cuts of holes for feet and vias $\pm$ 50 μm
5. Accuracy in the cut of substrate: $\pm$ 100 μm.
6. Stay-clear region on front of HDI for gluing the fanout, minimum length: 4.5 mm.
7. Stay-clear regions on the four corners of the HDI for mechanical tools accessing: at least 2.5 x 0.5 mm^2.
8. Connectors to the tail: Berg connectors glued or soldered on the HDI.
9. Total thickness, including external mounted components: no more than 7.4 mm.

Thermal Requirements for the HDI

The power dissipated on the HDI will be in the range 3.8 - 7.6 W, while the maximum operating temperature of the chip is 40° C. For this reason the HDI substrate must have high thermal conductivity and a good thermal contact with the cooling system.

FEA calculations and laboratory measurements have been carried out, with consistent results. They show that an AlN substrate with a thickness of 1.2 mm provides sufficient thermal conductivity to meet the requirement on the chip operating temperature.

Electrical Requirements for the HDI

As a general principle, the electrical layout of the HDI must minimize the coupling between the digital and the analog sections. All digital signals have to run as a complementary pair of traces which will carry differential signals. Power supply on the HDI must be distributed so to minimize inductance of the traces and to match in a very good way with the current return.

The HDI must provide the following electrical connections:

1. Power and ground: Three different power supplies are required, +5V (AVDD) and +2 V (AVDD2) analog, +5 V (DVDD) digital.

   There are two different returns, one for digital current (DGND) and one for analog current (AGND).

   Each power line must be filtered locally with capacitors to the common return (AVDD and AVDD2 to AGND, DVDD to DGND).

2. Clock and command: Two redundant sets of differential clock and command lines must be bussed to all the chips and terminated so as to mach with the characteristic impedance of the tail.

3. Data: Redundant differential data lines on the HDI must be connected to the first and to the last chips on each side.

4. Detector bias voltage: The detector bias voltage (VDET) must be capacitively coupled to the AVDD2 line, which is the analog reference voltage of the readout IC front-end.

5. ϕ and z side coupling: The HDI must provide for capacitive coupling between the two (ϕ and z) readout sections.

6. Temperature monitors: Each HDI must host and provide connections to one resistive temperature monitor.

7. Remote Voltage sensing: Each HDI must provide connections for remote sensing lines for all three of the IC voltages.

Mechanical Requirements for the Tail

1. Maximum allowed dimensions: length 50 cm, width 5.25 mm, thickness 0.5 mm.
2. Material: Flexible cable with resilient structure and partial torsional elasticity.
3. Minimum width of signal traces: 125 μm.
4. Connectors: Both ends shaped to fit into a 30-contact Berg connector.

Electrical Requirements for the Tail

1. Five conductive layers for power and ground planes and one signal plane.
2. Controlled characteristic impedance of 35 - 45 ohms, to be matched to drivers and receivers at both ends of the tail.
3. Separation of digital and analog signal to minimize cross talk and noise.
4. Each signal directly coupled to its own current return.

II-B-3 Data Transmission Requirements

Data Rate

The data transmission must be capable of handling at least 100 Mbits/sec/readout section. This number depends upon background rates and integration times. Using the occupancy rates given in section I-D, the highest hit rate in a single readout section at nominal background is 12.4 hits/μs (layer 1,stave 1, z side). Then assuming the nominal trigger jitter window of 1 μs, an average of 20 bits of data per hit (including header and trailer records), and a worst case level 1 trigger rate of 10 kHz, the average data rate is 2.5 Mbits/sec data per readout section. To cope with fluctuations in the average rate, we take a safety factor of four. Requiring that the system perform up to ten times the nominal background then requires a data rate of 100 MBits/sec/readout section.

Power Consumption

The power consumption of the data transmission system for components located inside the support tube must not exceed 500 mW/readout section This is not an absolute limit. We currently do not have a limit on how much heat can be removed from the electronics area, but a reasonable goal should be to keep the data transmission power consumption to a fraction of that for the front-end electronics. Since no active compoents are planned for the data transmission inside the support tube, this requirement should not pose a problem.

Reliability

We have not established a quantitative value for this. The life expectancy of the detector is 10 years and the on-detector part of the data transmission system can only be accessed by a long shut down which may occur no more than once every two years. It is important that only a small fraction of the detector area die during such a two year period or else data quality will suffer.

Physical Size

There are size limitations at B1 magnet and along the entire length of the support tube. There is a small amount of space for a PCB in a region near the back of the B1 magnet. A transition card now called the "Matching Card" may be place here for each HDI. Roughly 14 cm^2 is available for such a PCB.

Inside the support tube, space is again at a premium so as not to enlarge the support tube and infringe on the other detector sub-systems that surround it. Present agreement with the IR group has allocated a cross- sectional area of 1.75 cm^2 per HDI for both power and data transmission cables, for a total of 91 cm^2 on each side.

Outside the support tube, there is more space for cabling but it will still be limited until the cables reach the region outside the full detector. There is not yet a specific limit for this cabling size but it should be kept to a minimum.

Radiation Hardness

The data transmission components should remain operational up to 100 krad total dose. This is just a guess at this time. A real estimate is required from the IR group but is not yet available.

Low Noise Generation

This requirement has two parts. The first is to minimize coupling between the digital supplies and signals and the analog supplies along the length of the transmission run. The second part is to minimize noise injection into the vertex detector front-end electronics. This latter concern is somewhat mitigated by the choice to move the transmission system several centimeters away from the silicon sensors and the front-end electronics, but it should not be overlooked. It is especially true that the interface between the front-end ICs and the data transmission system must be designed with care to avoid those signals coupling into the pre-amps.

Error Rate

The bit error rate should be less than 10^{-11}/bit. To estimate how severe this error rate is we can estimate the quantity of data transmitted from backgrounds since that makes up the bulk of the hits. Assuming an integration time of 1 μs, 20 bits of data per hit to transmit and a 10 kHz trigger rate, the average number of bits transmitted per trigger is $2.4\text{x}10^4$ for the whole vertex detector. An error rate of 10^{-11} would then imply one bit error in every $4\text{x}10^6$ events transmitted. Slightly worse error rates are probably tolerable but this seems like a good goal which would allow avoidance of complicated error correction techniques.

Safety

The cables used in the SVT data transmission must meet the SLAC standards for non-flammability.

II-B-4 Power Supplies

Introduction

The power supply system of the Silicon Vertex Tracker must meet severe requirements of accuracy, stability, and insensitivity to disturbances on the utility lines. It must be an intrinsically low-noise power supply system, in order to alleviate the filtering functions between the power supply output and the circuit to be powered. All these requirements are related to the need of keeping any noise injection from external sources into the SVT front- end chip as small as possible.

The specifications about tolerances on the voltage values and ripple slewing rate refer to the voltages as measured at the input of the front-end chips. The particular structure of the power supply system where these voltages are controlled by servoloops that sense the voltages at the chip inputs would make specifications related to the output of the power supply modules meaningless.

In the context of this document the values of the currents relevant to the FE chips are intended per power supply module, this being the unit which powers one HDI hybrid, holding up to a maximum of 20 FE chips. Meanwhile, the currents relevant to the detector section are intended per detector half-module.

Power Supply Mains

The main power supply will provide 120 V, 60 Hz AC at 20 amps.

Main Power will be provided from the BaBar detector power distribution system, with the SVT system ground tied to Earth at the SVT Power Supplies racks. A rack containing the MUX boards which optically communicate with the DAQ system, reside 30 meters from the power supplies, just outside the detector. All power, shields, and Earth Ground for the Mux racks and Front-end Electronics, is provided from the Power Supplies.

Power Supply Transformer Isolation

Electrostatic shielding between primary and secondary windings is foreseen to minimize noise injection from external sources. Use of 60Hz stabilizer is being considered at the Power Supplies.

Voltage and Current Specifications

The voltage and current specifications for each floating power supply module are given in Table 5. Each power supply module services one HDI.

Power Supply Earth and Shield Connection Options

	Tolerance	Current (mA)	Max. Ripple peak-to-peak and slew rate
Analog			
+5V	+/-5%	400	5 mV, 500 mV/s
+2V	+/-5%	640	2 mV, 100 mV/s
0V		-1040	-
Digital			
+5V	+/-5%	300	–
0V		-300	–

Table 5: Voltage and current specifications for each HDI power supply module.

Max. Voltage	Tolerance	Currents	Max. Ripple peak-to-peak and slew rate
Detector Bias			
+40V	+/-5%	1 mA	1 mV, 100 mV/s
0V		-1 mA	
-40V	+/-5%	-1 mA	1 mV, 100 mV/s
0V		1 mA	
Edge Guard Offset			
0 – 10V		-1 mA	1 mV, 100 mV/s
0V		1 mA	
Input Offset Bias			
-3V – 3V		+/- 10 μA	1 mV, 100 mV/s

Table 6: Specifications for the detector bias voltage supplies.

Each voltage source must be able to float, with options to tie the sources together and to tie either the center tap, or either side of teh silicon bias supply to earth ground. Options must be provided to connect the electrostatic shield to the center or to either side of the silicon bias supply, or directly to earth ground.

Readout IC Voltage Control

The setting of the two analog supply voltages and of the digital supply voltage is computer actuated with a minimum resolution of 1 part in 64 as fixed by a 6 bit (minimum) ADC. Optoelectronic link is used between computer and power supply system.

Detector Bias

The Silicon Detector Bias voltages are set by the specification that all detector wafers are guaranteed to deplete at 55 volts. In order to minimize voltage potentials relative to Earth, the SVT will run with the Silicon Bias split above and below Earth potential. The Input offset bias and Edge Guard Offset are to minimize the voltage across the coupling capacitors, in case of a capacitor short. The specifications are summarized in Table 6.

Detector Voltage Control

The setting of all the voltages in the detector section is computer actuated with a 6 bit minimum resolution. Optoelectronic link is employed between computer and the power supply system.

MUX Board Supply

5 volts must be supplied to the front-ends of the Mux boards, biased up and down along with the Front-end electronics potential, to operate the Driver / Receiver communication with the Chips. Each Power Supply crate must also contain a +-5 volt supply, referenced at Earth Ground to supply the Back-ends of the Mux boards which contain the multiplexers and optical communications G-Link.

Specifications: TBD

Turn-on and Turn-off Sequences

In the turn-on process the FE chip supply voltages are applied first, in the following sequence: 1) 5V analog 2) 2V 3) 5V digital. Once this sequence is completed the detector bias voltage and the edge guard offset are applied.

In the turn-off operation the detector bias voltage and the edge guard offset are removed first, then the FE chip supply voltages are removed.

Voltage Ramping

The turn-on and off procedures are based upon linear ramping up and down of the voltages at rates that should not exceed 10V/s for the FE chip voltages and 15V/s for the detector bias.

Remote Sensing

The values of the supply voltages at the input of the FE chips are sensed and fed back to the power supply system in order to implement the closed-loop control of these voltages. No similar closed-loop action is deemed necessary in the detector section.

Monitoring

Provisions are made for monitoring the following parameters on each power supply module.

- The status ON/OFF of all generated voltages
- The values of all the FE chip voltages and the detector bias voltage. It must be pointed out that for the voltages that are closed- loop controlled, rather than simply monitoring those at the power supply output, the monitoring of their values at the HDI level becomes feasible.
- The values of the currents absorbed from all the supply voltages, from the detector bias and from the edge-guard bias.

Source Current Limits

On each power supply module, current limit monitors are provided for the detector bias and for the sources powering the front-end chips. The current limits are preset via computer for the detector bias voltage and by potentiometer for the other voltages. If the preset limits are exceeded, a command signal is generated with a delay of 10ms. This command activates the turn-off procedure on the detector bias if the current which exceeds the limit is that of the detector. If the current which exceeds the limit is relevant to any of the low voltage sources, the turn-off procedure of the power supply module is activated.

Source Voltage Limits

Voltage limit are preset by a potentiometer on all the voltages that power the front-end chips. If any of this limits is exceeded, with a delay of 1ms a command signal is generated which commands the turn-off of the power supply module.

Power Supply Interlocks

Each Power Supply Module must accept several external interlock inputs, which can prohibit the turn on of the supply, or shut it down in a controlled manner if it is on. The shut down sequence is the same as for a normal power down. Eight of the interlocks affect the entire system at once. The individual HDI over-temperature interlocks affect only the Power Supply Module supplying that module.

Interlock signal inputs must be asserted low TTL signals to allow operation. And are either asserted high when an interlock fault exists, or float high (i.e. High impedance) when the transmitting driver is not powered. The Interlock signal receiver must employ a pull-up resistor.

This is a list of interlock signals:

1. Single Power Supply Module interlocks:
    - Individual HDI over-temperature interlock
2. Power Supply System wide interlocks
    - SVT over-temperature interlock
    - Cooling system interlock (collected at Cooling system)
        - Cooling system off interlock
        - Cooling system flow rate interlock
        - Cooling system over-temperature interlock
    - Over-humidity interlock
    - Radiation burst interlock
    - Beam injection interlock
    - Nitrogen flow interlock

II-B-5 Detector Monitoring

There are four main areas of detector monitoring: radiation, position, temperature and humidity monitoring. The schedule for the design of all the SVT detector monitoring sytems is later than for the rest of the electronic readout, due to shorter lead time to procure the monitoring components and the fact that it is not directly coupled to the detector module assembly and testing. These requirements should be considered very preliminary and are still under development.

Radiation Monitoring

The radiation-monitoring system should be operational at all times when beams are present in the accelerator and the SVT is installed. The primary requirement of the radiation monitor system is to:

- protect SVT components from radiation damage by early detection of increasing radiation levels and triggering of the PEP-II beam abort system as well as interlocking of the SVT high-voltage system.

The secondary requirements of this system are to:

- provide real-time monitoring of slowly-varying radiation levels in the interaction region for accelerator tuning and diagnostics as well as for detector high-voltage interlocks, and
- to estimate the total integrated doses received by SVT detectors and front-end electronics.
- to conform with the interface requirements of the beam-abort system, the SVT high-voltage system, and the detector and accelerator control systems.

Position Monitoring

The primary requirement of the position monitoring system is to monitor the relative motions between the B1 magnets and the SVT, in order to ensure that no load is applied to the SVT. This system should be operational during mounting and unmounting of the SVT on the B1 magnets, during installation and removal of the support tube in the detector, and when the support tube is inside the detector.

The maximum relative motions allowed at the forward cone end is an angular motion of 2.25°, changing the large-end gap changes from nominal 9.81 mm to 0 mm while the small-end gap changes from nominal 3.67 mm to 2.68 mm. The maximum deflection due to gravity loading during support tube installation is 1.5–2.4 mm, depending on the support tube design. A deflection of 2.0 mm causes a 1.1 mrad relative rotation of both cones with respect to the B1 magnets, resulting in a 0.275 mm motion at the large end of cones.

The required sensitivity for the position monitoring system is to measure the expected deflections with 5–10% accuracy and measure gaps where contact can be made with accuracy of at least 1% of full range of motion.

A secondary goal for this system is to provide input for determining the alignment of the SVT with respect to the drift chamber. The alignment requirements for physics analysis are an overall spatial resolution $\simeq 10\ \mu$m.

Temperature Monitoring

The front-end electronics generates about 3 mW per channel, or about 500 W total for the 150,000 readout channels. The electronics is actively cooled with water, and should be shut down if for any reason the temperature rises significantly above the normal operating range. Providing a signal for a fail-safe interlock on the power supplies for the front-end is the primary requirement for the temperature monitoring system. There will be one resistive temperature monitor per HDI provided for this purpose.

The secondary requirements for temperature monitoring are to track temperature stability in order to monitor thermal expansion of the mechanical structure and any sensitivity of the SVT electronics to small excursions in temperature.

Stable temperatures for the detectors and support structures are needed so that we can meet the requirement that the relative positions of the various wafers be stable to the 5 μm level over long periods of time (months or more). This translates into a stability of $\pm 1^\circ$C.

The gain and shaping time of the SVT electronics are slightly sensitive to the temperature. However, this sensitivity should not be an issue for temperatures in the range $(20-50)^\circ$C, according to SPICE simulations.

Therefore, the main requirement for temperature stability is imposed by thermal expansion. To maintain temperatures to $\pm 1^\circ$C, the temperature should be measured to an accuracy of a fraction of a degree. This should be easy.

Humidity Monitoring

The primary requirement for the humidity monitors is that they must monitor the dew-point and, together with the temperature monitors, allow a determination of whether there is sufficient moisture in the environment and a low enough ambient temperature near the SVT detectors and electronics for condensation to occur. If the ambient temperature approaches the dew-point, action must be taken to either increase the purge rate with dry nitrogen, raise the temperature, or both.

References

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