



L1 Simulation Readiness Review

August 1st, 2005
SLAC

Eric Torrence
University of Oregon

Note: This is an overview. Most of this we will come back to in more detail later.



Review Agenda



Session 1: 11:00 - 12:30

Room: TBA

Time	Topic	Speaker
20+10	Overview	torrence
20+10	GLT	halyo
10+10	TSF	torrence/boyd

Session 2: 2:00 - 4:00

Room: Madrone Room

Teleconference: +1-510-665-5437, code 1574

Time	Topic	Speaker
10+10	BLT	torrence
10+10	PTD	torrence
15+10	ZPD	torrence
15+15	System integration and validation	torrence
30	Final discussion	



People Involved



Recently Active

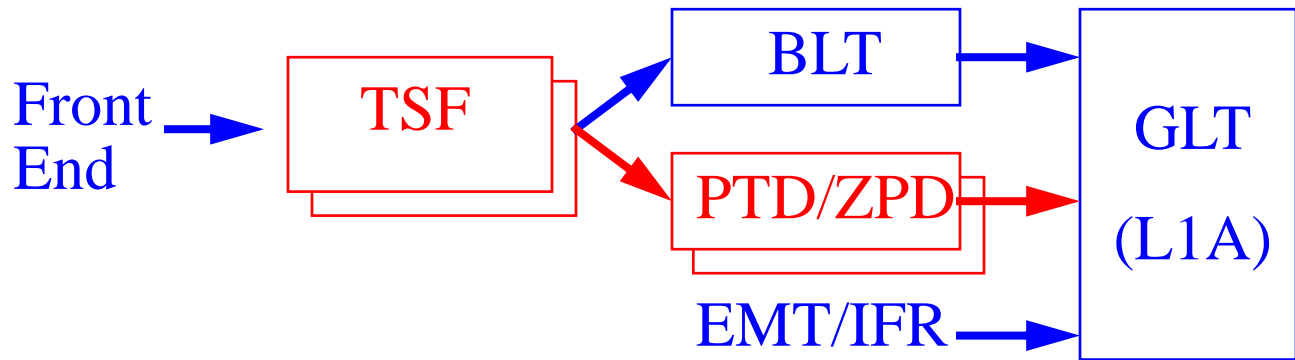
- Rainer Bartoldus
- Jamie Boyd
- Valerie Halyo
- Olya Igonkina
- SuDong
- Eric Torrence

Historically Involved

- Anders Borgland
- Gerald Grenier
- Nick Sinev
- Harvard ZPD team

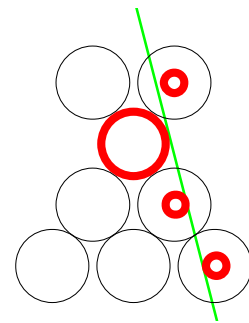


L1 Upgrade Overview



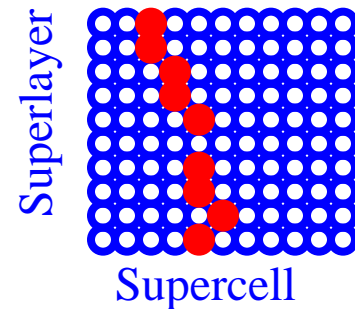
Track Segment Finder (TSF)

24 TSF boards, all replaced



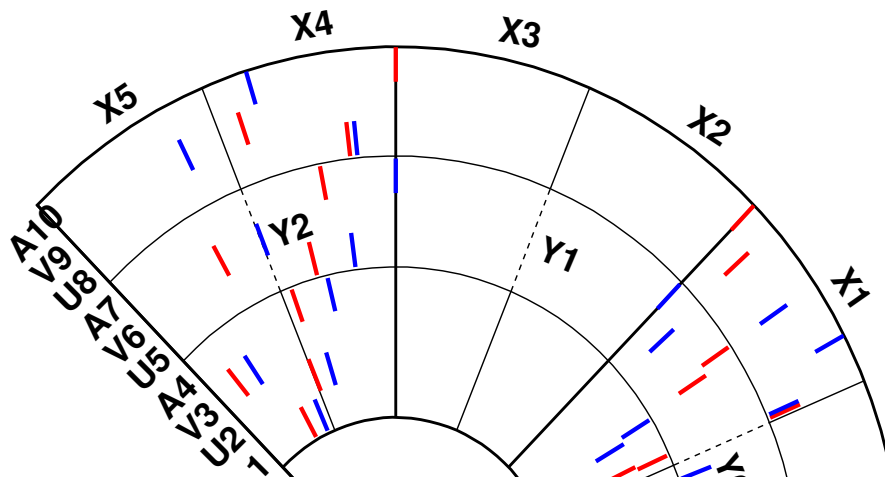
Binary Link Tracker (BLT)

1 BLT board, unchanged



P_T Discriminator (PTD)

8 PTD Boards, replace with ZPD





Scope of Software Project



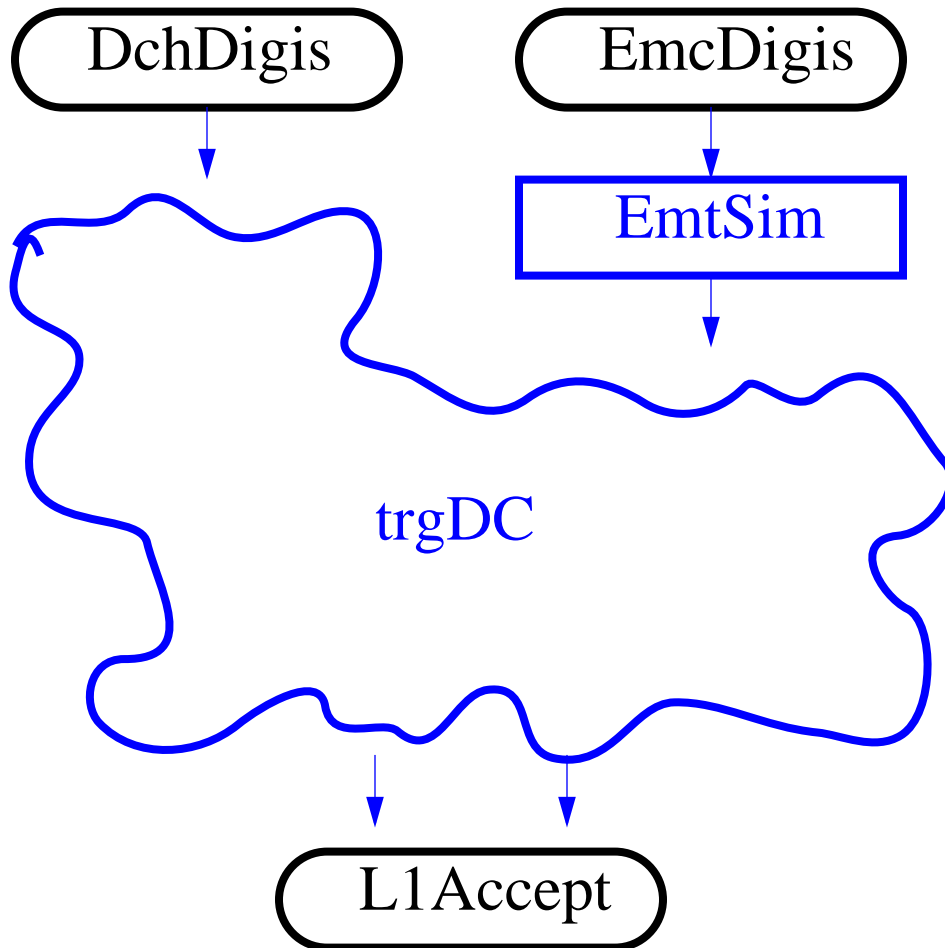
Overview of work done

- Simulation of new trigger boards (ZPD)
Required by L1 DCT upgrade
- Simulation of old trigger boards (PTD)
Replacement of trgDC
- New scheme for configuring trigger hardware properly from configDB
- New scheme to configure trigger simulation from same configDB as hardware
- Teststand validation of Hardware-simulation
- Online/offline software integration in IR2
- Simulation software integration into SP???

This review designed to cover items in red ONLY!



Starting Point

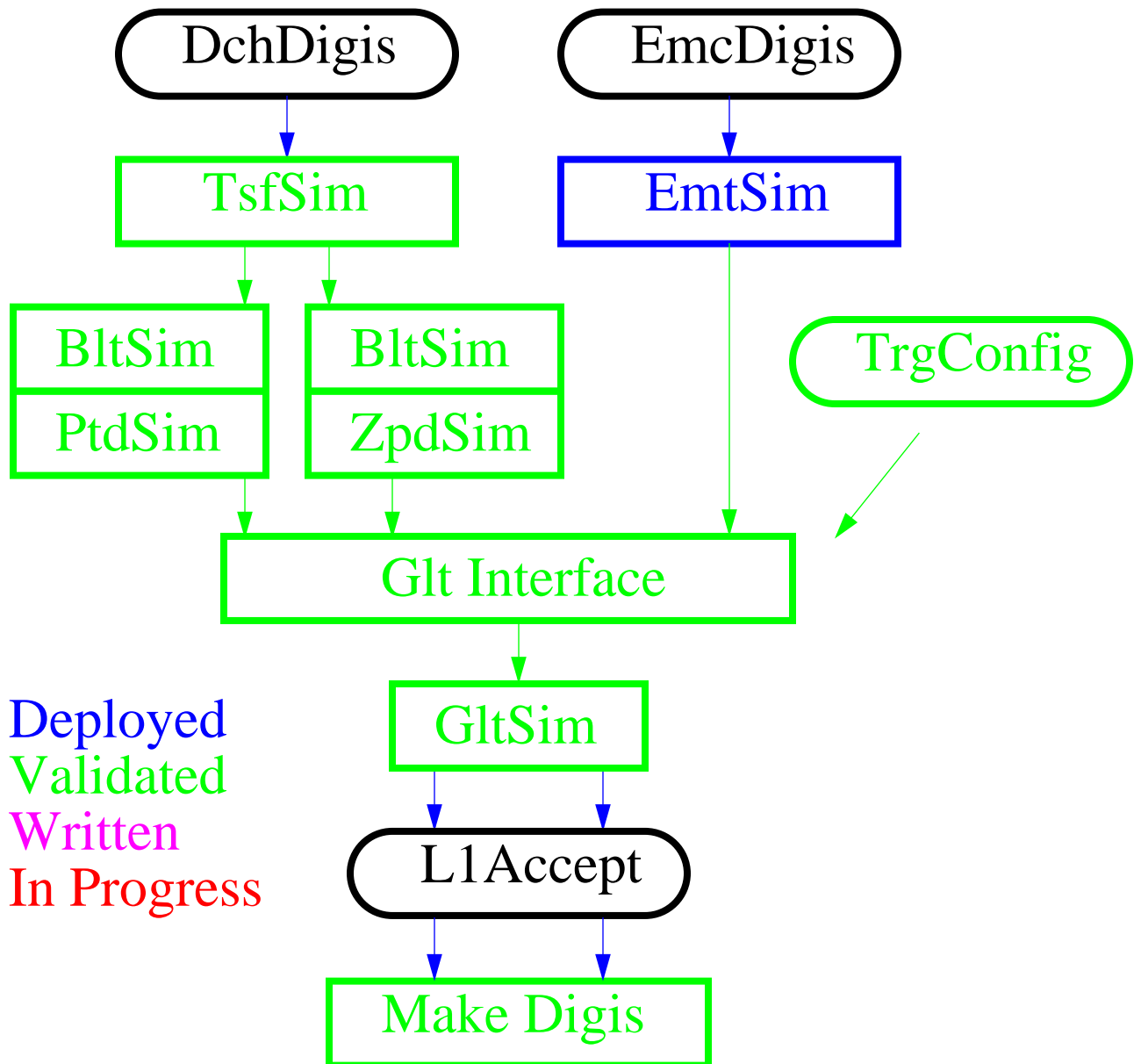


This IS the current SP8 (18.2.0)

This will not simulate Run5 data



New Code Layout



Individual framework modules to match hardware functions

Intermediate data passed by “timebuffers”

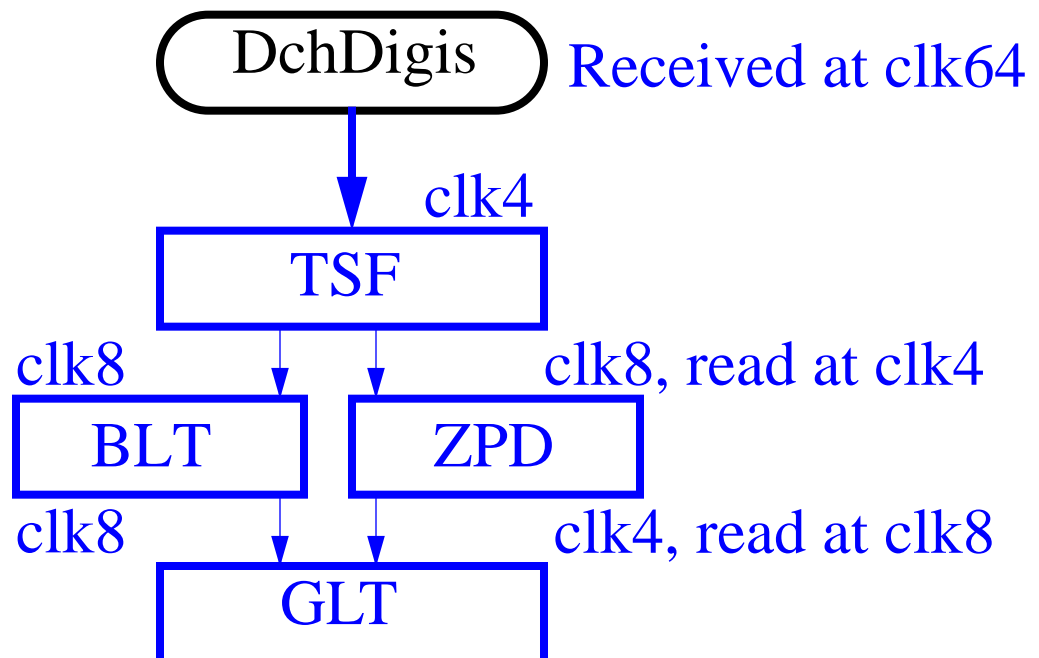


FCS Clocks



Clock	ν (MHz)	Divisor	2^n
BX	238	1	0
32	29.8	8	3
16	14.9	16	4
8	7.4	32	5
4	3.7	64	6

Trigger boards are basically FPGAs which exchange information at synchronous clock edges.





L1SimUtils



```
class<T> L1SimTimeBuffer ::  
    public vector<T>
```

- Stores **one tick** worth of data per vector element (e.g.: list of TSF segments)
- Demands **T.operator<<()** and **T.operator>>()** to provide standardized debugging I/O
- **L1SimTclInput** and **L1SimTclOutput** provide standard module I/O including from ASCII files
- TB indexed by **L1SimTickClock**, which are instantiated as **clk4**, **clk8**, etc.
- Simple utilities convert between clocks hiding complexity of **FcsSim**

Avoid clock phase problems which apparently plagued trgDC in the past

Provide data for hardware validation



L1Sim Output



L1 Accept Time

- Actually produced by **L1FctSim/L1FctDigiMaker**
- Based on L1GltSim output

L1 Digis

- Simulation of data written by boards
- e.g.: HepAList<L1DTsfDigi>
- Information distilled from detailed simulation output in timebuffers
- Readout window applied around L1A time
- Only TSF Digis used later (L3 tracking)
- Only basis for IR2 data-MC comparison



Configuration Overview



Hardware Config

- All configuration parameters are now in configDB and loaded to the boards
- No more file pointers

Simulation Config

- For Run5, simulation is configured from the same configDB entries as data
- For Runs 1-4, currently use “hardcoded” values (typically via tcl parameters)
- In some cases, have “fallback proxies”

Simulation-specific Config

- There are a few numbers (latencies) which are simulation-specific
- These are currently set via tcl
- Could be put in conditions some day...



MooseApp Test



```
Moose/AppUserBuildNewL1Sim.cc
#define SIMAPP_NEWL1SIM
#include "Moose/AppUserBuild.cc"
```

In nightly for last 2 months

```
Moose/AppUserBuild.cc
#ifdef SIMAPP_NEWL1SIM
    // New code here
#else
    // Old code here
#endif
```

**Necessary changes to production code
already in place, just not enabled by default**

**Plots shown today produced by this
code running in recent nightly**

tcl changes similarly encapsulated by

```
FwkCfgVar SimAppNewL1Sim false
if { $SimAppNewL1Sim } {
    # New tcl code
} else {
    # Old tcl code
}
```



L1SimSequence



New L1 Simulation Sequence

```
L1Sim/L1SimSequence  
L1DctSimSequence  
L1EmtSimSequence  
L1GltSimSequence  
L1FctSimSequence  
EidSimMakerModule*  
L1SimPPDigiSequence**
```

*Historical artifact, should be removed?

**Temp name to hold new Digi-making code

- Called directly from SimApp
- Rational hierarchy
- All L1Sim code in one place (in framework)

Most code is new, so no name-clash issues

Many exceptions have actually been renamed:

L1GltMakeDigis (trgDC) -> L1GltDigiMaker (new)



Config Loading



Old Code

```
L1TOepEnvSequence (AppUserBuild* forWhom) {
    BdbConfigInitSequence( forWhom );
    forWhom->add( new L1DctBuildEnv() );
    forWhom->add( new L1EmtBuildEnv() );

    // Load TSF LUT
    forWhom->add(new L1DctConfigLoader());
}
```

New Code (paraphrased)

```
L1DctSimSequence {

    // Setup environment
    new L1DctBuildEnv();
    new L1DctConfigLoader(); // Load TSF LUT
    new L1DctZpdLutLoader(); // Load ZPD LUT
    new L1DctBltMaskLoader(); // Load BLT Mask
    new L1DctLatencyLoader(); // Load latencies

    // Board simulation sequences
    L1DTsfSimSequence( forWhom );
    L1DBltSimSequence( forWhom );
    L1DPtdSimSequence( forWhom );
    L1DZpdSimSequence( forWhom );

}
```

Load directly in sequences which need them!



Framework Switching



Need to decide which trigger boards to simulate

TrigConfig - TRGGLTSOURCES

Listing of all modules contributing to trigger
BLT EMT PTD ZPD

L1DctSimSequence

```
if {[string first "ZPD" $TRGGLTSOURCES]<0} {  
  ErrMsg routine "L1DctSimSequence:  
  ZPD not found in TRGGLTSOURCES,  
  disable L1DZpdSimSequence"  
  sequence disable L1DZpdSimSequence  
}  
  
if {[string first "PTD" $TRGGLTSOURCES]<0} {  
  ErrMsg routine "L1DctSimSequence:  
  PTD not found in TRGGLTSOURCES,  
  disable L1DPtdSimSequence"  
  sequence disable L1DPtdSimSequence  
}
```

Switching is done in same sequence where
modules are included...

Also being used to 'hardcode' old config values
e.g.: BLT mask, DCT latencies



Readiness Criteria



Simulation readiness

- L1A decision (L1 line rates)
- L1A mean time (t0 input)
- TSF segments (L3 tracking)
- L1A width (potential impact on SVT/DIRC)

Listed in rough priority order (my view)

Even L1 decision irrelevant for 95%
of BaBar physics...

Integration readiness

- Configuration works properly
- Full Run1-Run5 samples can be produced
- L1 outputs are unchanged for downstream consumers



Data Samples



Data Samples (from XTC)

May2004 and May2005 data samples
HadronicBScript, L3OutMuPair, L3OutBhabhaFlat

New MC Simulation (Moose)

May2004 and May2005 configKey
BB (default), e^+e^- (bhwide), $\mu^+\mu^-$ $\tau^+\tau^-$ (kk)

No background frames for 2005!

Also, $\tau^+\tau^-$ for May 2000-2003

Old MC Simulation (Moose)

May2004 configKey
BB (default), e^+e^- (bhwide), $\mu^+\mu^-$ $\tau^+\tau^-$ (kk)



Tentative Conclusions (Eric)



With a couple of exceptions, L1 Simulation looks good from where we sit

System integration issues are well in hand with new MooseApp

Broader validation of physics quantities would be most easily facilitated by full-blown validation and QA running

New simulation is at least as good as trgDC for runs 1-4, and at least in one place better

We hope to convince you of this today...