



Binary Link Tracker

L1Sim Readiness Review

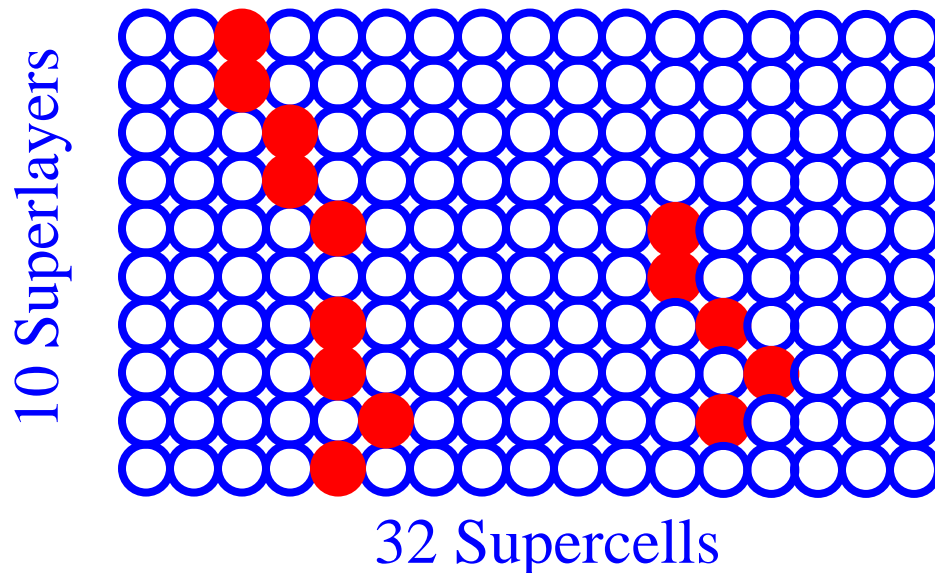
August 1st, 2005

SLAC

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BLT Algorithm



- Input stretched TSF segments
- One bit per 32x10 **supercell**
- Correct **stereo** superlayers (+/- 1)
- Apply BLT mask (**force supercell ON**)
- Link tracks from contiguous hits
+/- 1 or 2 depending upon Axial/Stereo transition
- Allow for few missing superlayers
- Final product: **A tracks (SL10) B tracks (SL5)**
- To GLT: **2 x 16 bit word each clk8**
Each bit is 1/16th in phi at SL5 or SL10

New system uses same board as old



BLT Simulation Code



<u>Module</u>	<u>Input</u>	<u>Output</u>
L1DBltReducer	vec<L1DTsfSimDigi>	L1DBltHitMap
Change TSF segments into 10x32 Supercell hit map Actually part of the physical TSF board		
L1DBltSimModule	L1DBltHitMap	2xL1DBltPhiMap
Core algorithm, apply stereo rotation, apply mask, find A & B tracks in 32 phi bins create single A/B phi map per clk8 tick		
L1DBltPrePost	2xL1DBltPhiMap	2xL1DBltPhiMap
Pre-post (stretch) phi maps by +/- 1 tick Reduce 32 bins -> 16 bins in phi (not trivial)		



BLT Configuration



BLT Mask

- 10 32-bit words giving supercells always **ON**
- Now properly in configDB - **L1DBltMask**
- Previously was a file pointer for hardware
- Hardcoded (wrong) in trgDC

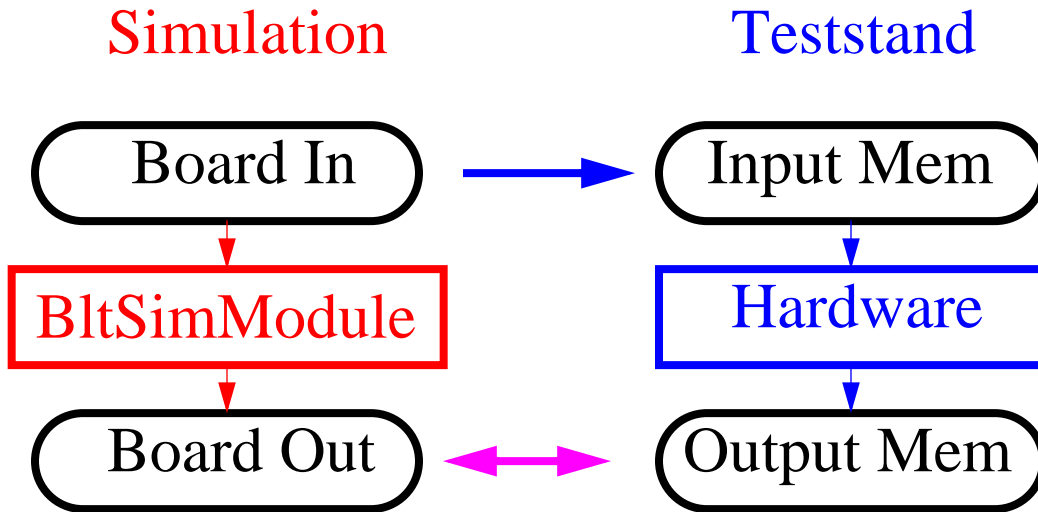
(Almost) never changed in Run1-4
Hardcode value using tcl (SL6, SC29)

BLT DAQ Latency

- Now properly in configDB
L1DBltZpdSimpleConfig
- Previously a magic number in a text file?
- Somewhat arbitrary number for simulation
Only effects monitoring output WRT L1A

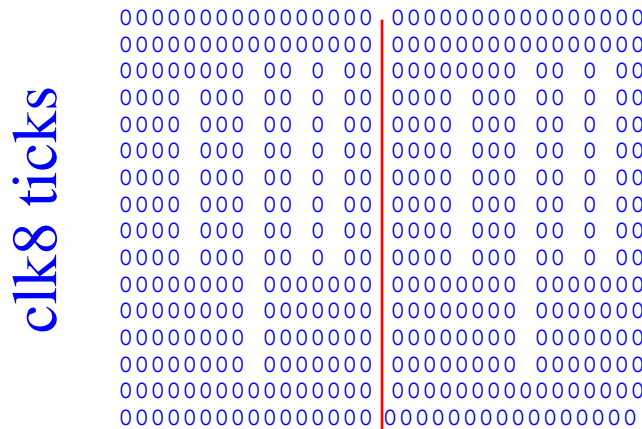


BLT Teststand Validation



- Run Moose, dump input and output TB for **L1DBltSimModule**
- Convert to memory maps for **teststand**
- Load input register of real board, and clock through full event
- **Compare board output with simulated output**

16 phi bins (A tracks)



Done with Nick Berger, 1000 events



BLT OepMuPair Comparison

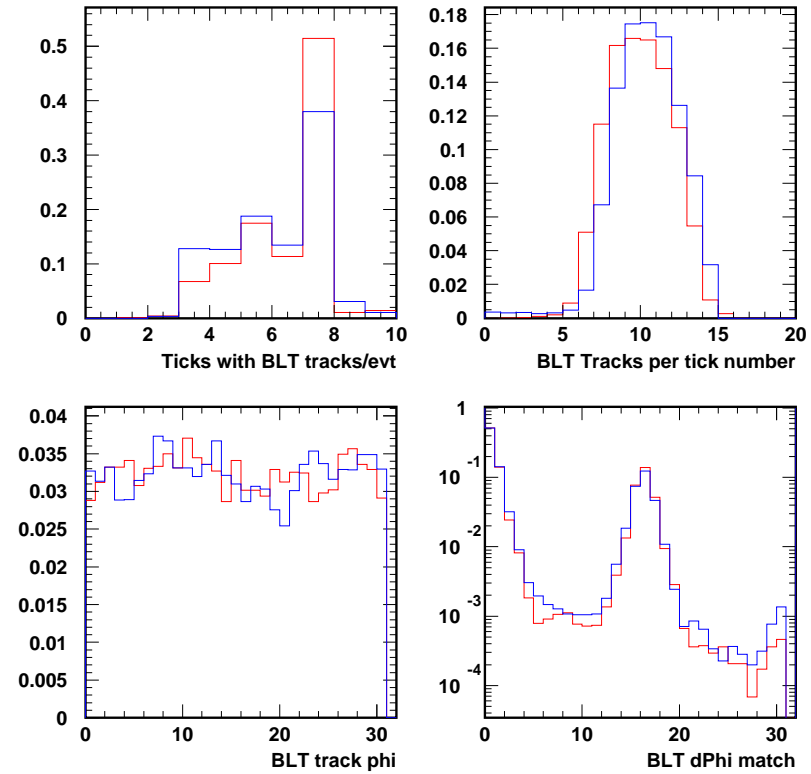
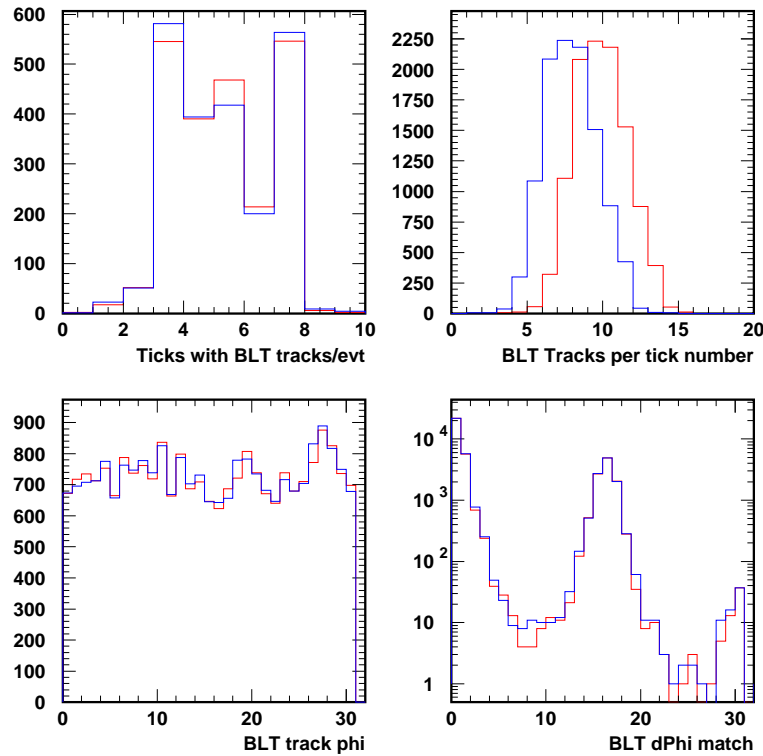


trgDC vs newSim

r48145 vs newSim

trgDC-L1Sim mupair BLT A 2005/07/31 13.16

r48145 - L1Sim BLT B 2005/07/31 13.17



BLT A Tracks

BLT B Tracks

see <plots/blt/bltMuStudy.ps> for more



BLT HadronicBScript Comparison



trgDC vs newSim

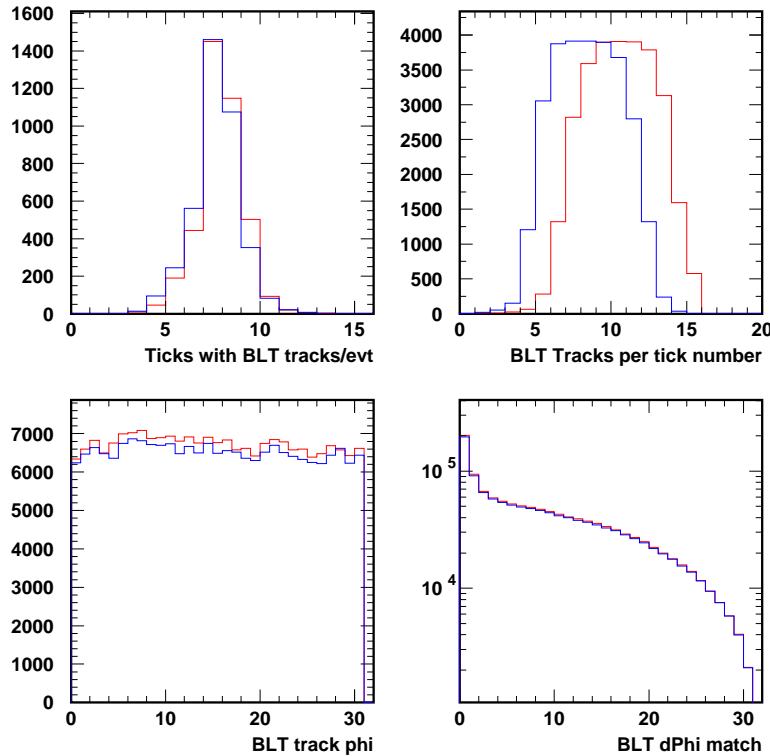
r48145 vs newSim

trgDC-L1Sim BBbar BLT B

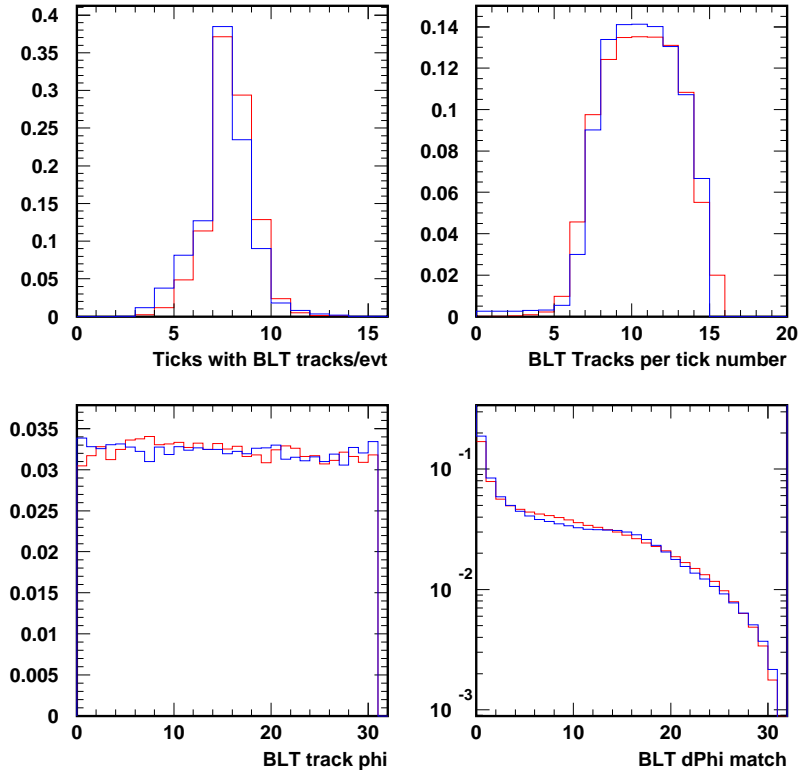
2005/07/31 18.10

r48145 - L1Sim BLT B

2005/07/31 18.12



BLT A Tracks



BLT B Tracks

see <plots/blt/bltHadStudy.ps> for more

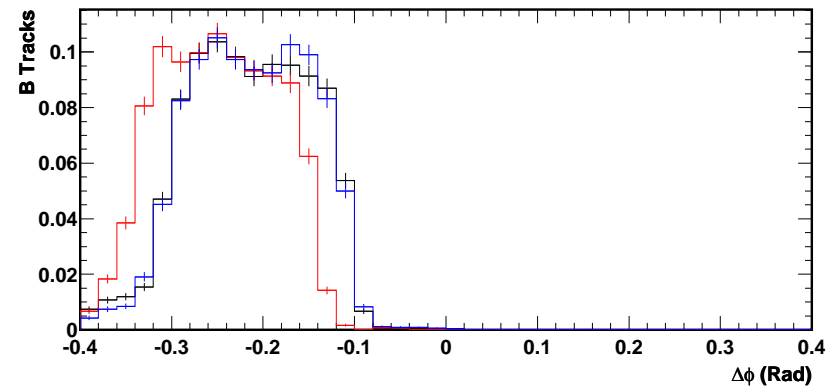
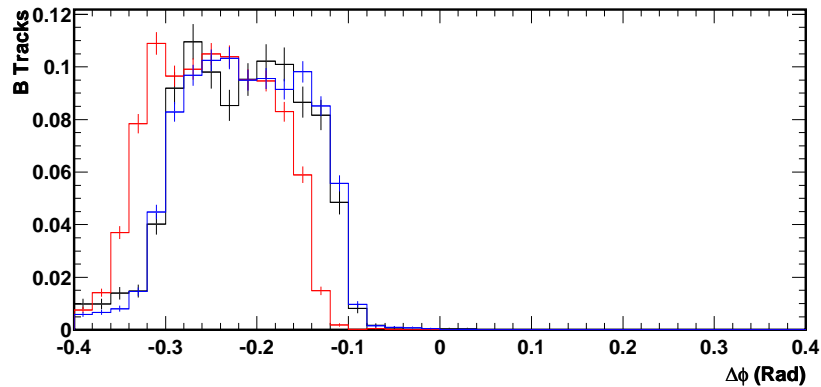
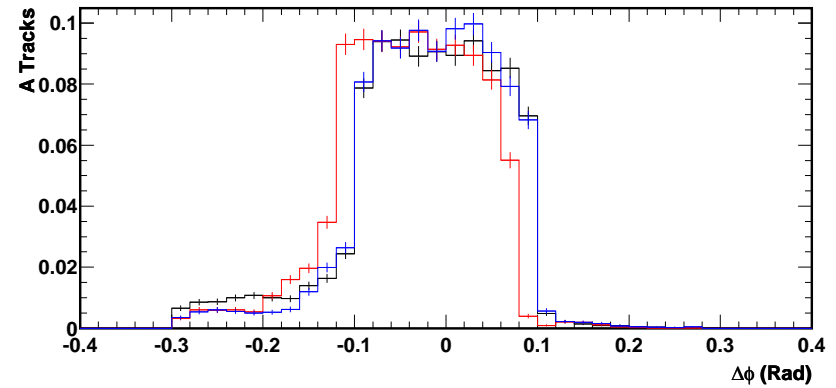
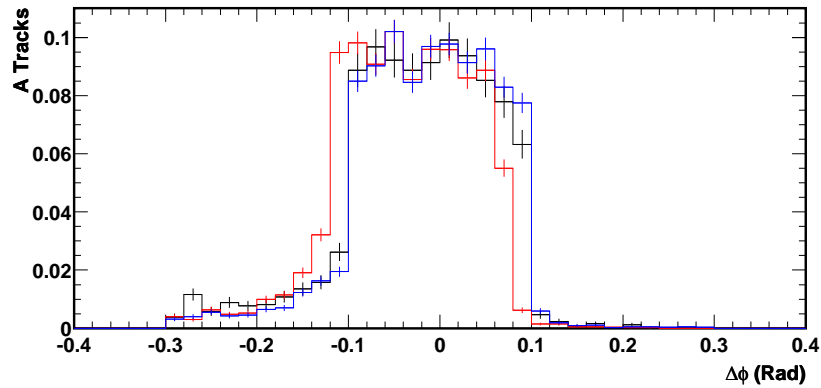


Reco Track Residuals



MuPair

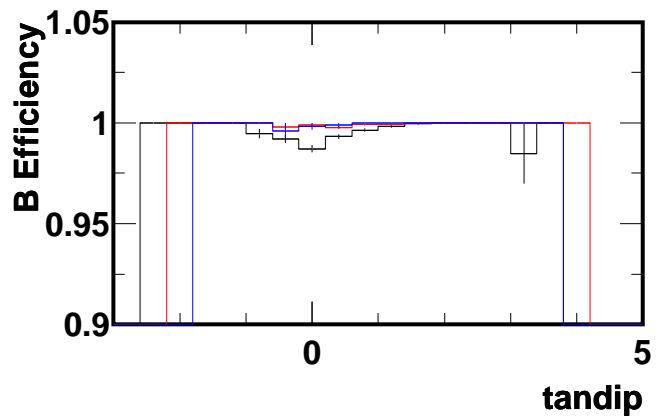
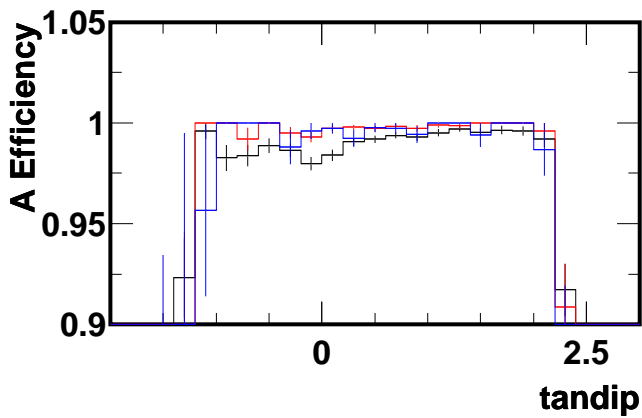
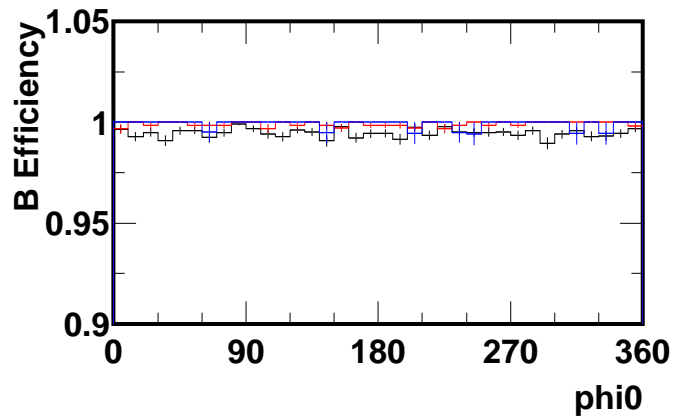
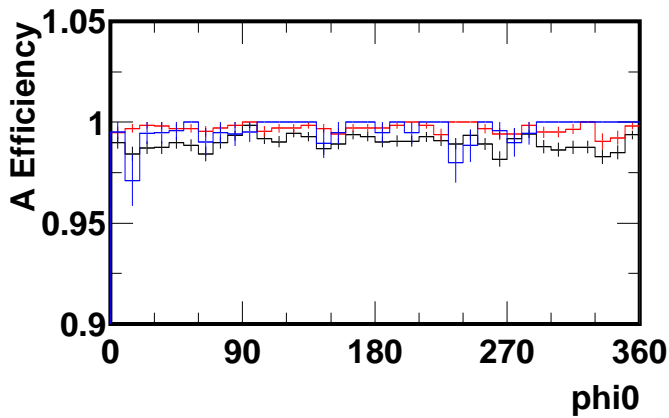
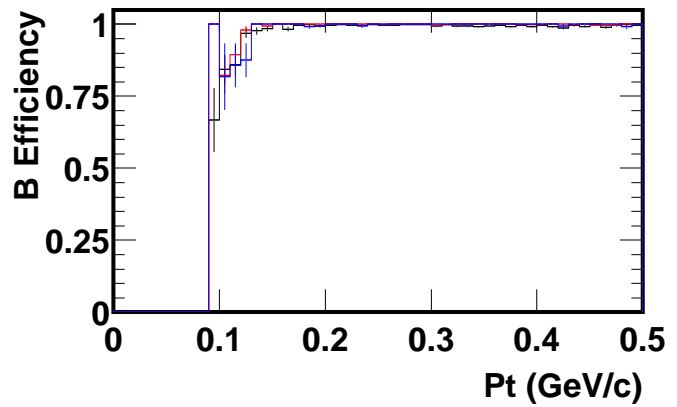
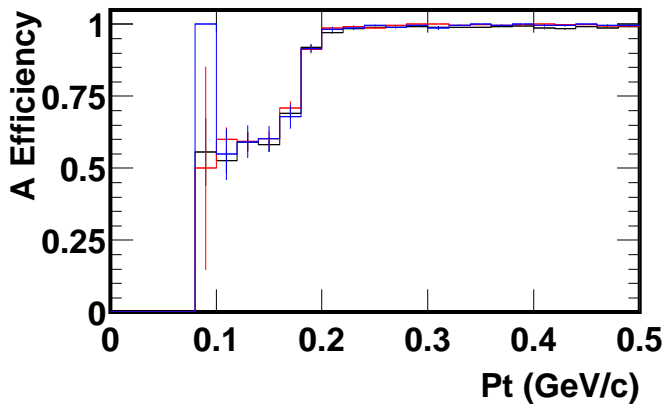
Bhabha



r48145 vs trgDC vs newSim



BBbar OprMon Comparison



r48145 vs **trgDC** vs **newSim**



BLT Simulation Status



New code almost identical to trgDC

Still would like to test TSF->BLT
data path on teststand

Simulation appears more than adequate
for production