

16-Jul-02							FC / Data Receiver	Finder/Filter 0	Finder/Filter 1	Finder/Filter 2	Finder/Filter 3	Finder/Filter 4	Finder/Filter 5	Decision Module	System ACE	Front Panel	Comment	
Group	PinGrid	Traces	Protocol															
Signal	Name		Drive	Drive termination	Receive	Far end termination												
<b>ZPDi I/O</b>																		
SEGMENTS[152:0]	(#s only)	153	LVDCI_33	on ZPDi	LVC MOS33	no	I										J1 and J2	
FRAME_IN[8:0]	FR	9	LVDCI_33	on ZPDi	LVC MOS33	no	I										actually send clk60 now	
CLK8_OUT	Clk8	2	LVDS	no	LVDS	yes	O											
DECISION[7:0]	DO	8	LVDCI_33	on chip	LVC MOS33	no								O				
SPARE		1					IO											
<b>FC I/O</b>																		
CLINK	CLNK	1	TTL		TTL		I										J3 Buffered by SN74LVT245B	
DLINK	DLNK	1	TTL		TTL		O											
CCLK	CCK	2	ECL		LVDS	on board	I										ECL to LVDS passive network	
DCLK	DCK	2	ECL		LVDS	on board	I										ECL to LVDS passive network	
GA[3:0]	GA	4	TTL		TTL		I											
<b>MegaBus and Friends</b>																		
MEGABUS[74:0]	(#s only)	150	LVDS	on board	LVDS	on board	O	I	I	I	I	I	I	I				
FRAME	Frame	2	LVDS	on board	LVDS	on board	O	I	I	I	I	I	I					
CLK60A	Clk60	2	LVDS	on board	LVDS	on board	O	I	I	I	I	I	I					
CLK60B	Clk60B	2	LVDS	on board	LVDS	on board	O							I				
CLK4A	Clk4	2	LVDS	on board	LVDS	on board	O	I	I	I	I	I	I					
CLK4B	Clk4B	2	LVDS	on board	LVDS	on board	O							I				
<b>MiniBus and Friends</b>																		
MINIBUS[15:0]	MB	16	LVC MOS	no	LVC MOS	no	IO	IO	IO	IO	IO	IO	IO	IO			Addr or Data	
STRB_ADDR	S_A	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I				
DATA_LO	D-LO	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I				
DATA_HI	D-HI	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I				
LONG_WORD	LW	1	LVC MOS	no	LVC MOS	no	O	I	I	I	I	I	I	I			32 vs 16 bit Read/Write	
READ_SELECT	R-S	1	LVC MOS	no	LVC MOS	no	O	I	I	I	I	I	I	I			1=read; 0=write	
CS0A	CS0A	1	LVC MOS	no	LVC MOS	no	O	I									Chip Selects	
CS0B	CS0B	1	LVC MOS	no	LVC MOS	no	O	I										
CS1A	CS1A	1	LVC MOS	no	LVC MOS	no	O		I									
CS1B	CS1B	1	LVC MOS	no	LVC MOS	no	O		I									
CS2A	CS2A	1	LVC MOS	no	LVC MOS	no	O			I								
CS2B	CS2B	1	LVC MOS	no	LVC MOS	no	O			I								
CS3A	CS3A	1	LVC MOS	no	LVC MOS	no	O				I							
CS3B	CS3B	1	LVC MOS	no	LVC MOS	no	O				I							
CS4A	CS4A	1	LVC MOS	no	LVC MOS	no	O					I						
CS4B	CS4B	1	LVC MOS	no	LVC MOS	no	O						I					
CS5A	CS5A	1	LVC MOS	no	LVC MOS	no	O							I				
CS5B	CS5B	1	LVC MOS	no	LVC MOS	no	O								I			
CS_DM	CS-DM	1	LVC MOS	no	LVC MOS	no	O									I		
<b>DAQ Memory Access</b>																		
L1A	L1A	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I			DAQ data goes onto MiniBus Copy data to buffer	
L1A_DAQ_BUF[1:0]	WDB	2	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I	I	I			Buffer address for L1A	
RETURN_BUF	RD_E	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I			Prepare to readout DAQ buffer	
RET_DAQ_BUF[1:0]	RDB	2	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I	I	I			Buffer address for read event	
ERROR	ERR	1	LVC MOS	no	LVC MOS	on board	I	O	O	O	O	O	O	O			Pulled low; drive high for error	
DAQ_RST	DAQR	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I	I			DAQ buffer reset	
<b>Diagnostic Memory Control</b>																		
EN_MEM_FF	E_MF	1	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I	I				F/F diagnostic mem enable	

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			Drive	Drive termination	Receive	Far end termination											
PLAY_MEM_MB	P_MM	1	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I				MegaBus mem	
PLAY_MEM_FIND	P_M_FR	1	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I				1=Play; 0=Record	
PLAY_MEM_FIT	P_MF	1	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I				1=Play; 0=Record	
EN_MEM_DM	E_MDM	1	LVDCI_33	on chip	LVC MOS	no	O						I			Output diagnostic mem enable	
PLAY_MEM_DMFI T	P_MDF	1	LVDCI_33	on chip	LVC MOS	no	O						I			Fit results mem	
PLAY_MEM_OUT	P_MO	1	LVDCI_33	on chip	LVC MOS	no	O						I			1=Play; 0=Record	
ONESHOT_MEM	OS_M	1	LVDCI_33	on chip	LVC MOS	no	O	I	I	I	I	I	I			1=single; 0=continuous play	
START_MEM	S_M	1	LVC MOS	no	LVC MOS	on board	O	I	I	I	I	I	I			Start strobe	
<b>Fit Results</b>																	
FIT_RESULTS0[11:0]	FR0_	12	LVDCI_33	on chip	LVC MOS	no		O					I				
FIT_RESULTS1[11:0]	FR1_	12	LVDCI_33	on chip	LVC MOS	no			O				I				
FIT_RESULTS2[11:0]	FR2_	12	LVDCI_33	on chip	LVC MOS	no				O			I				
FIT_RESULTS3[11:0]	FR3_	12	LVDCI_33	on chip	LVC MOS	no					O		I				
FIT_RESULTS4[11:0]	FR4_	12	LVDCI_33	on chip	LVC MOS	no						O	I				
FIT_RESULTS5[11:0]	FR5_	12	LVDCI_33	on chip	LVC MOS	no							O	I			
<b>Miscellaneous</b>																	
LA_DD[15:0]	LA	16	LVC MOS				O									Logic Analyzer	
LA_FF0[31:0]	LA	32	LVC MOS					O								small connector + berg	
LA_FF1[31:0]	LA	32	LVC MOS						O								
LA_FF2[31:0]	LA	32	LVC MOS							O							
LA_FF3[31:0]	LA	32	LVC MOS								O						
LA_FF4[31:0]	LA	32	LVC MOS									O					
LA_FF5[31:16]	LA	16	LVC MOS										O			only 16 upper bits	
LA_DM[31:0]	LA	32	LVC MOS											O			
XBUS[7:0]	XB	8					IO	IO	IO	IO	IO	IO	IO	IO		Exta bus for contingency	
FF0_GA[2:0]	GA	3			PWR/GND			I								Global Address	
FF1_GA[2:0]	GA	3			PWR/GND				I							hardwired	
FF2_GA[2:0]	GA	3			PWR/GND					I							
FF3_GA[2:0]	GA	3			PWR/GND						I						
FF4_GA[2:0]	GA	3			PWR/GND							I					
FF5_GA[2:0]	GA	3			PWR/GND								I				
LOCALCLK1	CLK1	1				on board	I										
LOCALCLK2	CLK2	1				on board									I		
CONFIG_LED	CNFG	8	LV TTL				O	O	O	O	O	O	O	O		next to each FPGA	
RUN	RUN	1	LVC MOS				O	I	I	I	I	I	I				
RESET	RESET	1	LVC MOS				O	I	I	I	I	I	I				
ACE_DONE_IN	A_DN	1	LV TTL	no	LV TTL	no							I			tied to ACE_DONE line, for LED	
<b>Front Panel</b>																	
POWER_LED[3:0]		6	LV TTL													x	
SOFTWARE_LED[3:0]	S_L	4	LV TTL				O									x	
COUNTER_A[23:0]	CT_A	24	LV TTL										O			12x2 LED array	
CONFIG_LED	CF_L	1	LV TTL										O			global config, from ACE_DONE	
RUN_LED	R_L	1	LV TTL										O			Blue. On=RUN mode	
SYSRESET		1	LV TTL											I		Recessed reset button	
EN_LED_IN	E_L_I	1	LV TTL				O									Diag. Mem status	
PLAY_LED_IN	P_L_I	1	LV TTL				O									x	
ACTIVE_LED_IN	A_L_I	1	LV TTL				O									x	

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			Signal	Name	Drive											
EN_LED_FF	E_L_F	1	LVTTTL				O								x	could use EN_MEM_FF
PLAY_LED_MB	P_LMB	1	LVTTTL				O								x	
PLAY_LED_FIND	P_LFD	1	LVTTTL				O								x	
PLAY_LED_FIT	P_L_F	1	LVTTTL				O								x	
ACTIVE_LED_FF	A_L_F	1	LVTTTL				O								x	
EN_LED_DM	E_LDM	1	LVTTTL										O		x	could use EN_MEM_OUT
PLAY_LED_DMFIT	P_LDM	1	LVTTTL										O		x	
PLAY_LED_OUT	P-L-O	1	LVTTTL										O		x	
ACTIVE_LED_DM	A_LDM	1	LVTTTL										O		x	
ONESHOT_LED	OS_L	1	LVTTTL										O		x	
DM_CTS		1											I		x	To debug port via buffer
DM_DCD		1											I		x	"
DM_DTR		1											O		x	"
DM_RTS		1											O		x	"
DM_RXD		1											I		x	"
DM_SHDN		1											O		x	"
DM_TXD		1											O		x	"
<b>System ACE</b>																
ACE_DATA[7:0]	D	8	LVTTTL	no	LVTTTL	no	I	I	I	I	I	I	I	O		
ACE_CS0	CSB	1	LVTTTL	no	LVTTTL	no	I							O		
ACE_CS1	CSB	1	LVTTTL	no	LVTTTL	no	I	I	I					O		
ACE_CS2	CSB	1	LVTTTL	no	LVTTTL	no				I	I	I		O		
ACE_CS3	CS_B	1	LVTTTL	no	LVTTTL	no							I	O		
ACE_INIT	INIT_B	1	LVTTTL	no	LVTTTL	no	O	O	O	O	O	O	O	I		open drain
ACE_DONE	DONE	1	LVTTTL	no	LVTTTL	no	O	O	O	O	O	O	O	I		open drain
ACE_MODE[2:0]	M	3	LVTTTL	no	LVTTTL	no	I	I	I	I	I	I	I	O		hardwire?
ACE_CCLK	CCLK	1	LVTTTL	no	LVTTTL	on board	I	I	I	I	I	I	I	O		buffered
ACE_RDWR_B	RDWR_B	1	LVTTTL	no	LVTTTL	no	I	I	I	I	I	I	I	O		
ACE_PROGRAM_B	PROG_B	1	LVTTTL	no	LVTTTL	no	I	I	I	I	I	I	I	O		reset drives low
ACE_STATUS[3:0]		4	LVTTTL											O		status LEDs
<b>JTAG</b>																
TDI	TDI	1	LVTTTL		LVTTTL		I	I	I	I	I	I	I	I		TDI -> TDO chain
TDO	TDO	1	LVTTTL		LVTTTL		O	O	O	O	O	O	O	O		
TMS	TMS	1	LVTTTL		LVTTTL		I	I	I	I	I	I	I	I		buffered
TCK	TCK	1	LVTTTL		LVTTTL	on board	I	I	I	I	I	I	I	I		buffered
<b>Total Traces:</b>		814														